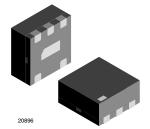


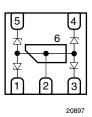
4-Line (Quad) ESD Protection Diode Array in LLP1010-6L

Features

- Ultra compact LLP1010-6L package
- Low package height < 0.4 mm
- 4-line ESD protection (quad)
- Low leakage current < 0.1 μA
- Low load capacitance C_D = 12 pF
- ESD-protection acc. IEC 61000-4-2
 - ± 15 kV contact discharge
 - ± 17 kV air discharge
- Surge current acc. IEC 6100-4-5 I_{PP} > 2.5 A
- Soldering can be checked by standard vision inspection. No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC







Marking (example only)



Dot = Pin 1 marking X = Date code

Y = Type code (see table below)

Ordering Information

Device name Ordering code		Taped units per reel (8 mm tape on 7" reel)	Minimum order quantity		
VESD05A4A-HS4	VESD05A4A-HS4-GS08	5000	5000		

Package Data

Device name	Package name	Type code	Weight	Molding compound flammability rating	Moisture sensitivity level	Soldering conditions
VESD05A4A-HS4	LLP1010-6L	Α	1.07 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

^{**} Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

VESD05A4A-HS4

Vishay Semiconductors



Absolute Maximum Ratings

Rating	Test conditions			Value	Unit
Peak pulse current	BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot			2.5	Α
	BiSy-mode: each input (pin 1, 3 to 5) to any other input Pin 2 and 6 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$;	I _{PPM}	2.5	А	
Pook pulgo power	BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot			30	W
Peak pulse power	BiSy-mode: each input (pin 1, 3 to 5) to any other input pin. Pin 2 and 6 not connected. Acc. IEC 61000-4-5; t_p = 8/20 μ s; single shot			33	W
ESD immunity	Acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6)	Contact discharge	V _{ESD}	± 15	kV
		Air discharge	V _{ESD}	± 17	kV
	Acc. IEC 61000-4-2; 10 pulses BiSy-mode: each input (pin 1, 3 to 5) to any other input pin.	Contact discharge	V _{ESD}	± 15	kV
	Pin 2 and 6 not connected.	Air discharge	V _{ESD}	± 17	kV
Operating temperature	Junction temperature			- 40 to + 125	°C
Storage temperature				- 55 to + 150	°C

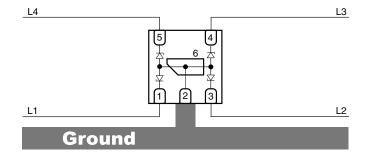
<u>BiAs-Mode (4-line Bidirectional Asymmetrical protection mode)</u>

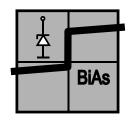
With the **VESD05A4A-HS4** up to 4 signal- or data-lines (L1 to L4) can be protected against voltage transients. With pin 2 and 6 connected to ground and pin 1, 3, 4 and 5 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified **Maximum Reverse Working Voltage** (**V**_{RWM}) the protection diode between data line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The Clamping Voltage (V_C) is defined by the BReakthrough Voltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low Forward Voltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the **VESD05A4A-HS4** clamping behaviour is **Bi**directional and **As**ymmetrical (**BiAs**).





20898



Electrical Characteristics

Ratings at 25 °C, ambient temperature unless otherwise specified

VESD05A4A-HS4

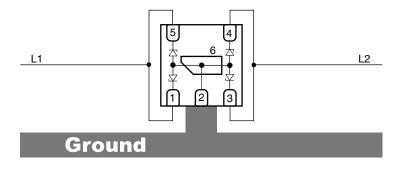
BiAs mode: each input (pin 1, 3, 4 and 5) to ground (pin 2 and/or 6)

Parameter	Test conditions/remarks	Symbol	Min.	Тур.	Max.	Unit
Protection paths	Number of line which can be protected	N _{lines}			4	lines
Reverse stand-off voltage	at I _R = 0.1 μA	V _{RWM}	5			V
Reverse current	at $V_R = V_{RWM} = 5 \text{ V}$	I _R		< 0.01	0.1	μΑ
Reverse breakdown voltage	at I _R = 1 mA	V _{BR}	6		8	V
Clamping voltage	at I _{PP} = 2.5 A acc. IEC 61000-4-5	V _C			12	V
Forward clamping voltage	at I _F = 2.5 A acc. IEC 61000-4-5	V _F			2.5	V
Capacitance	at V _R = 0 V; f = 1 MHz	C _D		12	15	pF
	at V _R = 2.5 V; f = 1 MHz	C _D		7.5	8.5	pF

If a higher surge current or peak pulse current (I_{PP}) is needed, some protection diodes in the **VESD05A4A-HS4** can also be used in parallel in order to "multiply" the performance.

If two diodes are switched in parallel you get

- double surge power = double peak pulse current (2 x I_{PPM})
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line Capacitance (2 x C_D)
- double Reverse leakage current (2 x I_R)



20900

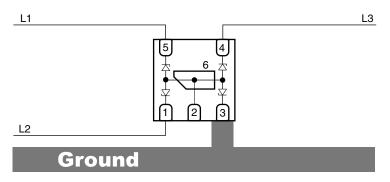


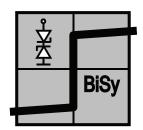
BiSy-mode (3-line Bidirectional Symmetrical protection mode)

If a bipolar symmetrical protection device is needed the **VESD05A4A-HS4** can also be used as a three-line protection device. Therefore three pins (example: pin 1, 3, and 5) has to be connected to the signal- or dataline (L1 to L3) and pin 3 to ground. Pin 2 and 6 must not be connected!

Positive and negative voltage transients will be clamped in the same way. The clamping current from one data line through the **VESD05A4A-HS4** to the ground passes one diode in forward direction and the other one in reverse direction. The **C**lamping **V**oltage (V_C) is defined by the **BR**eakthrough **V**oltage (V_{BR}) level of one diode plus the forward voltage of the other diode plus the voltage drop at the series impedances (resistances and inductances) of the protection device.

Due to the same clamping levels in positive and negative direction the **VESD05A4A-HS4** voltage clamping behaviour is also **Bi**directional and **Sy**mmetrical (**BiSy**).





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Electrical Characteristics

Ratings at 25 °C, ambient temperature unless otherwise specified

VESD05A4A-HS4

BiSy mode: each input (pin 1, 3, 4 or 5) to any other input pin connected to ground; pin 2 and 6 not connected

Parameter	Test conditions/remarks	Symbol	Min.	Тур.	Max.	Unit
Protection paths	Number of line which can be protected	N _{lines}			3	lines
Reverse stand-off voltage	at $I_R = 0.1 \mu A$	V_{RWM}	5.5			V
Reverse current	at $V_R = V_{RWM} = 5.5 \text{ V}$	I _R		< 0.01	0.1	μΑ
Reverse breakdown voltage	at I _R = 1 mA	V_{BR}	6.5		8.7	V
Clamping voltage	at I _{PP} = 2.5 A acc. IEC 61000-4-5	V _C		11.5	13	V
Capacitance	at $V_R = 0 V$; $f = 1 MHz$	C _D		6	8	pF
	at $V_R = 2.5 \text{ V}$; $f = 1 \text{ MHz}$	C _D		5	7	pF



Typical Characteristics (T_{amb} = 25 °C, unless otherwise specified)

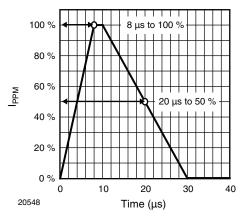


Figure 1. 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

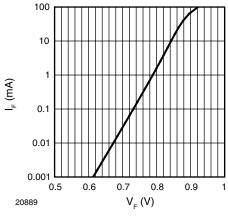


Figure 4. Typical Forward Current $I_{\textrm{F}}$ vs. Forward Voltage $V_{\textrm{F}}$

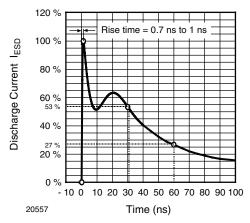


Figure 2. ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 $\Omega/150$ pF)

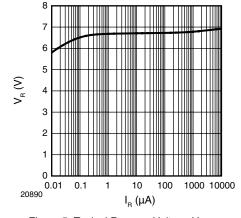


Figure 5. Typical Reverse Voltage V_R vs. Reverse Current I_R

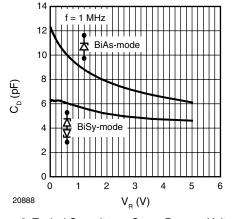


Figure 3. Typical Capacitance C_{D} vs. Reverse Voltage V_{R}

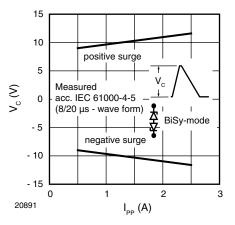


Figure 6. Typical Peak Clamping Voltage $V_{\rm C}$ vs. Peak Pulse Current $I_{\rm PP}$



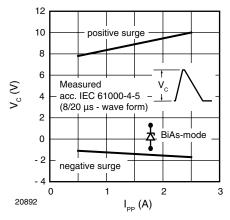


Figure 7. Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

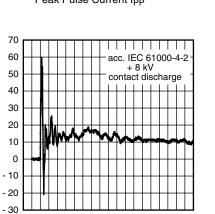


Figure 8. Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

40

t (ns)

50 60 70 80 90

10 20 30

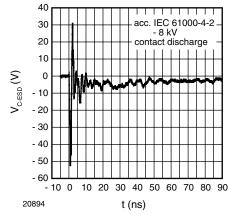


Figure 9. Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

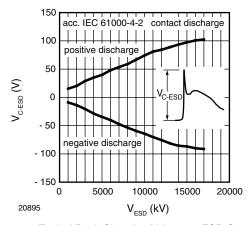
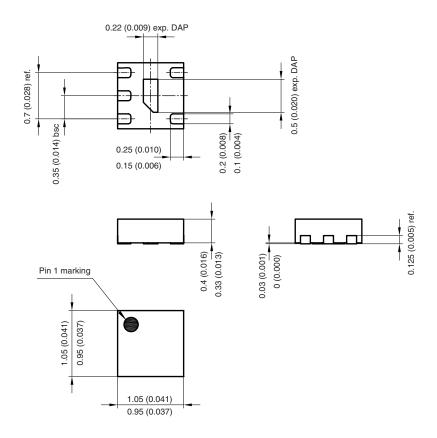
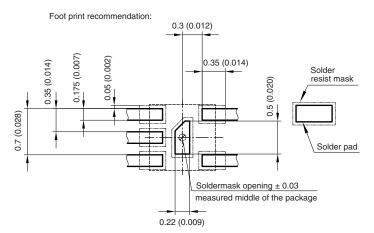


Figure 10. Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)



Package Dimensions in millimeters (inches): LLP1010-6L





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