

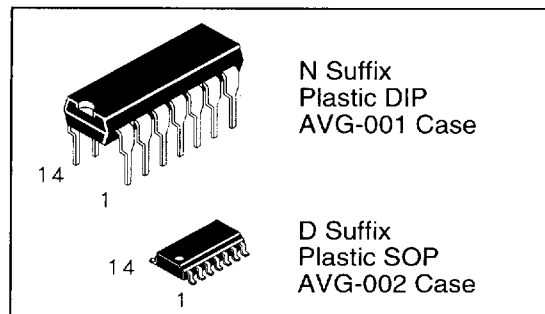
DV4069UB Available Q2, 1995

Quad 2-Input NOR (NAND) Gate Dual 4-Input NOR (NAND) Gate Triple 3-Input NOR (NAND) Gate Quad 2-Input OR (AND) Gate Hex Inverter Gate (unbuffered)

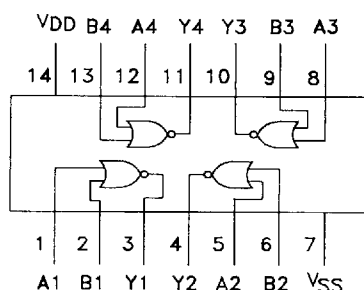
DV4001B (DV4011B)
DV4002B (DV4012B)
DV4025B (DV4023B)
DV4071B (DV4081B)
DV4069UB

These logic gates are constructed with P and N Channel devices in a single monolithic structure (Complementary MOS). They are used for low power dissipation and/or high noise immunity. The DV4069UB is an unbuffered device having slightly less gain but useful for certain applications such as oscillators.

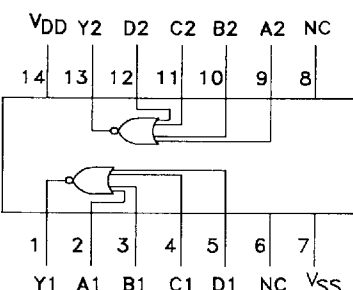
- Supply voltage range = 3.0 Vdc to 18 Vdc
- All outputs buffered
- Capable of driving 4 Low Power TTL loads or one LS TTL load over the rated temperature range
- Diode protection on all inputs
- Highest noise immunity at 12V supply



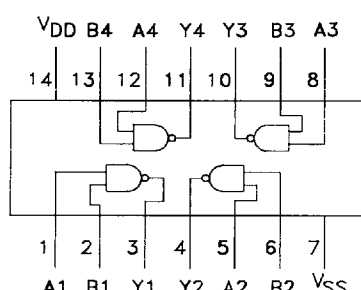
4001B



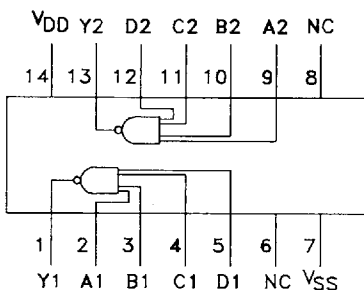
4002B



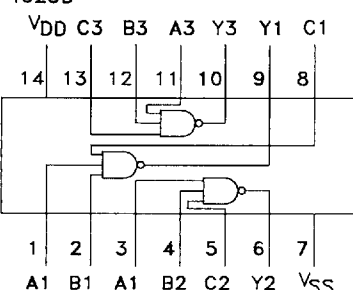
4011B



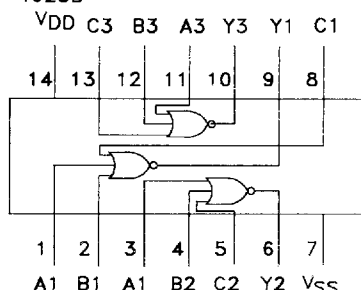
4012B



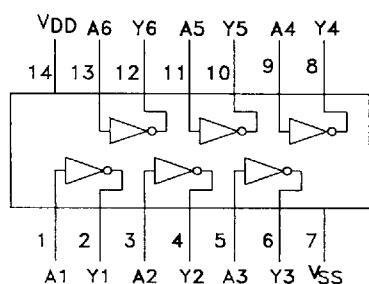
4023B



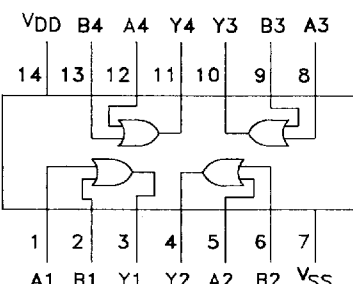
4025B



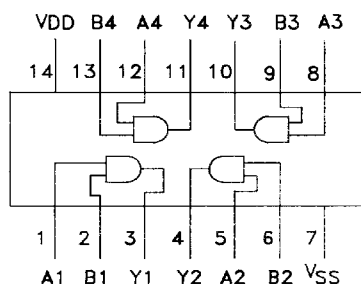
4069UB



4071B



4081B



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage (Referenced to V _{SS})	-0.5 to +18.0	V
V _{IN} , V _{OUT}	Input or Output Voltage	-0.5 to V _{DD} +0.5	V
I _{IN} , I _{OUT}	DC Current Into or Out of Any Pin	± 10	mA
P _D	Power Dissipation in Still Air, Derating: 12 mW/°C from 65° to 85°C	500	mW
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, (8 Second Soldering)	260	°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter		V _{DD}	Guaranteed Limits							Unit
				-40°C		25°C			85°C		
				Min	Max	Min	Typ	Max	Min	Max	
V _{OL}	Output Voltage V _{IN} =V _{DD} or 0	"0" Level	5.0	-	0.05	-	0	0.05	-	0.05	V _{dc}
			10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
V _{OH}	V _{IN} = 0 or V _{DD}	"1" Level	5.0	4.95	-	4.95	5.0	-	4.95	-	V _{dc}
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
V _{IL} Buffered Devices	Input Voltage (V _O =4.5 or 0.5 V _{dc}) (V _O =9.0 or 1.0 V _{dc}) (V _O =13.5 or 1.5 V _{dc})	"0" Level	5.0	-	1.5	-	2.25	1.5	-	1.5	V _{dc}
			10	-	3.0	-	4.50	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
V _{IL} Un- buffered Devices	DV4069UB only		5.0		1.0			1.0		1.0	V _{dc}
			10		2.0			2.0		2.0	
			15		2.5			2.5		2.5	
V _{IH} Buffered Devices	(V _O =0.5 or 4.5 V _{dc}) (V _O =1.0 or 9.0 V _{dc}) (V _O =1.5 or 13.5 V _{dc})	"1" Level	5.0	3.5	-	3.5	2.75	-	3.5	-	V _{dc}
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
V _{IH} Un- buffered Devices	DV4069UB only		5.0	4.0		.0			.0		
			10	8.0		8.0			8.0		
			15	12.5		12.5			12.5		
I _{OH}	Output Drive Current (V _{OH} = 2.5 V _{dc}) (V _{OH} = 4.6 V _{dc}) (V _{OH} = 9.5 V _{dc}) (V _{OH} = 13.5 V _{dc})	Source	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	mAdc
			5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
			10	-1.3	-	-1.1	-2.25	-	-0.9	-	
			15	-3.6	-	-3.0	-8.8	-	-2.4	-	
I _{OL}	(V _{OL} = 0.4 V _{dc}) (V _{OL} = 0.5 V _{dc}) (V _{OL} = 1.5 V _{dc})	Sink	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc
			10	1.3	-	1.1	2.25	-	0.9	-	
			15	3.6	-	3.0	8.8	-	2.4	-	
I _{IN}	Input Current		15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdc
C _{IN}	Input Capacitance	V _{IN} =0	-	-	-	-	5.0	7.5	-	-	pF
I _{DD}	Quiescent Current (Per Package)		5.0	-	1.0	-	0.0005	1.0	-	7.5	μAdc
			10	-	2.0	-	0.0010	2.0	-	15	
			15	-	4.0	-	0.0015	4.0	-	30	

SWITCHING CHARACTERISTICS ($C_L=50\text{ pF}, T_A=25^\circ\text{C}$)

Symbol	Characteristics	V_{DD}	Min	Typ	Max	Unit
t_{TLH}	Output Rise Time	5.0	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
t_{THL}	Output Fall Time	5.0	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
t_{PLH}, t_{PHL}	Propagation Delay Time 4001B, 4011B Only	5.0	-	125	250	ns
		10	-	50	100	
		15	-	40	80	
	All Other 2, 3, and 4 Input Gates	5.0	-	160	300	
		10	-	65	130	
		15	-	50	100	
	DV4069UB only	5.0		65	125	ns
		10		40	75	
		15		30	55	

SWITCHING WAVEFORMS