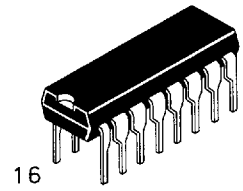
4-Bit Magnitude Comparator

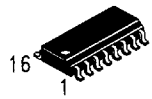
DV74HC85

This 4-Bit Magnitude Comparator compares two 4-bit nibbles and gives a high voltage level on either the $A>B_{out}$, $A=B_{out}$, or $A<B_{out}$ output, leaving the other two at a low voltage level. This device also has $A>B_{in}$, and $A<B_{in}$ inputs, eliminating the need for external gates when cascading

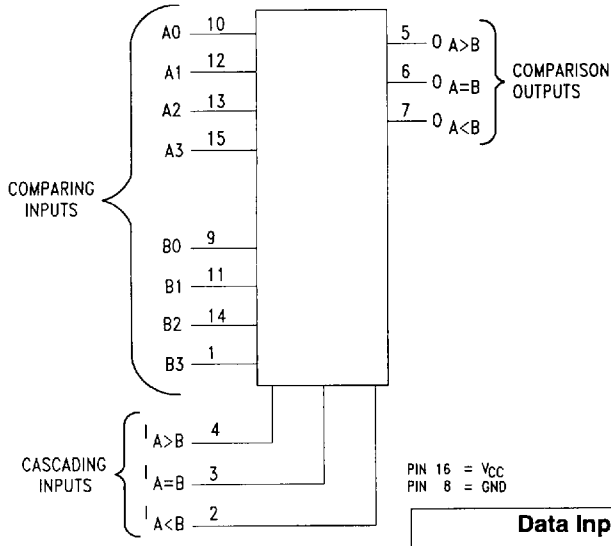
- **Output Drive Capability: 10 LSTTL Loads**
- **Outputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range: 2 to 6 V**
- **Low Input Current: 1 μA**
- **DC, AC parameters guaranteed from -55°C to 125°C**



N Suffix
Plastic DIP
AVG-003 Case

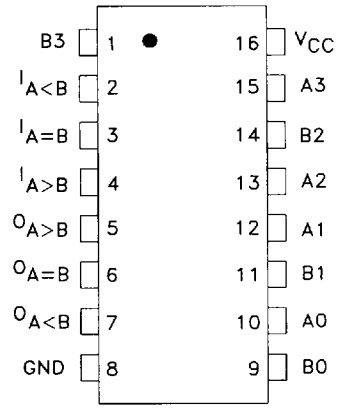


D Suffix
Plastic SOP
AVG-004 Case



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



TRUTH TABLE

Data Inputs				Cascading Inputs			Output		
A3,B3	**A2,B2**	**A1,B1**	**A0,B0**	**$A>B_{IN}$**	**$A=B_{IN}$**	**$A<B_{IN}$**	**A>B**	**$A=B_{OUT}$**	**$A<B_{OUT}$**
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	L	H
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	L	H
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	H	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	X	H	X	L	H	L

H = High Logic Level L = Low Logic Level X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP (SOP Package)	750	mW
T_{STG}	Storage Temperature Range	−65 to +150	°C
TL	Lead Temperature, 1mm from Case for 10 Seconds (Plastic DIP or SOP Package)	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Ambient Temperature		−55	+125	°C
t_r, t_f	Input Rise and Fall Ti	V_{CC}=2.0V V_{CC}=4.0V V_{CC}=6.0V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Vcc V	Guaranteed Limits 25°C to −55°C	Guaranteed Limits ≤85°C	Guaranteed Limits ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT} =0.1 V, $\|I_{OUT}\|\leq$ 20 µA or V_{OUT} = V_{CC}−0.1V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low- Level Input Voltage	V_{OUT} =0.1 V,$\|I_{OUT}\|$=20µA or V_{OUT} = V_{CC}−0.1V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|\leq$ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|\leq$ 4.0mA $\|I_{OUT}\|\leq$ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
VOL	Maximum Low Level Output Voltage	VIN = V_{IH} or V_{IL} $\|I_{OUT}\|\leq$ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|\leq$ 4.0mA $\|I_{OUT}\|\leq$ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, $\|I_{OUT}\|$= 0 µA	6.0	8.0	80	160	µA

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AC ELECTRICAL CHARACTERISTICS over full operating conditions (C_L=50pF, Input t_f=t_r=6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input A or B To Outputs A>B or A<B	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input A or B To Outputs A=B	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input A <B or A=B to Output A>B	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input A >B or A=B to Output A<B	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input A = B to Output A=B	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	—	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	**Typical @ 25°C, V_{CC} = 5 V** 50	pF

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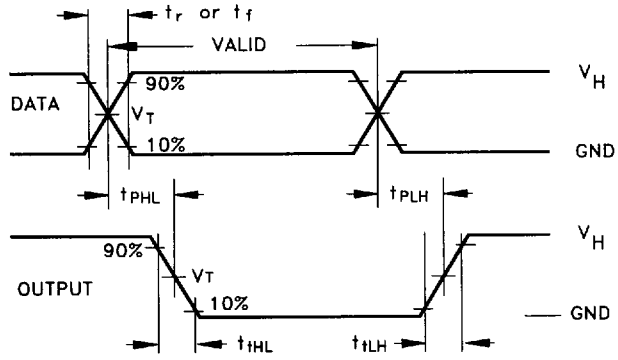
SWITCHING WAVEFORMS



Input and Output Threshold Voltage:
V_T = 50% V_{CC} for HC,1.3V for HCT,
V_H = V_{CC} for HC, 3V for HCT