

Available Q2, 1995

Octal 3-State Bus Transceivers and D-Type Flip-Flops

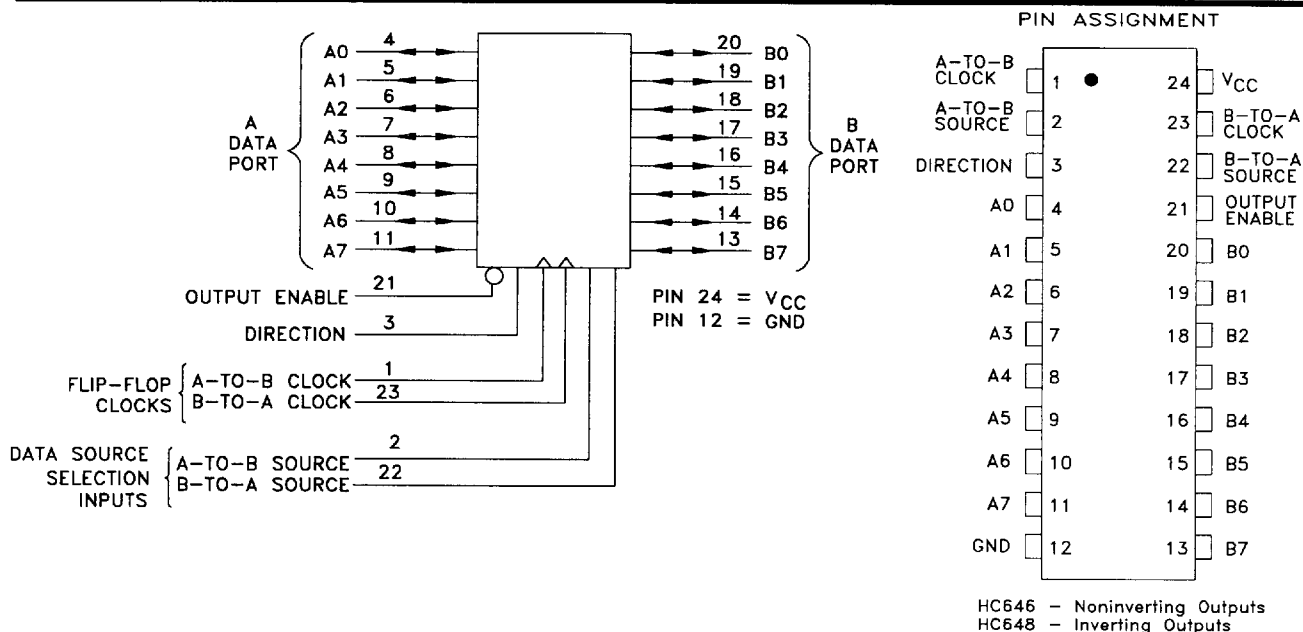
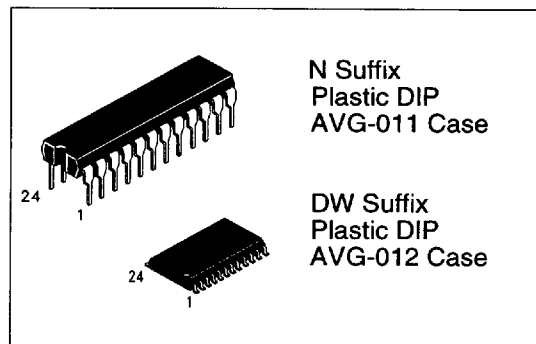
These devices are bus transceivers with D-type flip flops. Depending on the status of the Data-Source Selection pins, data may be routed to the outputs either from the flip-flops or transmitted in real time from inputs.

The Output Enable and the Direction pins control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip-flops simultaneously. Also, the A and B flip-flops can be routed as outputs to Bus A and Bus B simultaneously. Additionally, when either or both of the ports are in the high-impedance state, these I/O pins may be used as inputs to the D-type flip flops for data storage. Because the clocks are not gated with the Direction and Output Enable pins, data at the A and B ports may be clocked into the storage flip-flops at any time. The '646 has normal outputs, the '648 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V

- Low Input Current: 1 μ A
- DC, AC parameters guaranteed from -55°C to 125°C

DV74HC646, DV74HCT646
DV74HC648, DV74HCT648



646, 648

TRUTH TABLE

Output Enable	DIR	Clock CAB	Clock CBA	Source SAB	Source SBA	A0-A7	B0-B7	Operation or Function
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

H=HIGH Voltage Level

L=LOW Voltage Level

X=Either Low or High Logic Level

↑ = Low to High Transition

The data output functions may be enabled or disabled by various signals at the OE or DIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

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DV74HC646, DV74HC648

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ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	− 1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	± 20	mA
I _{OUT}	DC Output Sink/Source Current, per Pin	± 35	mA
I _{CC}	DC V _{CC} or GND Current Pin	± 75	mA
P _D	Power Dissipation in Still Air Plastic DIP SOP Package	750 500	mW
T _{stg}	Storage Temperature	− 65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage, (Ref. to GND)		0	V _{CC}	V
t _r , t _f	Input Rise and Fall Time	V _{CC} @ 2.0 to 6.0	100	100	ns
T _A	Operating Ambient Temperature Range		−55	+125	°C

HC – 646, 648

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	HC646, HC648 Guaranteed Limits			Unit
				25°C to −55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High Level Input Voltage	V _{OUT} = V _{CC} − 0.1 V I _{OUT} ≤ 20 μA	2.0	1.50	1.50	1.50	V
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V _{IL}	Maximum Low Level Input Voltage	V _{OUT} = 0.1 V I _{OUT} ≤ 20 μA	2.0	0.50	0.50	0.50	V
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} I _{OUT} ≤ 20 μA	2.0	1.90	1.90	1.90	V
			4.5	4.40	4.40	4.40	
			6.0	5.90	5.90	5.90	
		V _{IN} = V _{IH} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5	3.98	3.84	3.70	V
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IL} I _{OUT} ≤ 20 μA	2.0	0.10	0.10	0.10	V
			4.5	0.10	0.10	0.10	
			6.0	0.10	0.10	0.10	
		V _{IN} = V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5	0.26	0.33	0.40	V
			6.0	0.26	0.33	0.40	
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.00	±1.00	μA
I _{oz}	Maximum 3-State Current (Output in High Impedance State)	V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	mA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0	8	80	160	μA

AC CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6 ns)

Symbol	Parameter	Vcc (V)	Guaranteed Limits			Unit
			+25°C to -55°C	≤ 85°C	≤ 125° C	
fMAX	Maximum Clock Frequency (50% Duty Cycle)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay, Input A to Output B (or input B to Output A)	2.0 4.5 6.0	170 34 29	215 43 37	265 51 43	ns
tPLH, tPHL	Maximum Propagation Delay, A to B Clock to Output B (or B to A Clock to Output A)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
tPLH, tPHL	Maximum Propagation Delay, A to B Source to Output B (or B to A Source to Output A)	2.0 4.5 6.0	170 34 29	215 43 37	265 51 43	ns
tpZL, tpZH	Maximum Propagation Delay, Direction or Output Enable to Output A or B	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tPLZ, tPHZ	Maximum Propagation Delay Time, Direction or Output Disable to Output A or B	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
tTLH, tTHL	Maximum Output Transition Time, any Output	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
CIN	Maximum Input Capacitance	—	10	10	10	pF
COUT	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF
CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: PD = CPD VCC2f + ICC VCC	Typical @ 25°C, Vcc = 5.0 V				pF
		60				

TIMING REQUIREMENTS (CL = 50 pF, Input tr = tf = 6.0 ns)

Symbol	Parameter	Vcc (V)	Guaranteed Limits			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
tsu	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
th	Minimum Hold Time, Clock to Data	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
tw	Minimum Pulse Width, Clock	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns

HCT – 646, 648**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	V _{CC} (V)	HCT646,648			Unit
				TA = +25°C		TA = −40 to +85°C	
				Typ	Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage	V _{OUT} = 0.1V or V _{CC} − 0.1 V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low Level Input Voltage	V _{OUT} = 0.1V or V _{CC} − 0.1 V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V