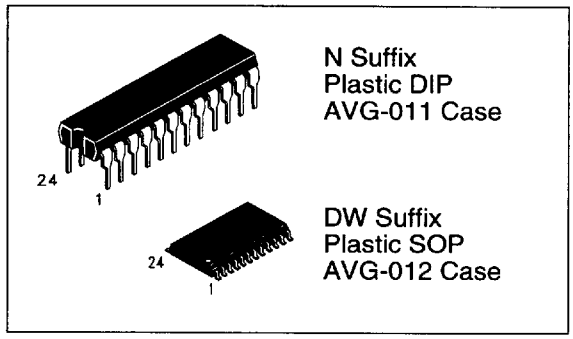
Available Q2, 1995

DV74HC651, DV74HC652
DV74HCT651, DV74HCT652

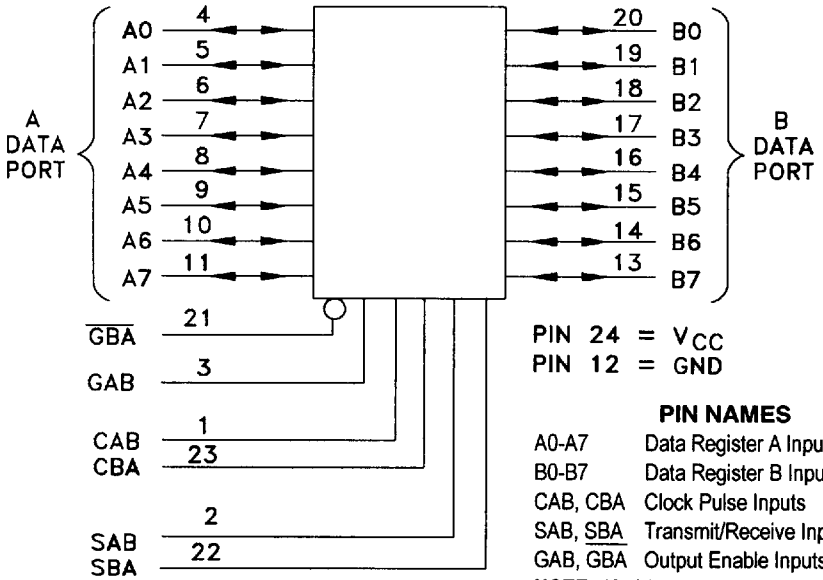
Octal Transceiver/Register with 3-State Outputs



This device is a high speed registered, bus transceiver circuit with outputs D-flip flops and control circuitry providing multiplexed transmission from the buses or from the internal regisaters. The 'HC/'HCT 651 has inverted outputs. The 'HC/'HCT 652 has normal outputs.

- **Output Drive Capability: 10 LSTTL Loads**
- **Ouputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range: 2 to 6 V**
- **Low Input Current: 1mA**
- **High Noise Immunity Characteristic of CMOS Devices**

651, 652

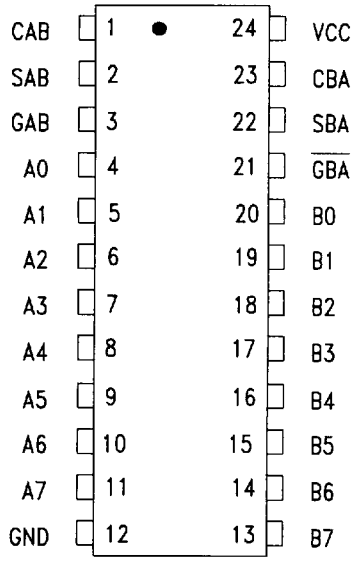


PIN 24 = V_{CC}
PIN 12 = GND

PIN NAMES

A0-A7	Data Register A Inputs/Outputs
B0-B7	Data Register B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, $\overline{SBA}$	Transmit/Receive Inputs
GAB, GBA	Output Enable Inputs

NOTE: '651 has inverted outputs



TRUTH TABLE

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A0-A7	B0-B7	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↑ ↑	H or L ↑	X X**	X X	Input Input	Unspecified* Output	Store A, Hold B Store A in Both Registers
L L	X L	H or L ↑	↑ ↑	X X	X X**	Unspecified* Output	Input Input	Hold A, Store B Store B in Both Registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H=HIGH Voltage Level L=LOW Voltage Level X=Don't Care ì=LOW-to-HIGH Transition

* The data output functions may be enabled or disabled by various signals at the GBA and GAB inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

** Select control=L:Clocks can occur simultaneously

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 35	mA
I_{CC}	DC V_{CC} or GND Current Pin	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP SOP Package	750 500	mW
Tstg	Storage Temperature	– 65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage, (Ref. to GND)		0	V_{CC}	V
t_r, t_f	Input Rise and Fall Time	V_{CC} @ 2.0 to 6.0	100	100	ns
T_A	Operating Ambient Temperature Range		–55	+125	°C

HC — 651, 652

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = V_{CC}–0.1 V $\|I_{OUT}\|$ ≤ 20 µA	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V $\|I_{OUT}\|$ ≤ 20 µA	2.0 4.5 6.0	0.50 1.35 1.80	0.50 1.35 1.80	0.50 1.35 1.80	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\|$ ≤ 20 µA	2.0 4.5 6.0	1.90 4.40 5.90	1.90 4.40 5.90	1.90 4.40 5.90	V
		V_{IN} = V_{IH} $\|I_{OUT}\|$ ≤ 6.0 mA $\|I_{OUT}\|$ ≤ 7.8 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.70 5.20	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\|$ ≤ 20 µA	2.0 4.5 6.0	0.10 0.10 0.10	0.10 0.10 0.10	0.10 0.10 0.10	V
		V_{IN} = V_{IL} $\|I_{OUT}\|$ ≤ 6.0 mA $\|I_{OUT}\|$ ≤ 7.8 mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.00	±1.00	µA
I_{OZ}	Maximum 3-State Current (Output in High Impedence State)	V_{IN}=V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	6.0	±0.5	±5.0	±10.0	mA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA	6.0	8	80	160	µA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter (C_L = 50 pF)	V_{CC} (V)	HC651, 652			Unit
			+25°C to −55°C	≤ 85°C	≤ 125° C	Unit
t_{PLH} t_{PHL}	Propagation Delay, CPBA or CPAB to An or B_n	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t_{PLH} t_{PHL}	Propagation Delay, A or B to Bn or A_n	2.0 4.5 6.0	180 36 31	225 45 38	270 54 46	ns
t_{PLH} t_{PHL}	Propagation Delay, SBA or SAB to An or B_n	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{PZH} t_{PHL}	Output Enable Time, $\overline{OEBA}$ to A_n	2.0 4.5 6.0	180 36 31	225 45 38	270 54 46	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{OEBA}$ to A_n	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
ts	Setup Time, HIGH or LOW An or Bn to CPBA or CPAB	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
th	Hold Time, HIGH or LOW An or Bn to CPBA or CPAB	2.0 4.5 6.0	25 5 5	30 6 5	40 8 7	ns
tw	CBAB, CPBA Pulse Width, HIGH or LOW	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns

C_{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consupmption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	**Typical @ 25°C, V_{CC} = 5.0 V** 60	pF

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

651, 652

HCT — 651, 652

DC ELECTRICAL CHARACTERISTICS

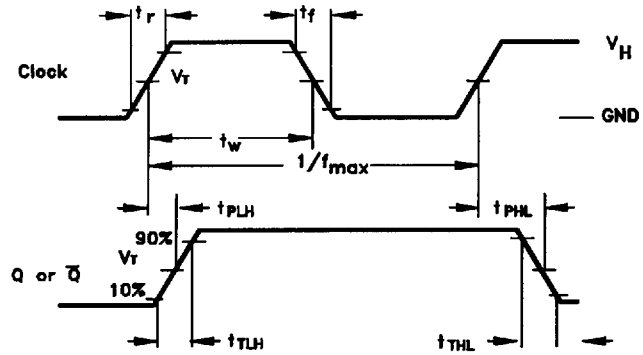
Symbol	Parameter	Conditions	V_{CC} (V)	HCT651,652			Unit
				TA = +25°C		TA = −40 to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC} − 0.1 V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC} − 0.1 V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = −50 µA	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V
		$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24mA −24 mA	4.5 5.5		3.86 4.86	3.76 4.76	V

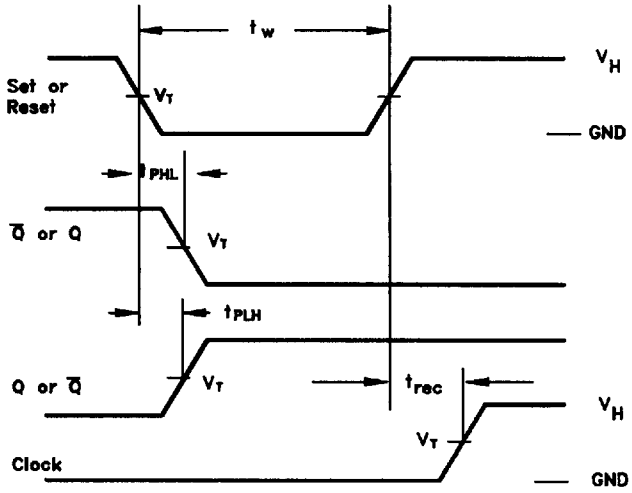
Symbol	Parameter	Conditions	Vcc (V)	HCT651,652			Unit
				TA = +25°C		TA = –40 to +85°C	
				Typ	Guaranteed Limits		
V_{OL}	Maximum Low Level Output Voltage	I_{OUT}= 50 µA	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V
		V_{IN} = V_{IL} or V_{IH} I_{OL} 24mA 24 mA	4.5 5.5		0.36 0.36	0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	V_I=V_{CC}, GND	5.5		±0.1	±1.0	µA
ΔI_{CCT}	Additional Max I_{CC}/Input	V_I=V_{CC} – 2.1 V	5.5	0.6		1.5	mA
I_{OZ}	Maximum 3-State Current	V_{OE} = VIH VI = V_{CC} or GND V = V_{CC} or GND	5.5		±0.6	±6.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		8.0	80	µA

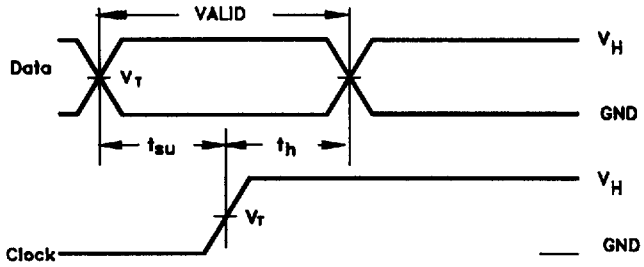
AC CHARACTERISTICS (CL = 50 pF, Input t_r = t_f = 6 ns)

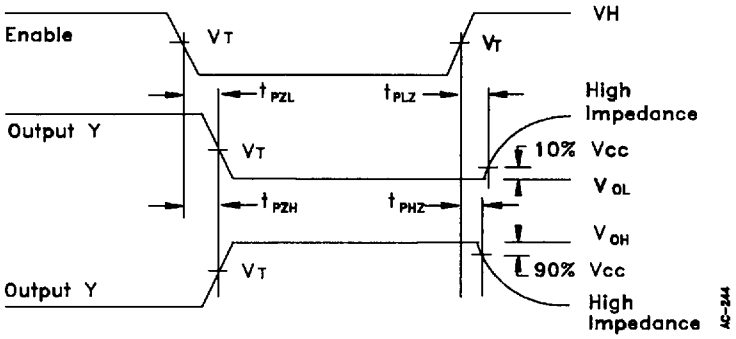
Symbol	Parameter (C_L = 50 pF)	Vcc (V)	HCT651, 652			Unit
			+25°C to –55°C	≤ 85°C	≤ 125° C	
t_{PLH} t_{PHL}	Propagation Delay, CPBA or CPAB to A_n or B_n	5.0	47	58	71	ns
t_{PLH} t_{PHL}	Propagation Delay, A or B to B_n or A_n	5.0	31	39	47	ns
t_{PLH} t_{PHL}	Propagation Delay, SBA or SAB to A_n or B_n	5.0	48	60	72	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OEBA}$ to A_n	5.0	30	38	45	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{OEBA}$ to A_n	5.0	38	48	57	ns
t_{PZH} t_{PZL}	Output Enable Time, OEAB to B_n	5.0	36	45	54	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OEAB to B_n	5.0	36	45	54	ns
ts	Setup Time, HIGH or LOW An or Bn to CPBA or CPAB	5.0	10	13	15	ns
th	Hold Time, HIGH or LOW An or Bn to CPBA or CPAB	5.0	5	5	5	ns
tw	CBAB, CPBA Pulse Width, HIGH or LOW	5.0	20	25	30	ns

SWITCHING WAVEFORMS

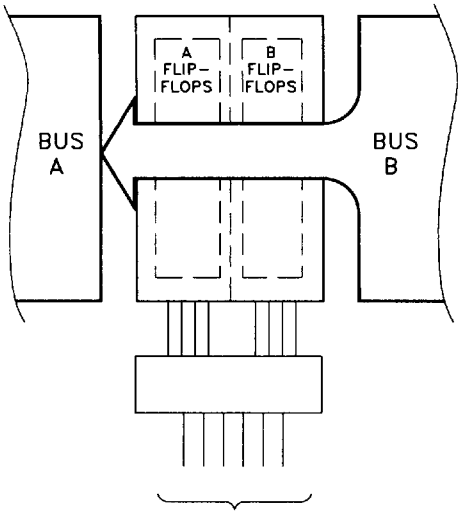






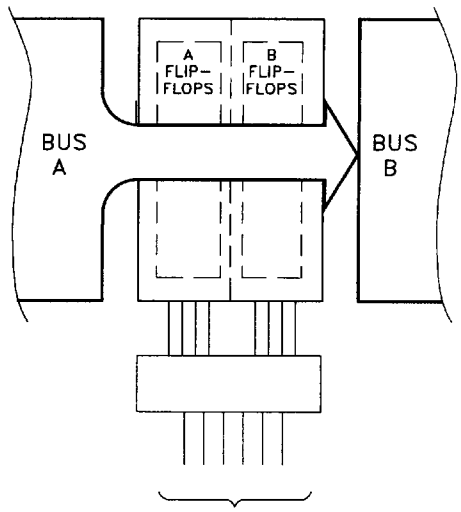


Input and output threshold voltage:
V_T = 50% V_{CC} for HC; 1.3V for HCT;
V_H = V_{CC} for HC, 3V for HCT



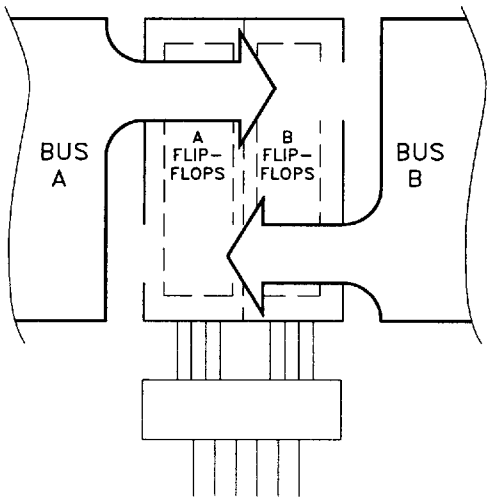
Real-Time Transfer
Bus B to Bus A

Real-Time Transfer Bus B to Bus A						
Pin #	**21**	**3**	**1**	**23**	**2**	**22**
Function	$\overline{GBA}$	GAB	CAB	CBA	SAB	SBA
Logic State	L	L	X	X	X	L



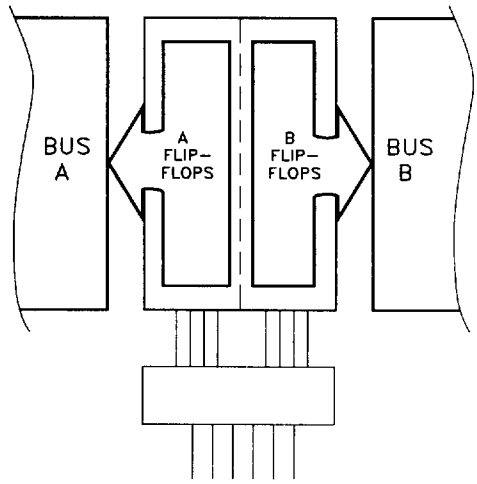
Real-Time Transfer
Bus A to Bus B

Real-Time Transfer Bus A to Bus B						
Pin #	**21**	**3**	**1**	**23**	**2**	**22**
Function	$\overline{GBA}$	GAB	CAB	CBA	SAB	SBA
Logic State	H	H	X	X	L	X



Storage From
A, B, or A and B

Storage From A, B or GAB						
Pin #	**21**	**3**	**1**	**23**	**2**	**22**
Function	$\overline{GBA}$	GAB	CAB	CBA	SAB	SBA
Logic State	L	H	↑	↑	X	X



Transfer Stored Data
To A or B

Transfer Stored Data to A or B						
Pin #	**21**	**3**	**1**	**23**	**2**	**22**
Function	$\overline{GBA}$	GAB	CAB	CBA	SAB	SBA
Logic State	L	H	X	X	H	H