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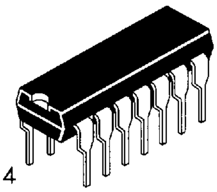
Dual JK Negative Edge-Triggered Flip-Flops with SET, common CLEAR and common CLOCK

DV74LS114A DV74ALS114A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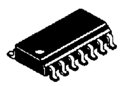
N Suffix
Plastic DIP
AVG-001 Case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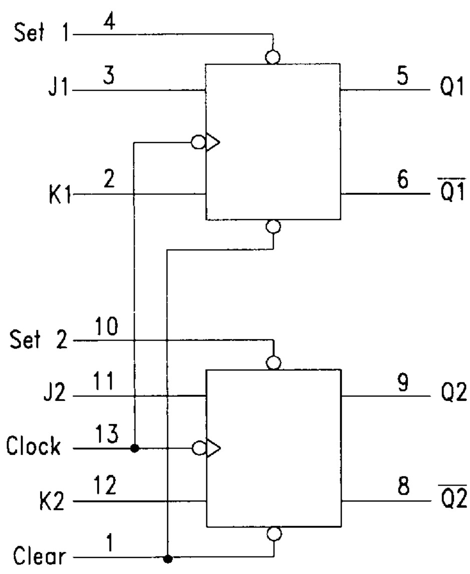
D Suffix
Plastic SOP
AVG-002 Case

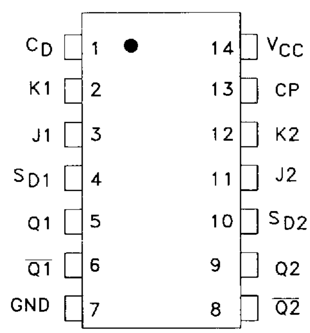
The circuity in this device contains common clock and common clear inputs. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the flip-flop will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative -going edge of the clock pulse.

- **AVG's LS operates over extended Vcc from 4.5 to 5.5 V**
- **AVG's LS and ALS both have guaranteed DC and AC specification over full temperature and Vcc range**
- **Switching specifications for ALS at 50 pF**
- **AVG's ALS has the lowest speed power product (4pJ per gate typical) of all logic series**



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



Note: Both outputs will be HIGH when both Set and Clear are LOW, but the output states are unpredictable if Set and Clear go HIGH simultaneously.

TRUTH TABLE

Inputs					Output	
Set	**Clear**	**Clock**	**J**	**K**	**Q**	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q_0	$\overline{Q_0}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q_0}$

H=HIGH Voltage Level
L=LOW Voltage Level
X=Immaterial

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	LS114A	ALS114A	Unit
V_{CC}	Supply Voltage	7.0	7.0	V
V_{IN}	Input Voltage	–0.5 to + 7.0	7.0	V
T_{STG}	Storage Temperature Range	–65 to +150	–65 to +150	°C

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GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	LS114A		ALS114A		Unit
		Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	2		2		V
V_{IL}	Low Level Input Voltage		0.8		0.8	V
I_{OH}	High Level Output Current		-0.4		-0.4	mA
I_{OL}	Low Level Output Current		8.0	0	8.0	mA
T_A	Operating Free Air Temperature Range	–10 to +70		–10 to +70		°C

Symbol	Parameter	Condition	LS114A			ALS114A			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC}= min, I_{IN} = -18 mA			-1.5			-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = min, I_{OH} =max	Vcc-2	3.5		Vcc-2			V
V_{OL}	Low Level Output Voltage	V_{CC}=min, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC}=min, I_{OL} = 8 mA		0.35	0.5		0.35	0.5	V
I_{IH}	High Level Input Current J, K Clock Set Clear	V_{CC}=max, V_{IN}= 2.7V			 20 160 60 120			 20 20 40 40	µA
	J, K Clock Set Clear	V_{CC}=max, V_{IN}= 7V			0.1 0.8 0.3 0.6			0.1 0.1 0.2 0.2	mA
I_{IL}	Low Level Input Current J, K Clock Clear Set	V_{CC}=max, V_{IN}=0.4V			 -0.4 -1.6 -1.6 -0.8			 -0.2 -0.2 -0.4 -0.4	mA
I_O	Output Short Circuit Current	VCC=max, V_{OUT} =2.25V	–20		–110	–30		–112	mA
I_{CC}	Power Supply Current	V_{CC}=max			6.0		2.5	4.5	mA

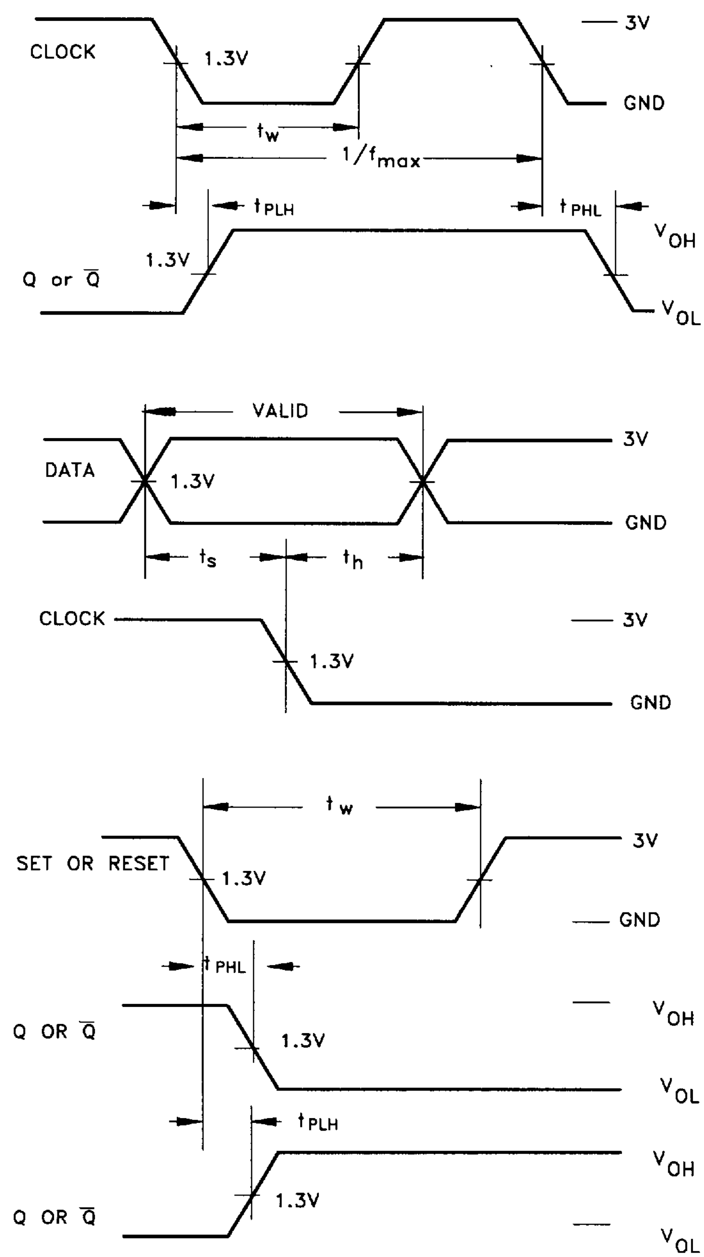
SWITCHING CHARACTERISTICS

Symbol	Parameter	INPUT	OUTPUT	LS114A C_L=15 pF		ALS114A C_L=50pF R_L=500Ω		Unit
				Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency			30		30		MHz
t_{PLH}	Propogation Delay Time Low-to-High Level Output	Clock	Any Q		20	3	15	ns
t_{PHL}	Propogation Delay Time High-to-Low Level Output	Clock	Any Q		20	5	19	ns
t_{PLH}	Propogation Delay Time Low-to-High Level Output	Set or Clear	Any Q		20	3	15	ns
t_{PHL}	Propogation Delay Time High-to-Low Level Output	Set or Clear	Any Q		20	4	18	ns

AC SETUP REQUIREMENTS

Symbol	Parameter		Limits				Unit
			LS114A		ALS 114A		
			MIN	MAX	MIN	MAX	
t_W	Pulse Width	Set or Reset Low Clock High Clock Low	25 20 20		10 16.5 16.5		ns
t_S	Setup Time	Data Set or Reset	20		22 20		ns
t_h	Hold Time		0		0		ns

SWITCHING WAVEFORMS



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