



5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

MAX6316-MAX6322

General Description

The MAX6316-MAX6322 family of microprocessor (μ P) supervisory circuits monitors power supplies and microprocessor activity in digital systems. It offers several combinations of push/pull, open-drain, and bidirectional (such as Motorola 68HC11) reset outputs, along with watchdog and manual reset features. The *Selector Guide* below lists the specific functions available from each device. These devices are specifically designed to ignore fast negative transients on VCC. Resets are guaranteed valid for VCC down to 1V.

These devices are available in 26 factory-trimmed reset threshold voltages (from 2.5V to 5V, in 100mV increments), featuring four minimum power-on reset timeout periods (from 1ms to 1.12s), and four watchdog timeout periods (from 6.3ms to 25.6s). Thirteen standard versions are available with an order increment requirement of 2500 pieces (see *Standard Versions* table); contact the factory for availability of other versions, which have an order increment requirement of 10,000 pieces.

The MAX6316-MAX6322 are offered in a miniature 5-pin SOT23 package.

Applications

Portable Computers
Computers
Controllers
Intelligent Instruments
Portable/Battery-Powered Equipment
Embedded Control Systems

Features

- ◆ Small 5-Pin SOT23 Package
- ◆ Available in 26 Reset Threshold Voltages
2.5V to 5V, in 100mV Increments
- ◆ Four Reset Timeout Periods
1ms, 20ms, 140ms, or 1.12s (min)
- ◆ Four Watchdog Timeout Periods
6.3ms, 102ms, 1.6s, or 25.6s (typ)
- ◆ Four Reset Output Stages
Active-High, Push/Pull
Active-Low, Push/Pull
Active-Low, Open-Drain
Active-Low, Bidirectional
- ◆ Guaranteed Reset Valid to VCC = 1V
- ◆ Immune to Short Negative VCC Transients
- ◆ Low Cost
- ◆ No External Components

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX6316LUK____-T	-40°C to +85°C	5 SOT23-5
MAX6316MUK____-T	-40°C to +85°C	5 SOT23-5
MAX6317HUK____-T	-40°C to +85°C	5 SOT23-5
MAX6318HUK____-T	-40°C to +85°C	5 SOT23-5
MAX6318MHUK____-T	-40°C to +85°C	5 SOT23-5

Ordering Information continued at end of data sheet.

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

Selector Guide

PART	WATCHDOG INPUT	MANUAL RESET INPUT	RESET OUTPUTS*			
			ACTIVE-LOW PUSH/PULL	ACTIVE-HIGH PUSH/PULL	ACTIVE-LOW BIDIRECTIONAL	ACTIVE-LOW OPEN-DRAIN
MAX6316L	✓	✓	✓	—	—	—
MAX6316M	✓	✓	—	—	✓	—
MAX6317H	✓	✓	—	✓	—	—
MAX6318LH	✓	—	✓	✓	—	—
MAX6318MH	✓	—	—	✓	✓	—
MAX6319LH	—	✓	✓	✓	—	—
MAX6319MH	—	✓	—	✓	✓	—
MAX6320P	✓	✓	—	—	—	✓
MAX6321HP	✓	—	—	✓	—	✓
MAX6322HP	—	✓	—	✓	—	✓

* The MAX6318/MAX6319/MAX6321/MAX6322 feature two types of reset output on each device.



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ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)

V_{CC}.....-0.3V to +6V
 RESET (MAX6320/MAX6321/MAX6322 only)..... -0.3V to +6V
 All Other Pins.....-0.3V to (V_{CC} + 0.3V)
 Input/Output Current, All Pins20mA

Continuous Power Dissipation (T_A = +70°C)

SOT23-5 (derate 7.1mW/°C above +70°C).....571mW
 Operating Temperature Range.....-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range.....-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	T _A = -40°C to +85°C	1		5.5	V
Supply Current	I _{CC}	MAX6316/MAX6317/MAX6318/ MAX6320/MAX6321: MR and WDI unconnected	V _{CC} = 5.5V	10	20	μ A
			V _{CC} = 3.6V	5	12	
		MAX6319/MAX6322: MR unconnected	V _{CC} = 5.5V	5	12	
			V _{CC} = 3.6V	3	8	
Reset Threshold Temperature Coefficient	$\Delta V_{TH}/^{\circ}\text{C}$			40		ppm/°C
Reset Threshold (Note 2)	V _{RST}	T _A = +25°C	V _{TH} - 1.5%	V _{TH}	V _{TH} + 1.5%	V
		T _A = -40°C to +85°C	V _{TH} - 2.5%	V _{TH}	V _{TH} + 2.5%	
Reset Threshold Hysteresis				3		mV
Reset Active Timeout Period	t _{RP}	MAX63_ _A_-T	1	1.4	2	ms
		MAX63_ _B_-T	20	28	40	
		MAX63_ _C_-T	140	200	280	
		MAX63_ _D_-T	1120	1600	2240	
V _{CC} to RESET Delay	t _{RD}	V _{CC} falling at 1mV/ μ s		40		μ s
PUSH/PULL RESET OUTPUT (MAX6316L/MAX6317H/MAX6318_H/MAX6319_H/MAX6321HP/MAX6322HP)						
RESET Output Voltage	V _{OL}	V _{CC} $\geq$ 1.0V, I _{SINK} = 50 μ A			0.3	V
		V _{CC} $\geq$ 1.2V, I _{SINK} = 100 μ A			0.3	
		V _{CC} $\geq$ 2.7V, I _{SINK} = 1.2mA			0.3	
		V _{CC} $\geq$ 4.5V, I _{SINK} = 3.2mA			0.4	
	V _{OH}	V _{CC} $\geq$ 2.7V, I _{SOURCE} = 500 μ A	0.8 x V _{CC}			
		V _{CC} $\geq$ 4.5V, I _{SOURCE} = 800 μ A	V _{CC} - 1.5			
RESET Output Voltage	V _{OL}	V _{CC} $\geq$ 2.7V, I _{SINK} = 1.2mA			0.3	V
		V _{CC} $\geq$ 4.5V, I _{SINK} = 3.2mA			0.4	
	V _{OH}	V _{CC} $\geq$ 1.8V, I _{SOURCE} = 150 μ A	0.8 x V _{CC}			
		V _{CC} $\geq$ 2.7V, I _{SOURCE} = 500 μ A	0.8 x V _{CC}			
		V _{CC} $\geq$ 4.5V, I _{SOURCE} = 800 μ A	V _{CC} - 1.5			

Note 1: Over-temperature limits are guaranteed by design, not production tested.

Note 2: A factory-trimmed voltage divider programs the nominal reset threshold (V_{TH}). Factory-trimmed reset thresholds are available in 100mV increments from 2.5V to 5V (see Table 1 at end of data sheet).

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

MAX6316-MAX6322

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 2.5V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIDIRECTIONAL RESET OUTPUT (MAX6316M/MAX6318MH/MAX6319MH)						
Transition Flip-Flop Setup Time	t _S	(Note 3)	400			ns
RESET Output Rise Time (Note 4)	t _R	V _{CC} = 3.0V, C _L = 120pF	333			ns
		V _{CC} = 5.0V, C _L = 200pF	333			
		V _{CC} = 3.0V, C _L = 250pF	666			
		V _{CC} = 5.0V, C _L = 400pF	666			
Active Pullup Enable Threshold	V _{PTH}	V _{CC} = 5.0V	0.4	0.65		V
RESET Active Pullup Current		V _{CC} = 5.0V	20			mA
RESET Pullup Resistance			4.2	4.7	5.2	kΩ
OPEN-DRAIN RESET OUTPUT (MAX6320P/MAX6321HP/MAX6322HP)						
RESET Output Voltage	V _{OL}	V _{CC} ≥ 1.0V, I _{SINK} = 50μA	0.3			V
		V _{CC} ≥ 1.2V, I _{SINK} = 100μA	0.3			
		V _{CC} ≥ 2.7V, I _{SINK} = 1.2mA	0.3			
		V _{CC} ≥ 4.5V, I _{SINK} = 3.2mA	0.4			
Open-Drain Reset Output Leakage Current	I _{LKG}		1.0			μA
WATCHDOG INPUT (MAX6316/MAX6317H/MAX6318_H/MAX6320P/MAX6321HP)						
Watchdog Timeout Period	t _{WD}	MAX63_ _ _ W-T	4.3	6.3	9.3	ms
		MAX63_ _ _ X-T	71	102	153	
		MAX63_ _ _ Y-T	1.12	1.6	2.4	s
		MAX63_ _ _ Z-T	17.9	25.6	38.4	
WDI Pulse Width	t _{WDI}	V _{IL} = 0.3 x V _{CC} , V _{IH} = 0.7 x V _{CC}	50			ns
WDI Input Threshold	V _{IL}	(Note 5)	0.3 x V _{CC}			V
	V _{IH}		0.7 x V _{CC}			
WDI Input Current (Note 6)	I _{WDI}	WDI = V _{CC} , time average	120 160			μA
		V _{WDI} = 0, time average	-20 -15			
MANUAL RESET INPUT (MAX6316_/MAX6317H/MAX6319_H/MAX6320P/MAX6322HP)						
MR Input Threshold	V _{IL}	V _{TH} > 4.0V	0.8			V
	V _{IH}		2.0			
	V _{IL}	V _{TH} < 4.0V	0.3 x V _{CC}			
	V _{IH}		0.7 x V _{CC}			
MR Input Pulse Width			1			μs
MR Glitch Rejection			100			ns
MR Pullup Resistance			35	52	75	kΩ
MR to Reset Delay		V _{CC} = 5V	230			ns

Note 3: This is the minimum time RESET must be held low by an external pulldown source to set the active pullup flip-flop.

Note 4: Measured from RESET V_{OL} to $(0.8 \times V_{CC})$, $R_{LOAD} = \infty$.

Note 5: WDI is internally serviced within the watchdog period if WDI is left unconnected.

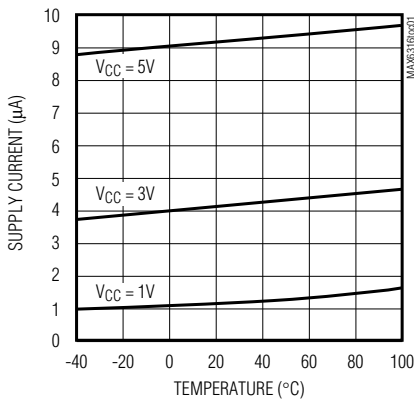
Note 6: The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed for a three-stated-output device with a $10\mu A$ maximum leakage current and capable of driving a maximum capacitive load of $200pF$. The three-state device must be able to source and sink at least $200\mu A$ when active.

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

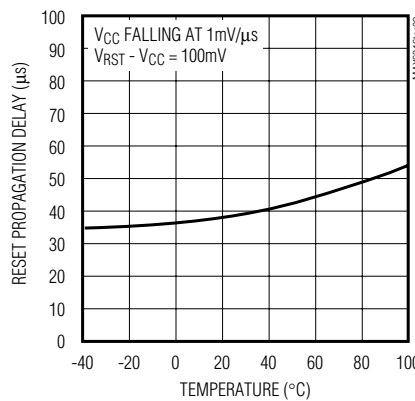
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

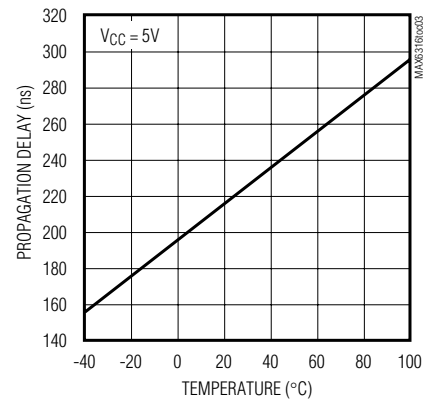
MAX6316/MAX6317/MAX6318/MAX6320/MAX6321
SUPPLY CURRENT vs. TEMPERATURE



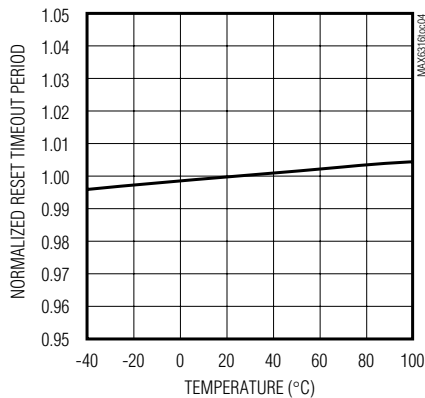
V_{CC} FALLING TO RESET PROPAGATION DELAY vs. TEMPERATURE



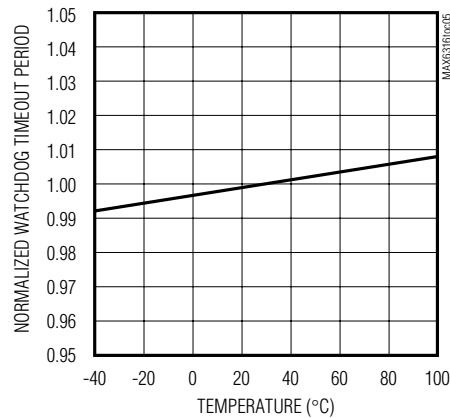
MAX6316/MAX6317/MAX6319/MAX6320/MAX6322
MANUAL RESET TO RESET PROPAGATION DELAY vs. TEMPERATURE



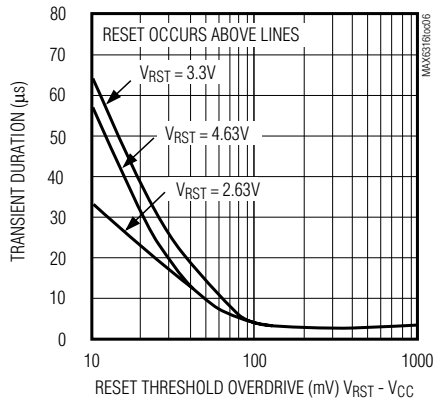
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



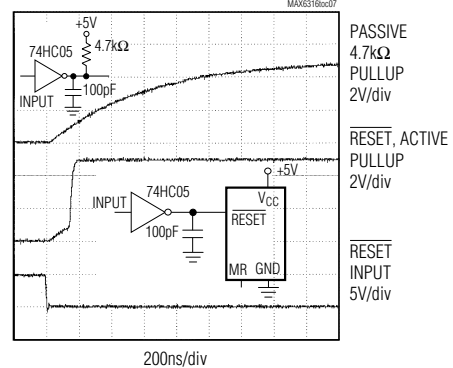
MAX6316/MAX6317/MAX6318/MAX6320/MAX6321
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



MAX6316M/6318MH/6319MH
BIDIRECTIONAL PULLUP CHARACTERISTICS



5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

Pin Description

MAX6316-MAX6322

PIN				NAME	FUNCTION
MAX6316L MAX6316M MAX6320P	MAX6317H	MAX6318LH MAX6318MH MAX6321HP	MAX6319LH MAX6319MH MAX6322HP		
1	—	1	1	RESET	MAX6316L/MAX6318LH/MAX6319LH: Active-Low, Reset Output. CMOS push/pull output (sources and sinks current). MAX6316M/MAX6318MH/MAX6319MH: Bidirectional, Active-Low, Reset Output. Intended to interface directly to microprocessors with bidirectional resets such as the Motorola 68HC11. MAX6320P/MAX6321HP/MAX6322HP: Open-Drain, Active-Low, Reset Output. NMOS output (sinks current only). Connect a pullup resistor from RESET to any supply voltage up to 6V.
—	1	3	3	RESET	Active-High, Reset Output. CMOS push/pull output (sources and sinks current). Inverse of RESET.
2	2	2	2	GND	Ground
3	3	—	4	MR	Active-Low, Manual Reset Input. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after MR transitions from low to high. Leave unconnected or connected to VCC if not used.
4	4	4	—	WDI	Watchdog Input. Triggers a reset if it remains either high or low for the duration of the watchdog timeout period. The internal watchdog timer clears whenever a reset asserts or whenever WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.
5	5	5	5	VCC	Supply Voltage. Reset is asserted when VCC drops below the Reset Threshold Voltage (VRST). Reset remains asserted until VCC rises above VRST and for the duration of the Reset Timeout Period (tRP) once VCC rises above VRST.

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

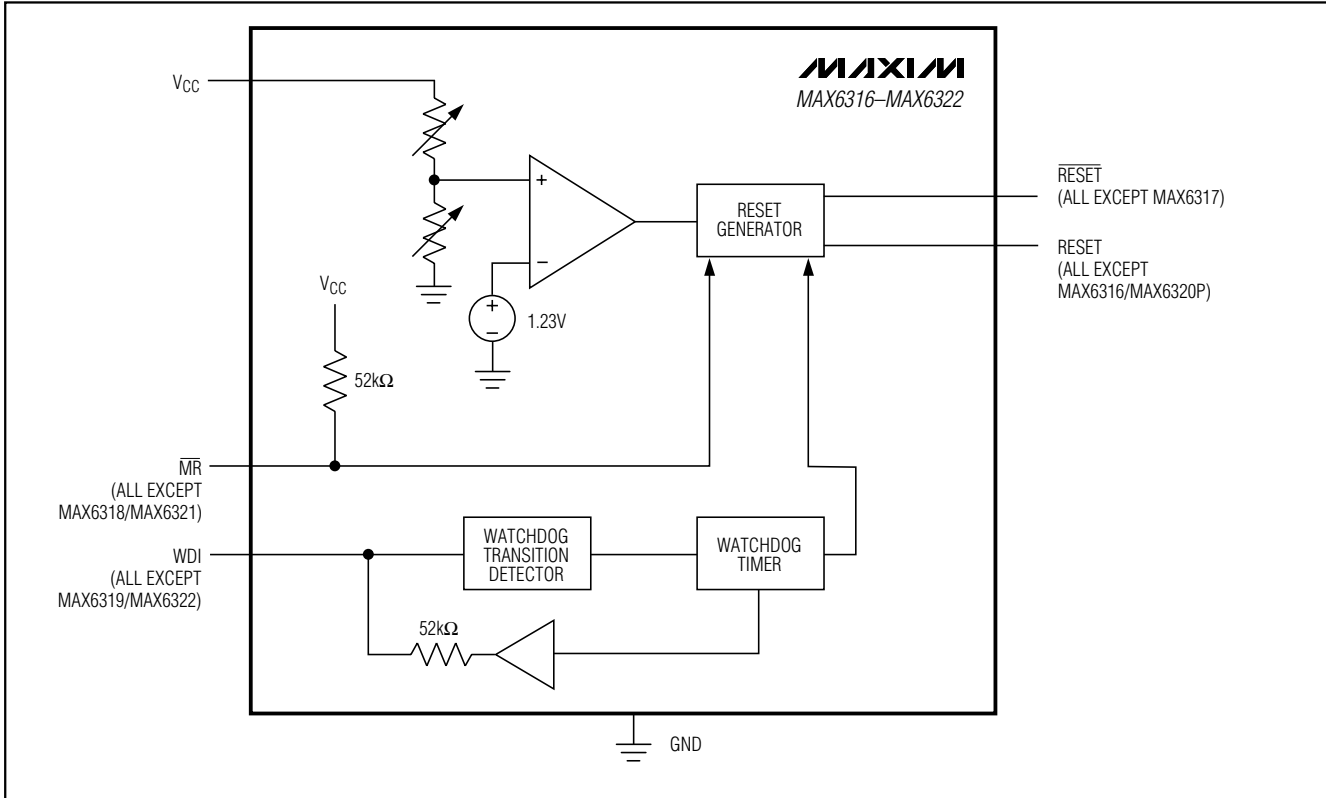


Figure 1. Functional Diagram

Detailed Description

A microprocessor's (μ P) reset input starts or restarts the μ P in a known state. The reset output of the MAX6316-MAX6322 μ P supervisory circuits interfaces with the reset input of the μ P, preventing code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Operating Circuit*). The MAX6316/MAX6317/MAX6318/MAX6320/MAX6321 are also capable of asserting a reset should the μ P become stuck in an infinite loop.

Reset Output

The MAX6316L/MAX6318LH/MAX6319LH feature an active-low reset output, while the MAX6317H/MAX6318_H/MAX6319_H/MAX6321HP/MAX6322HP feature an active-high reset output. $\overline{\text{RESET}}$ is guaranteed to be a logic low and RESET is guaranteed to be a logic high for V_{CC} down to 1V.

The MAX6316-MAX6322 assert reset when V_{CC} is below the reset threshold (V_{RST}), when $\overline{\text{MR}}$ is pulled low (MAX6316_/MAX6317H/MAX6319_H/MAX6320P/MAX6322HP only), or if the WDI pin is not serviced within

the watchdog timeout period (t_{WD}). Reset remains asserted for the specified reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{\text{MR}}$ transitions low to high, or after the watchdog timer asserts the reset (MAX6316_/MAX6317H/MAX6318_H/MAX6320P/MAX6321HP). After the reset active timeout period (t_{RP}) expires, the reset output deasserts, and the watchdog timer restarts from zero (Figure 2).

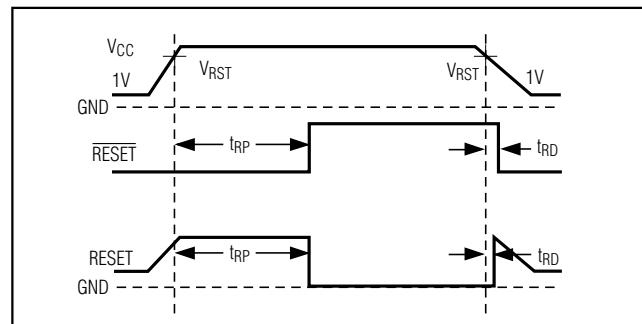


Figure 2. Reset Timing Diagram

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

Bidirectional $\overline{\text{RESET}}$ Output

The MAX6316M/MAX6318MH/MAX6319MH are designed to interface with μ Ps that have bidirectional reset pins, such as the Motorola 68HC11. Like an open-drain output, these devices allow the μ P or other devices to pull the bidirectional reset ($\overline{\text{RESET}}$) low and assert a reset condition. However, unlike a standard open-drain output, it includes the commonly specified 4.7k Ω pullup resistor with a P-channel active pullup in parallel.

This configuration allows the MAX6316M/MAX6318MH/MAX6319MH to solve a problem associated with μ Ps that have bidirectional reset pins in systems where several devices connect to $\overline{\text{RESET}}$ (Figure 3). These μ Ps can often determine if a reset was asserted by an external device (i.e., the supervisor IC) or by the μ P itself (due to a watchdog fault, clock error, or other source), and then jump to a vector appropriate for the source of the reset. However, if the μ P does assert reset, it does not retain the information, but must determine the cause after the reset has occurred.

The following procedure describes how this is done in the Motorola 68HC11. In all cases of reset, the μ P pulls $\overline{\text{RESET}}$ low for about four external-clock cycles. It then releases $\overline{\text{RESET}}$, waits for two external-clock cycles, then checks $\overline{\text{RESET}}$'s state. If $\overline{\text{RESET}}$ is still low, the μ P concludes that the source of the reset was external and, when $\overline{\text{RESET}}$ eventually reaches the high state, it jumps to the normal reset vector. In this case, stored-state information is erased and processing begins from

scratch. If, on the other hand, $\overline{\text{RESET}}$ is high after a delay of two external-clock cycles, the processor knows that it caused the reset itself and can jump to a different vector and use stored-state information to determine what caused the reset.

A problem occurs with faster μ Ps; two external-clock cycles are only 500ns at 4MHz. When there are several devices on the reset line, and only a passive pullup resistor is used, the input capacitance and stray capacitance can prevent $\overline{\text{RESET}}$ from reaching the logic high state ($0.8 \times V_{CC}$) in the time allowed. If this happens, all resets will be interpreted as external. The μ P output stage is guaranteed to sink 1.6mA, so the rise time can not be reduced considerably by decreasing the 4.7k Ω internal pullup resistance. See Bidirectional Pullup Characteristics in the *Typical Operating Characteristics*.

The MAX6316M/MAX6318MH/MAX6319MH overcome this problem with an active pullup FET in parallel with the 4.7k Ω resistor (Figures 4 and 5). The pullup transistor holds $\overline{\text{RESET}}$ high until the μ P reset I/O or the supervisory circuit itself forces the line low. Once $\overline{\text{RESET}}$ goes below V_{PTH} , a comparator sets the transition edge flip-flop, indicating that the next transition for $\overline{\text{RESET}}$ will be low to high. When $\overline{\text{RESET}}$ is released, the 4.7k Ω resistor pulls $\overline{\text{RESET}}$ up toward V_{CC} . Once $\overline{\text{RESET}}$ rises above V_{PTH} but is below ($0.85 \times V_{CC}$), the active P-channel pullup turns on. Once $\overline{\text{RESET}}$ rises above ($0.85 \times V_{CC}$) or the 2 μ s one-shot times out, the active pullup turns off. The parallel combination of the 4.7k Ω pullup and the

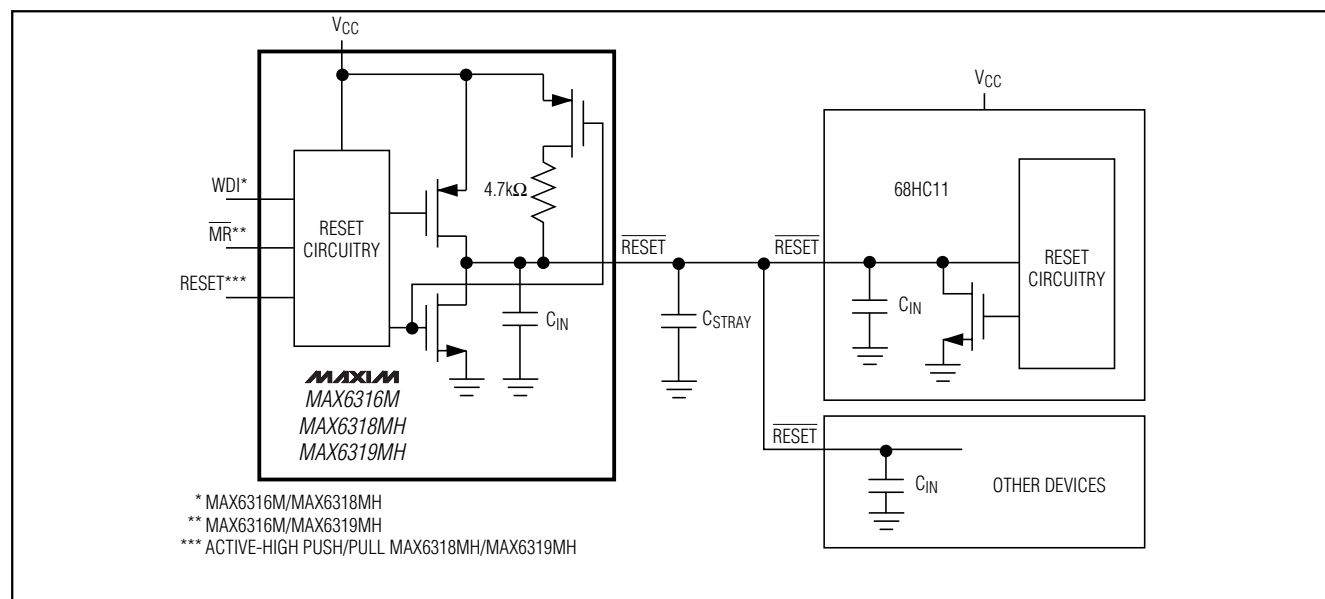


Figure 3. MAX6316M/MAX6318MH/MAX6319MH Supports Additional Devices on the Reset Bus

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

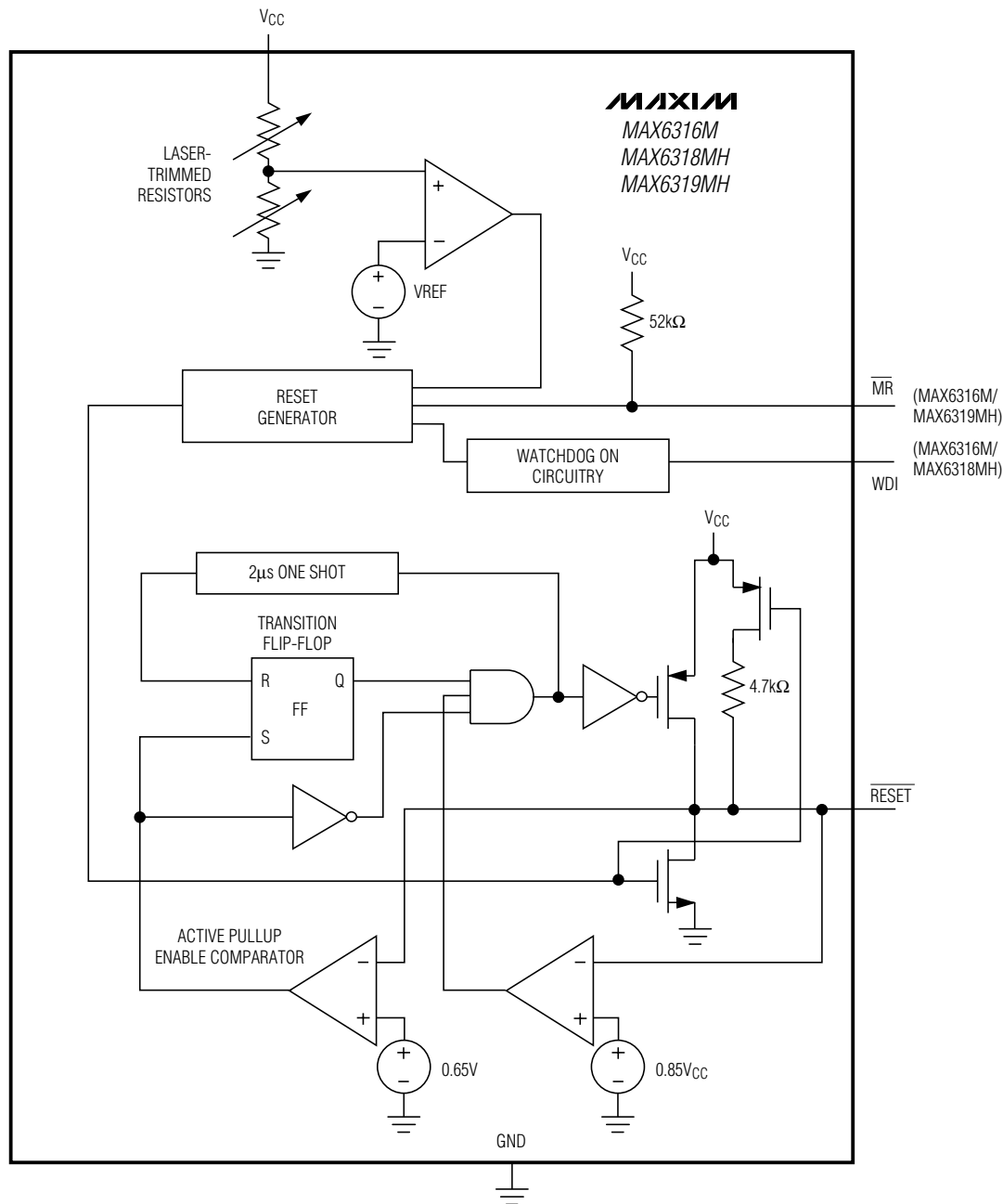


Figure 4. MAX6316/MAX6318MH/MAX6319MH Bidirectional Reset Output Functional Diagram

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

P-channel transistor on-resistance quickly charges stray capacitance on the reset line, allowing $\overline{\text{RESET}}$ to transition from low to high within the required two electronic-clock cycles, even with several devices on the reset line. This process occurs regardless of whether the reset was caused by V_{CC} dipping below the reset threshold, the watchdog timing out, $\overline{\text{MR}}$ being asserted, or the μ P or other device asserting $\overline{\text{RESET}}$. The parts do not require an external pullup. To minimize supply current consumption, the internal $4.7\text{k}\Omega$ pullup resistor disconnects from the supply whenever the MAX6316M/MAX6318MH/MAX6319MH assert reset.

Open-Drain $\overline{\text{RESET}}$ Output

The MAX6320P/MAX6321HP/MAX6322HP have an active-low, open-drain reset output. This output structure will sink current when $\overline{\text{RESET}}$ is asserted. Connect a pullup resistor from $\overline{\text{RESET}}$ to any supply voltage up to 6V (Figure 6). Select a resistor value large enough to

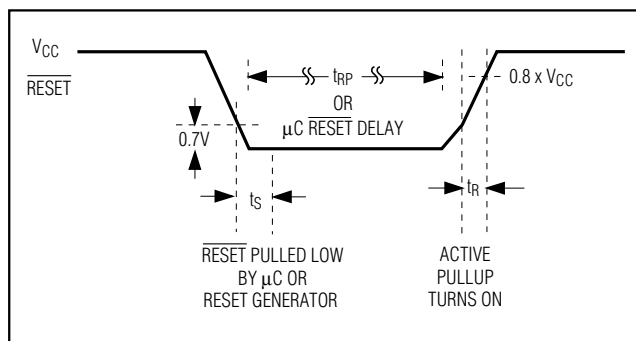


Figure 5. Bidirectional $\overline{\text{RESET}}$ Timing Diagram

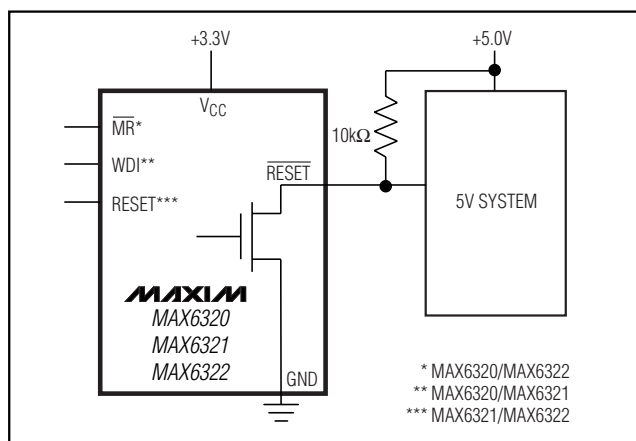


Figure 6. MAX6320P/MAX6321HP/MAX6322HP Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

register a logic low (see *Electrical Characteristics*), and small enough to register a logic high while supplying all input current and leakage paths connected to the $\overline{\text{RESET}}$ line. A $10\text{k}\Omega$ pullup is sufficient in most applications.

Manual-Reset Input

The MAX6316_/MAX6317H/MAX6319_H/MAX6320P/MAX6322HP feature a manual reset input. A logic low on $\overline{\text{MR}}$ asserts a reset. After $\overline{\text{MR}}$ transitions low to high, reset remains asserted for the duration of the reset timeout period (t_{RP}). The $\overline{\text{MR}}$ input is connected to V_{CC} through an internal $52\text{k}\Omega$ pullup resistor and therefore can be left unconnected when not in use. $\overline{\text{MR}}$ can be driven with TTL-logic levels in 5V systems, with CMOS-logic levels in 3V systems, or with open-drain or open-collector output devices. A normally-open momentary switch from $\overline{\text{MR}}$ to ground can also be used; it requires no external debouncing circuitry. $\overline{\text{MR}}$ is designed to reject fast, negative-going transients (typically 100ns pulses). A $0.1\mu\text{F}$ capacitor from $\overline{\text{MR}}$ to ground provides additional noise immunity.

The $\overline{\text{MR}}$ input pin is equipped with internal ESD-protection circuitry that may become forward biased. Should $\overline{\text{MR}}$ be driven by voltages higher than V_{CC} , excessive current would be drawn, which would damage the part. For example, assume that $\overline{\text{MR}}$ is driven by a +5V supply other than V_{CC} . If V_{CC} drops lower than +4.7V, $\overline{\text{MR}}$'s absolute maximum rating is violated [-0.3V to $(V_{CC} + 0.3\text{V})$], and undesirable current flows through the ESD structure from $\overline{\text{MR}}$ to V_{CC} . To avoid this, use the same supply for $\overline{\text{MR}}$ as the supply monitored by V_{CC} . This guarantees that the voltage at $\overline{\text{MR}}$ will never exceed V_{CC} .

Watchdog Input

The MAX6316_/MAX6317H/MAX6318_H/MAX6320P/MAX6321HP feature a watchdog circuit that monitors the μ P's activity. If the μ P does not toggle the watchdog input (WDI) within the watchdog timeout period (t_{WD}), reset asserts. The internal watchdog timer is cleared by reset or by a transition at WDI (which can detect pulses as short as 50ns). The watchdog timer remains cleared while reset is asserted. Once reset is released, the timer begins counting again (Figure 7).

The WDI input is designed for a three-stated output device with a $10\mu\text{A}$ maximum leakage current and the capability of driving a maximum capacitive load of 200pF . The three-state device must be able to source and sink at least $200\mu\text{A}$ when active. Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. When the watchdog timer is left open circuited, the timer is cleared internally at intervals equal to 7/8 of the watchdog period.

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

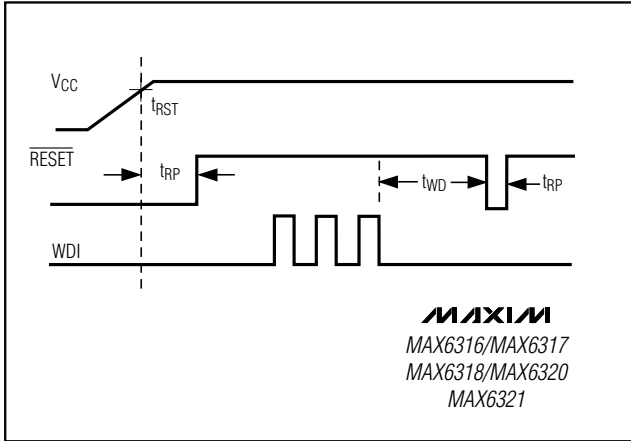


Figure 7. Watchdog Timing Relationship

Applications Information

Watchdog Input Current

The WDI input is internally driven through a buffer and series resistor from the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period. When high, WDI can draw as much as 160 μ A. Pulsing WDI high at a low duty cycle will reduce the effect of the large input current. When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain.

Negative-Going VCC Transients

These supervisors are immune to short-duration, negative-going VCC transients (glitches), which usually do not require the entire system to shut down. Typically, 200ns large-amplitude pulses (from ground to VCC) on the supply will not cause a reset. Lower amplitude pulses result in greater immunity. Typically, a VCC transient that goes 100mV under the reset threshold and lasts less than 4 μ s will not trigger a reset. An optional 0.1 μ F bypass capacitor mounted close to VCC provides additional transient immunity.

Ensuring Valid Reset Outputs Down to VCC = 0

The MAX6316_/MAX6317H/MAX6318_H/MAX6319_H/MAX6321HP/MAX6322HP are guaranteed to operate properly down to VCC = 1V. In applications that require valid reset levels down to VCC = 0, a pulldown resistor to active-low outputs (push/pull and bidirectional only, Figure 8) and a pullup resistor to active-high outputs (push/pull only, Figure 9) will ensure that the reset line is valid while the reset output can no longer sink or

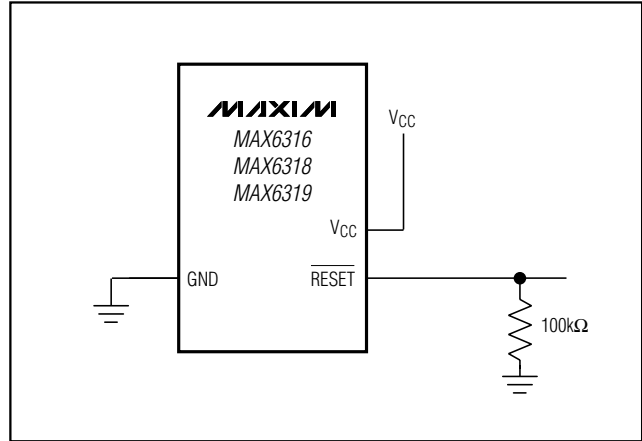


Figure 8. Ensuring $\overline{\text{RESET}}$ Valid to VCC = 0 on Active-Low Push/Pull and Bidirectional Outputs

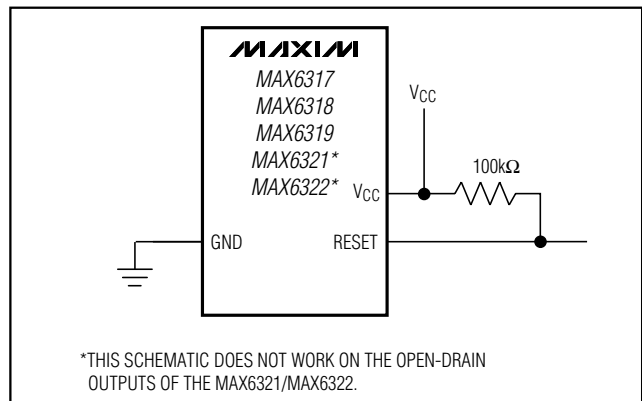


Figure 9. Ensuring RESET Valid to VCC = 0 on Active-High Push/Pull Outputs

source current. This scheme does not work with the open-drain outputs of the MAX6320/MAX6321/MAX6322. The resistor value used is not critical, but it must be large enough not to load the reset output when VCC is above the reset threshold. For most applications, 100k Ω is adequate.

Watchdog Software Considerations (MAX6316/MAX6317/MAX6318/MAX6320/MAX6321)

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

Figure 10 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the end of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would be quickly corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the *Watchdog Input Current* section, this scheme results in higher time average WDI current than does leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

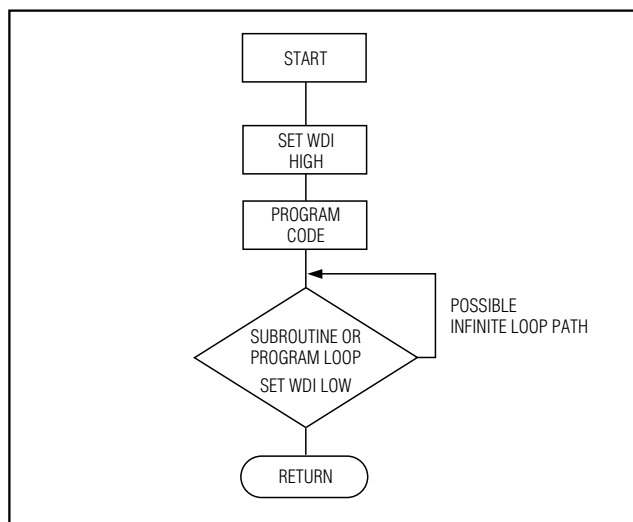
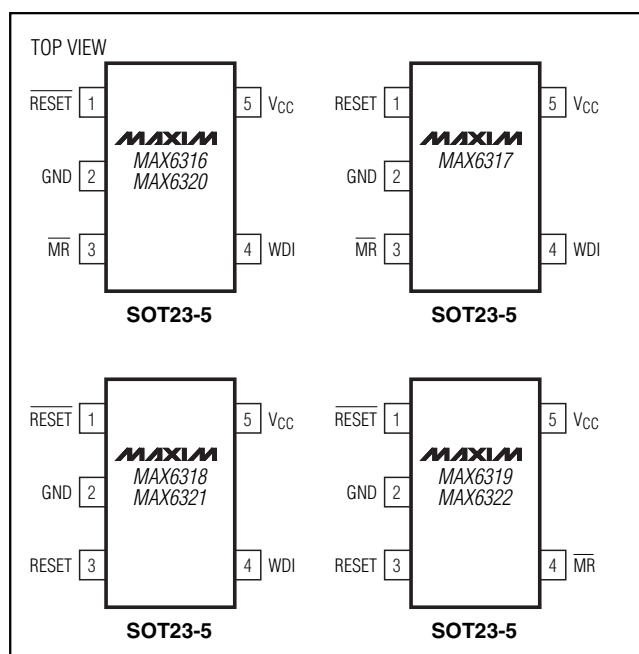
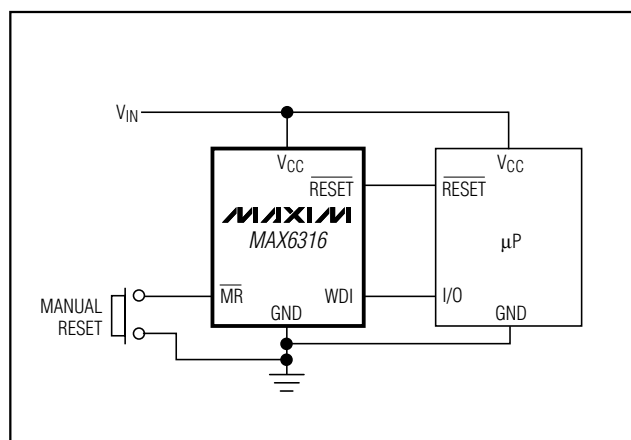


Figure 10. Watchdog Flow Diagram

Pin Configurations



Typical Operating Circuit



5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

Table 1. Factory-Trimmed Reset Thresholds

PART	T _A = +25°C			T _A = -40°C to +85°C	
	MIN	TYP	MAX	MIN	MAX
MAX63__50__-T	4.925	5.000	5.075	4.875	5.125
MAX63__49__-T	7.827	4.900	4.974	4.778	5.023
MAX63__48__-T	4.728	4.800	4.872	4.680	4.920
MAX63__47__-T	4.630	4.700	4.771	4.583	4.818
MAX63__46__-T	4.561	4.630	4.699	4.514	4.746
MAX63__45__-T	4.433	4.500	4.568	4.388	4.613
MAX63__44__-T	4.314	4.390	4.446	4.270	4.490
MAX63__43__-T	4.236	4.300	4.365	4.193	4.408
MAX63__42__-T	4.137	4.200	4.263	4.095	4.305
MAX63__41__-T	4.039	4.100	4.162	3.998	4.203
MAX63__40__-T	3.940	4.000	4.060	3.900	4.100
MAX63__39__-T	3.842	3.900	3.959	3.803	3.998
MAX63__38__-T	3.743	3.800	3.857	3.705	3.895
MAX63__37__-T	3.645	3.700	3.756	3.608	3.793
MAX63__36__-T	3.546	3.600	3.654	3.510	3.690
MAX63__35__-T	3.448	3.500	3.553	3.413	3.588
MAX63__34__-T	3.349	3.400	3.451	3.315	3.485
MAX63__33__-T	3.251	3.300	3.350	3.218	3.383
MAX63__32__-T	3.152	3.200	3.248	3.120	3.280
MAX63__31__-T	3.034	3.080	3.126	3.003	3.157
MAX63__30__-T	2.955	3.000	3.045	2.925	3.075
MAX63__29__-T	2.886	2.930	2.974	2.857	3.000
MAX63__28__-T	2.758	2.800	2.842	2.730	2.870
MAX63__27__-T	2.660	2.700	2.741	2.633	2.768
MAX63__26__-T	2.591	2.630	2.669	2.564	2.696
MAX63__25__-T	2.463	2.500	2.538	2.438	2.563

Table 2. Standard Versions

PART	RESET THRESHOLD (V)	MINIMUM RESET TIMEOUT (ms)	TYPICAL WATCHDOG TIMEOUTS (s)	SOT TOP MARK
MAX6316LUK29CY-T	2.93	140	1.6	ACDE
MAX6316LUK46CY-T	4.63	140	1.6	ACDD
MAX6316MUK29CY-T	2.93	140	1.6	ACDG
MAX6316MUK46CY-T	4.63	140	1.6	ACDF
MAX6317HUK46CY-T	4.63	140	1.6	ACDQ
MAX6318LHUK46CY-T	4.63	140	1.6	ACDH
MAX6318MHUK46CY-T	4.63	140	1.6	ACDJ
MAX6319LHUK46C-T	4.63	140	—	ACDK
MAX6319MHUK46C-T	4.63	140	—	ACDM
MAX6320PUK29CY-T	2.93	140	1.6	ACDO

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

MAX6316-MAX6322

Table 2. Standard Versions (continued)

PART	RESET THRESHOLD (V)	MINIMUM RESET TIMEOUT (ms)	TYPICAL WATCHDOG TIMEOUTS (s)	SOT TOP MARK
MAX6320PUK46CY-T	4.63	140	1.6	ACDN
MAX6321HPUK46CY-T	4.63	140	1.6	ACGL
MAX6322HPUK46C-T	4.63	140	1.6	ACGN

Note: Thirteen standard versions are available, with a required order increment of 2500 pieces. Sample stock is generally held on standard versions only. The required order increment for nonstandard versions is 10,000 pieces. Contact factory for availability.

Table 3. Reset/Watchdog Timeout Periods

RESET TIMEOUT PERIODS				
SUFFIX	MIN	TYP	MAX	UNITS
A	1	1.6	2	ms
B	20	30	40	
C	140	200	280	
D	1.12	1.60	2.24	s
WATCHDOG TIMEOUT				
W	4.3	6.3	9.3	ms
X	71	102	153	
Y	1.12	1.6	2.4	s
Z	17.9	25.6	38.4	

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX6319LHUK____-T	-40°C to +85°C	5 SOT23-5
MAX6319MHUK____-T	-40°C to +85°C	5 SOT23-5
MAX6320PUK____-T	-40°C to +85°C	5 SOT23-5
MAX6321HPUK____-T	-40°C to +85°C	5 SOT23-5
MAX6322HPUK____-T	-40°C to +85°C	5 SOT23-5

Note: These devices are available with factory-set V_{CC} reset thresholds from 2.5V to 5V, in 0.1V increments. Insert the desired nominal reset threshold (25 to 50, from Table 1) into the blanks following the letters UK. All devices offer factory-programmed reset timeout periods. Insert the letter corresponding to the desired reset timeout period (A, B, C, or D from Table 3) into the blank following the reset threshold suffix. Parts that offer a watchdog feature (see Selector Guide) are factory-trimmed to one of four watchdog timeout periods. Insert the letter corresponding to the desired watchdog timeout period (W, X, Y, or Z from Table 3) into the blank following the reset timeout suffix.

Chip Information

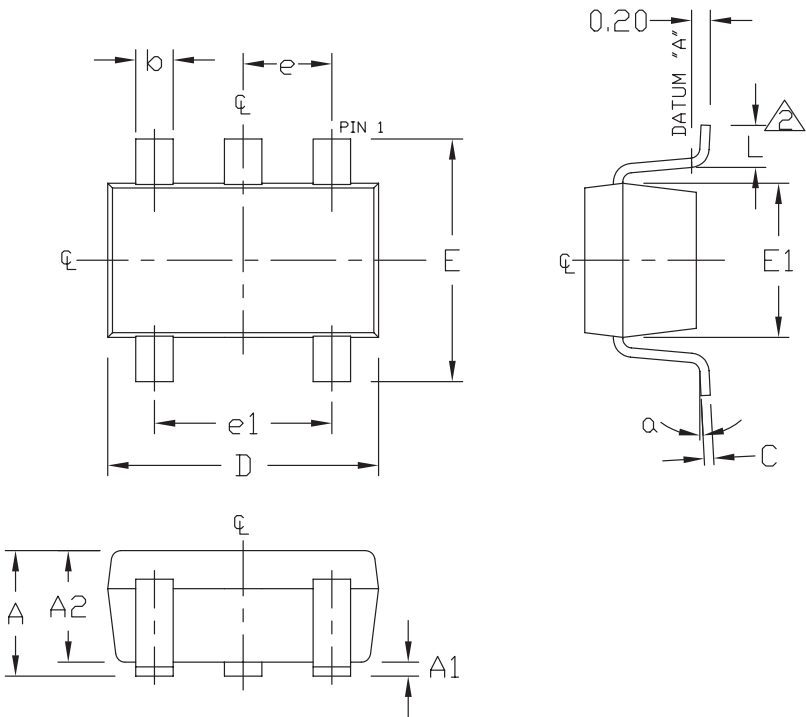
TRANSISTOR COUNT: 191

SUBSTRATE IS INTERNALLY CONNECTED TO V+

5-Pin μ P Supervisory Circuits with Watchdog and Manual Reset

Package Information

SOT-23



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°

- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
 3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
 4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
 5. MEETS JEDEC MO178.

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SOT-23, 5L

APPROVAL

DOCUMENT CONTROL NO.

21-0057

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