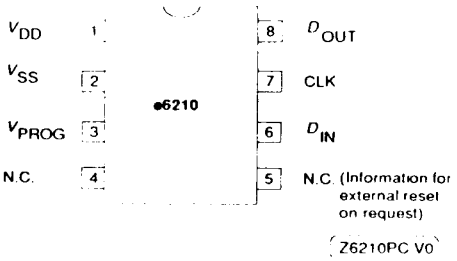
64 BIT SERIAL EEPROM

Features

- 64 bit serial organisation
- Bits individually addressable
- 2 Volt operation
- 100 000 erase/write cycles
- Self timed programming cycle
- 10 nA (typ.) stand-by current
- 8 pin package
- 10 years data retention time

Pad configuration



General description

The e6210 is a 64 bit serial EEPROM, produced in low voltage CMOS Silicon Gate Technology. The addressing scheme allows bit-wise access and an arbitary number of bits can be simultaneously written (or erased). Integrated on chip is all the necessary circuitry for operation of the EEPROM memory e.g. high voltage generation, timing logic for generation of the write/erase pulses and control logic for serial data transport.

Absolute maximum ratings

Supply voltage (V_{DD}-V_{SS})	-0.3 V ... +6 V
Input voltage range, all inputs	(V_{SS}-0.3 V) < V_I < (V_{DD}+0.3 V)
Output short circuit duration	indefinite
Power dissipation (DIL package)	125 mW*
Operating ambient temperatur range	-20° C ... +70°C
Storage temperature range	-40°C ... +125°C
Lead temperature during soldering at 2 mm distance, 10 sec	260°C

Absolute maximum ratings define parameter limits which, if exeeded, may permanently change or damage the device.

All inputs and outputs on EUROSIL electronic GmbH circuits are highly protected against electrostatic discharges However, precautions to minimize build-up of electrostatic charges during handling are recommended.

The circuits are protected against supply voltage reversal for typically 5 minutes.

* This value applies only to the package and will not be reached under normal operating conditions.

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Functional description

Memory cell

As well as the actual storage medium (FLOTOX cell), the memory cell contains a dynamic shift register for data transfer. Therefore the clock frequency for a serial data transfer must not be less than 20 kHz. After reading in the data, the dynamic shift register is configured to be a static latch, which stores the information during the write and erase cycles. Through these measures an extremely low current consumption is achieved, because current only flows during the (short) read pulse and during serial data transfer. For the rest of the time the circuit works completely statically, i.e. only leakage current flows.

HV-generator

The HV-generator produces the high voltage (-18 V) necessary for writing/erasing the EERPOM cells. The required supply voltage V_{PROG} is -5 V ±10%. To operate the complete circuit over a wide range of supply voltages, the supply voltage V_{PROG} has a separate connection. The V_{PROG} connection must only be at -5 V during programming, in normal operation it may remain unconnected. If the whole system always runs at 5 V, V_{PROG} can be connected to V_{SS}.

Control logic

The control logic provides all the necessary timing signals for serial data transfer, write/erase pulse width definition, read pulse sequence and OP-code decoding. A start bit and a 3 bit OP-code is used for the different operating modes (write/erase etc.). The clock input signal CLK is used as a timebase. Since all times/delays are not critical (including duration of write/erase pulses), the clock frequency may vary over a relatively wide range. After power up the chip has an initialization phase which lasts a maximum of 400 µsecs. During this time the chip can accept no OP-codes.

OP-code

A 3 bit OP-code is used to select the required operation modes. A LO to HI transition on D_{IN} prior to the 3 OP-code bits (during CLK = LO) is recognized as start condition. The OP-code definition is as follows:

OP-code	Bit 3	Bit 2	Bit 1	Function
OP0	0	0	0	Reserved code
OP1	0	0	1	Reserved code
OP2	0	1	0	Load shift register and write EEPROM
OP3	0	1	1	Load shift register and erase EEPROM
OP4	1	0	0	Reserved code
OP5	1	0	1	Reserved code
OP6	1	1	0	Reserved code
OP7	1	1	1	Read and shift out

Following is a detailed description of all OP-codes and how they perform:

OP2

Loads the shift register via the serial interface and performs a write operation. Bits to be written into the EEPROM have to be entered as logical HI into the shift register (see Figure 2). Bits that remain at LO will not be modified, i.e. the corresponding EEPROM cell remains in its previous state (written or erased).

OP3

Loads the shift register via the serial interface and performs an erase operation. Bits to be erased in the EEPROM have to be entered as logical LO into the shift register (see Figure 3a and Figure 3b). Bits that remain HI will not be modified, i.e. the corresponding EEPROM cell remains in its previous state (written or erased).

OP7

Is the read operation (see Figure 4a and Figure 4b). The EEPROM contents are transferred to the shift register and then after a delay of 6 clocks, serially shifted out.

Operating characteristics

V_{DD}=0 V (reference potential); V_{SS}=-5.0 V; V_{PROG}=-5 V; T_A=+25°C; all inputs open, unless otherwise specified

Parameter	Symbol	min.	typ. Note 1	max.	Unit	Conditions
Operating voltage	V_{SS}	-2	-5	-5.5	V	
Operating voltage HV-generator	V_{PROG}	-4.5	-5	-5.5	V	
Current consumption,serial data transfer	I_{SS}		20	40	µA	F_{CLK} = 50 kHz
Stand by current consumption	$I_{SS\ Stdby}$		10	100	nA	D_{IN}, CLK at V_{DD} or V_{SS}
Current consumption write/erase	I_{PROG}		400	600	µA	
D_{IN}, CLK LO level	$V_{DIN\ LO}$	V_{SS}-0.3 V		-0.9(V_{DD}-V_{SS})	V	
D_{IN}, CLK HI level	$V_{DIN\ HI}$	-0.1(V_{DD}-V_{SS})		V_{DD}+0.3 V	V	
D_{IN}, CLK leakage current	I_{Leak}			±100	nA	D_{IN}, CLK at V_{DD} or V_{SS}
D_{OUT} current LO	$I_{DOUT\ LO}$	1.6			mA	V_{DOUT} = V_{SS}+0.4 V
D_{OUT} current HI	$I_{DOUT\ HI}$	-0.5			mA	V_{DOUT} = V_{DD}-0.4 V
Clock frequency	F_{CLK}	20	50	100	kHz	
Write pulse length	t_W		50		msec	internally generated; F_{CLK} = 50 kHz
Erase pulse length	t_E		50		msec	internally generated; F_{CLK} = 50 kHz
Data set up time	$t_{Set\text{-}up}$	1			µsec	under all conditions
Data hold time	t_{Hold}	1			µsec	under all conditions
Data access time	t_{ACC}			3	µsec	under all conditions
Power on reset: Power supply voltage vs. power supply rise time	dV_{SS}/dt	-5			V/ msec	

Note 1:Typical parameters represent the statistical mean values

Figure 1: Block diagram

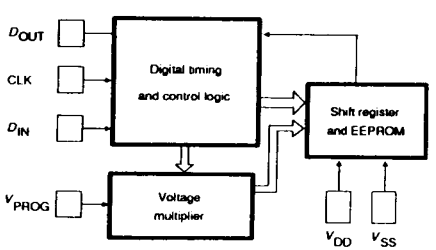

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Figure 2: OP2 (write) operation: Bit 63, 64 written, remaining bits unchanged

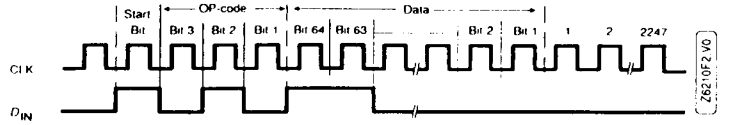


Figure 3a: OP3 (erase) operation: Bit 63, 64 erased, remaining bits unchanged

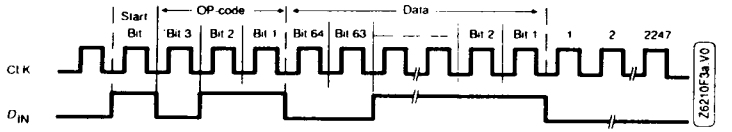


Figure 3b: Set up and hold time

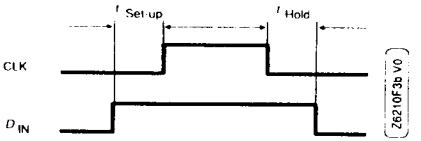


Figure 4a: OP7 = serial data out

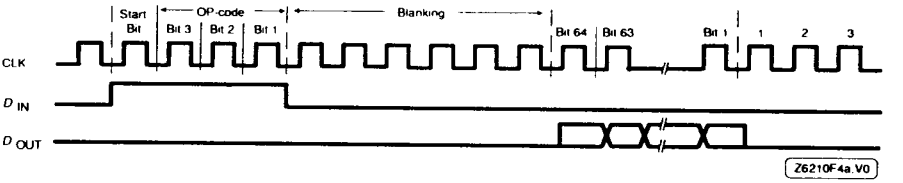
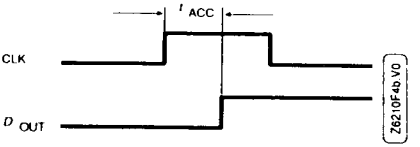


Figure 4b: Access time



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