# Edge818
# Octal 18V Pin Electronics Driver/window Comparator

**HIGH-PERFORMANCE PRODUCTS – ATE**

## Description

The Edge818 is an octal pin electronics driver and window comparator fabricated in a wide voltage CMOS process. It is designed specifically for Test During Burn In (TDBI) applications, where cost, functional density, and power are all at a premium.

The Edge818 incorporates eight channels of programmable drivers and window comparators into one 14 mm X 20 mm 100 pin MQFP package. Each channel has per pin driver levels, data, and high impedance control. In addition, each comparator has per pin high and low threshold levels.

The Edge818 uses "Flex In" and "Flex Out" digital inputs, and can therefore mate directly with any digital technology providing a minimum 2V swing. The digital outputs can mate directly with any digital technology.

The 18V driver output and receiver input range allow the Edge818 to interface directly with TTL, ECL, CMOS (3V, 5V, and 7V), LVCMOS, and custom level circuitry, as well as the high voltage (Super Voltage) level required for many special test modes for Flash Devices.

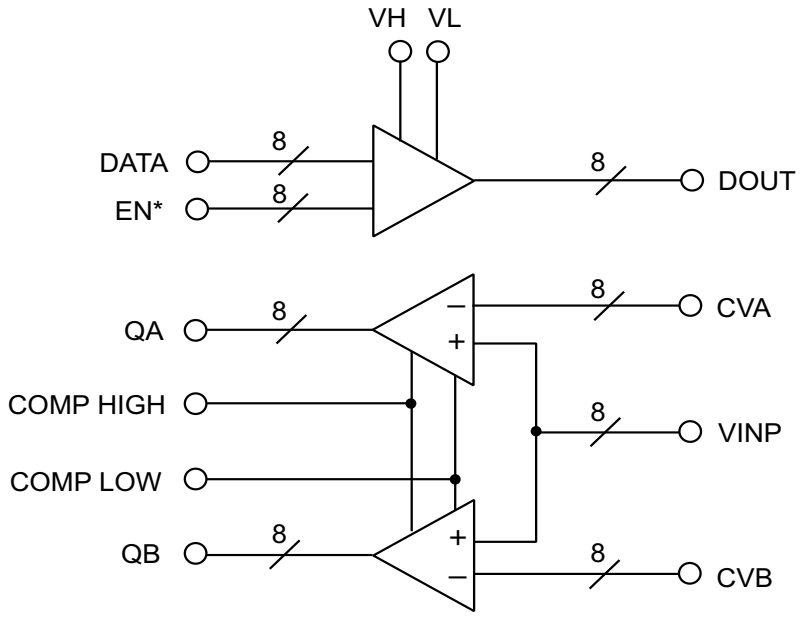
## Features

- 18V I/O Range
- 50 MHz Operation
- Per Pin Flexibility
- Programmable Input Thresholds
- Flex In Digital Inputs
- Flex Out Digital Outputs
- Small footprint (100 pin MQFP)

## Applications

- Burn In ATE
- Low Cost ATE
- Instrumentation

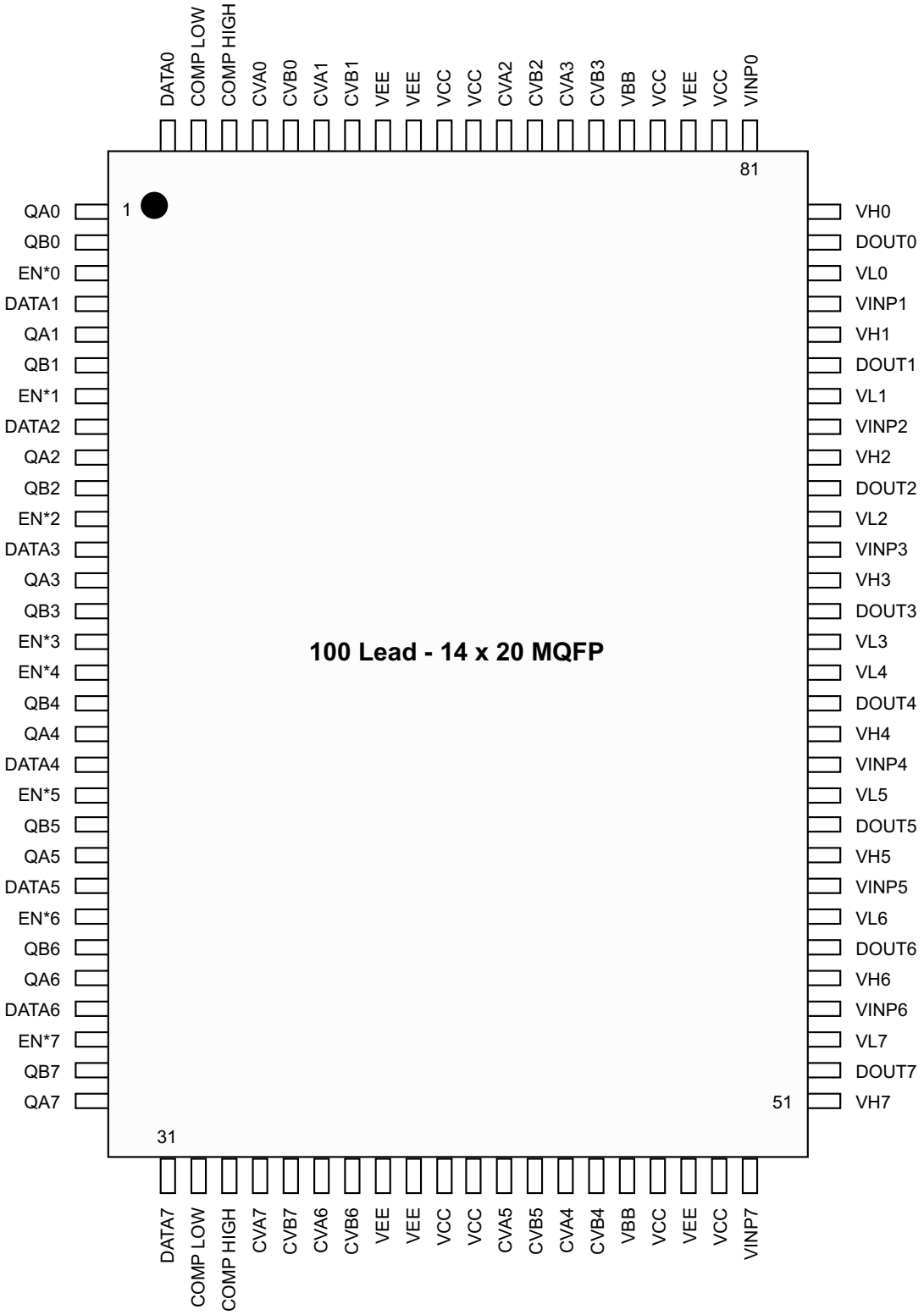
## Functional Block Diagram



## PIN Description

| Pin Name | Pin Number | Description |
|---|---|---|
| DATA (0:7) | 100, 4, 8, 12, 19, 23, 27, 31 | Digital inputs which determine the high/low state of the driver, when it is enabled. |
| EN* (0:7) | 3, 7, 11, 15, 16, 20, 24, 28 | Digital inputs wihch enable/disable the driver. |
| QA (0:7)<br>QB (0:7) | 1, 5, 9, 13, 18, 22, 26, 30<br>2, 6, 10, 14, 17, 21, 25, 29 | Comparator digital outputs. |
| DOUT (0:7) | 79, 75, 71, 67, 64, 60, 56, 52 | Driver Outputs. |
| VINP (0:7) | 81, 77, 73, 69, 62, 58, 54, 50 | Comparator Inputs. |
| VH (0:7) | 80, 76, 72, 68, 63, 59, 55, 51 | Unbuffered analog inputs that set the driver "high" voltage level. |
| VL (0:7) | 78, 74, 70, 66, 65, 61, 57, 53 | Unbuffered analog inputs that set the driver "low" voltage level. |
| CVA (0:7) | 97, 95, 89, 87, 44, 42, 36, 34 | Analog inputs that set the threshold for the A comparators. |
| CVB (0:7) | 96, 94, 88, 86, 45, 43, 37, 35 | Analog inputs that set the threshold for the B comparators. |
| VBB | 46, 85 | Analog input voltage that sets the threshold for the digital inputs. |
| COMP HIGH | 33, 98 | Unbuffered analog input that sets the high level of the comparator outputs. |
| COMP LOW | 32, 99 | Unbuffered analog input that sets the low level of the comparator outputs. |
| VCC | 40, 41, 47, 49, 82, 84, 90, 91 | Positive power supply. |
| VEE | 38, 39, 48, 83, 92, 93 | Negative power supply. |

## PIN Description *(continued)*



## Circuit Description

### Driver Description

The Edge818 supports programmable high and low levels and tristate per channel. There are no shared lines between any drivers. The EN* and DATA signals are wide voltage high impedance analog inputs capable of receiving digital signals over a wide common mode range. VBB is the high impedance analog input which sets the threshold for EN* and DATA.

| EN*, DATA | Status |
|---|---|
| > VBB | "1" |
| < VBB | "0" |

With EN* high, the driver goes into a high impedance state. With EN* low, DATA high forces the driver into a high state, and DATA low forces the driver into a low state.

| EN* | DATA | DOUT |
|---|---|---|
| 1 | X | HiZ |
| 0 | 1 | VH |
| 0 | 0 | VL |

### Drive High and Low

VH and VL define the logical "1" and "0" levels of the driver, and can be adjusted anywhere over the range determined by VCC and VEE. There are no restrictions between VH and VL, other than they must remain within the power supply levels.

$$VEE \leq VH \leq VCC$$
$$VEE \leq VL \leq VCC$$

The VH and VL inputs are unbuffered in that they also provide the driver output current (see Figure 3), so the source of VH and VL must have ample current drive capability.

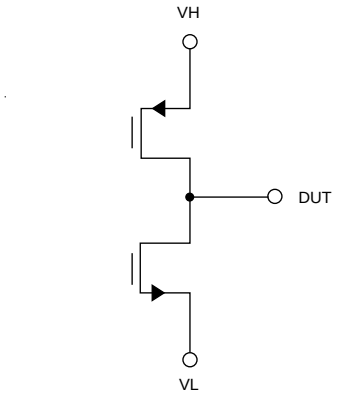



***Figure 3. Simplified Model of the Unbuffered Output Stage***

### Driver Output Protection

In a functional testing environment, where a resistor is added in series with the driver output to create a 50Ω driver, the Edge818 can withstand a short to any legal voltage for an indefinite amount of time.

In a low impedance application, with no additional output resistance, the system should be designed to check for a short circuit prior to connecting the driver, and tristate the driver if a short is detected.

### Receiver Description

The Edge818 supports a window comparator with independent threshold levels per channel. There are no shared comparator lines between channels. CVA and CVB are high impedance analog voltage inputs which define the threshold voltages for comparators A and B.

If VINP is more positive than CVA or CVB, QA and QB will be high. Otherwise, QA and QB will be low.

| VINP | | | QA |
|---|---|---|---|
| VINP | > | CVA | COMP HIGH |
| VINP | < | CVA | COMP LOW |

| VINP | | | QB |
|---|---|---|---|
| VINP | > | CVB | COMP HIGH |
| VINP | < | CVB | COMP LOW |

## Circuit Description *(continued)*

The comparator outputs are "Flex Out". They are technology independent and may be adjusted over a wide voltage common mode range. COMP HIGH and COMP LOW are analog inputs which set the digital high and low levels (respectively) of QA and QB. COMP HIGH and COMP LOW are unbuffered inputs that provide the necessary drive current, so the sources for these levels must have adequate current capability.

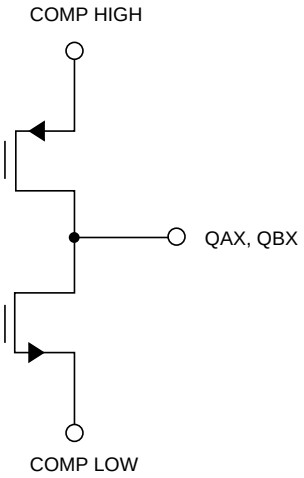



***Figure 4. Simplified Model of the Unbuffered Comparator Output Stage***

Typically, COMP HIGH and COMP LOW will be connected to the digital power supplies of the chip receiving QA and QB.

**Receiver Headroom**

There is ~3V of headroom required between the comparator thresholds and both power supply levels.

$$VEE + 3.0 \leq CVA, CVB \leq VCC - 3.0$$

## Application Information

### Power Supply Decoupling

VCC and VEE should be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor. A VCC and VEE plane, or at least a solid power bus, is recommended for optimal performance.

### VH and VL Decoupling

As the VH and VL inputs are unbuffered and supply the driver output current, which can be quite large during edge transitions, decoupling capacitors for these inputs are recommended in proportion to the amount of output current requirements.

For applications where VH and VL are shared over multiple channels, a solid power plane to distribute these levels is preferred.

### VBB

The two VBB pins are connected together on-chip. Therefore, only one VBB needs to be connected to for proper 818 operation.

The two pins may be used to daisy chain a VBB signal across a PC Board without having to route the actual signal underneath the 818.

### Latchup Protection

The Edge818 has several power supply requirements to protect the part in power supply fault situations, as well as during power up and power down sequences. VCC must remain greater than or equal to VDD (external supply for the digital logic) at all times. Both VCC and VDD must always be positive (above ground), and VEE must always be negative (at or below ground).

The three diode configuration shown in Figure 5 should be used on a once-per-board basis.

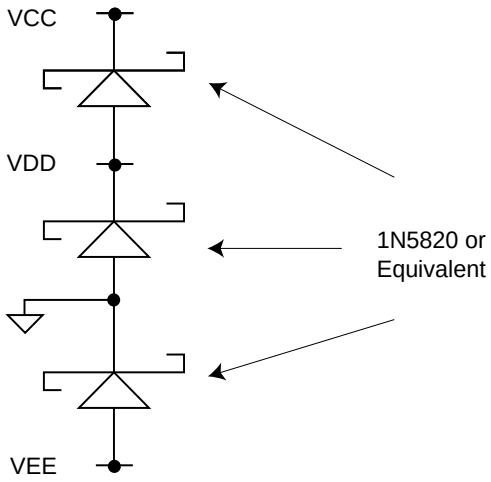
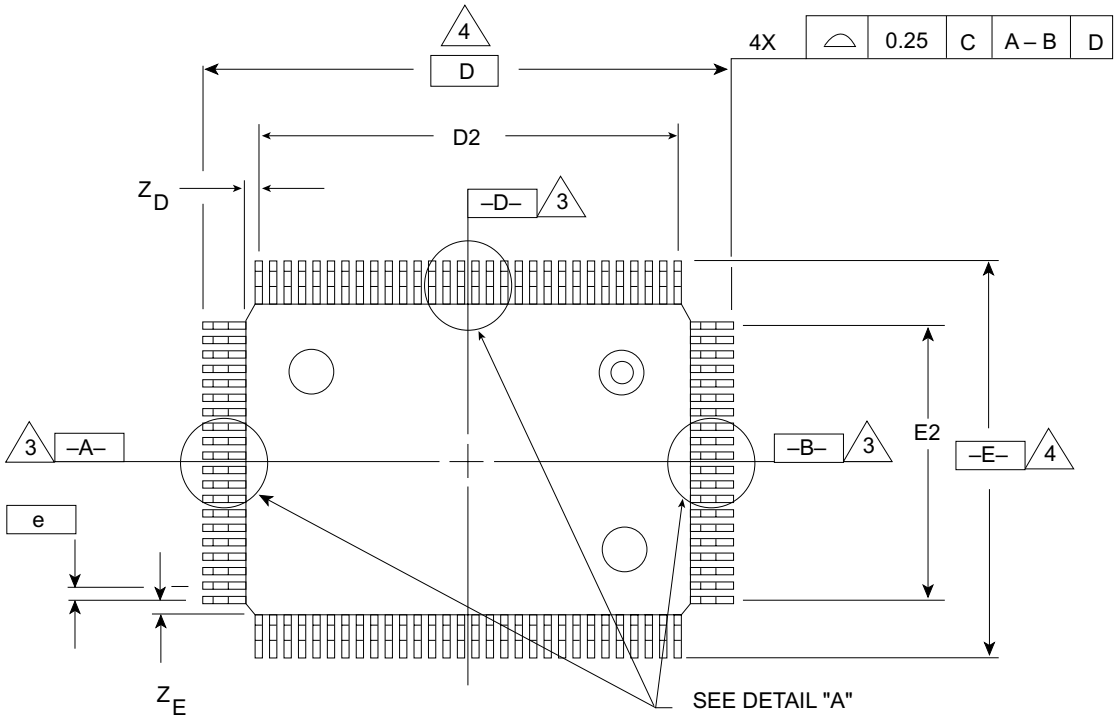



***Figure 5.***
***Power Supply Protection Scheme***

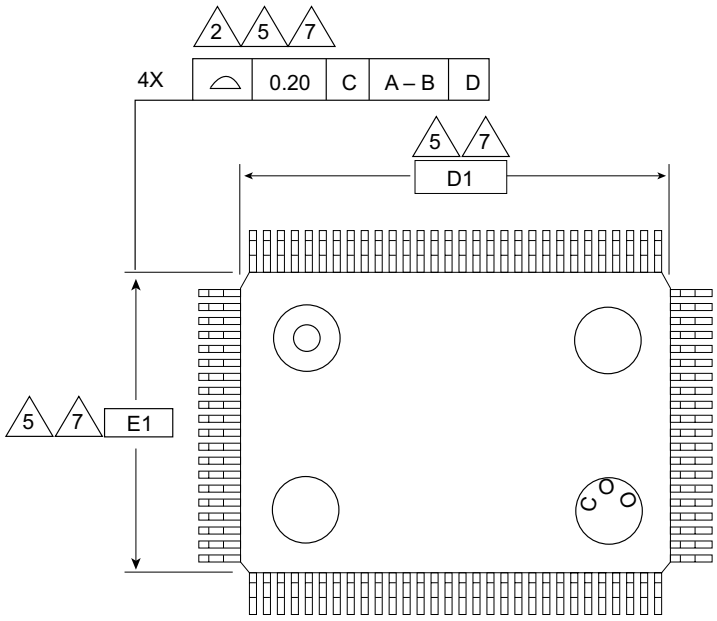
**Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE –0.5V to VCC +0.5V at any time, either during power up, normal operation, or during power down. Failure to adhere to this requirement could result in latchup of the device, which could be destructive if the system power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.**

## Package Information

**100-Pin MQFP**
**14 mm x 20 mm**

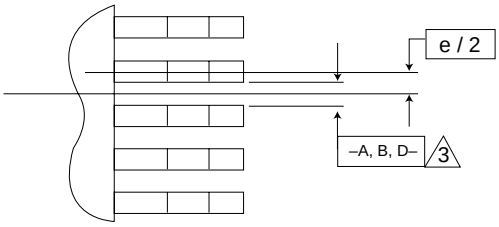



TOP VIEW

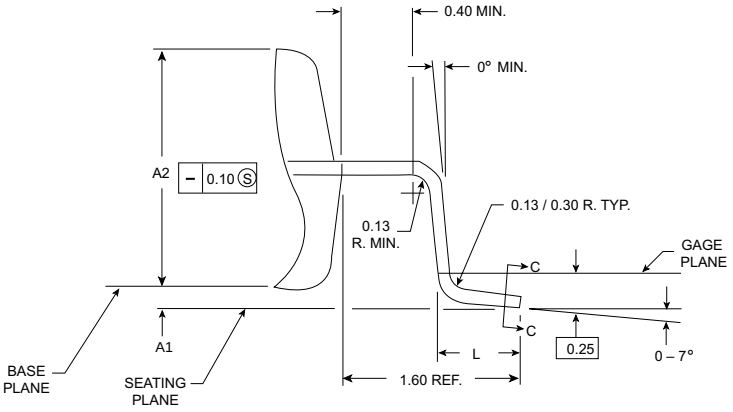



BOTTOM VIEW

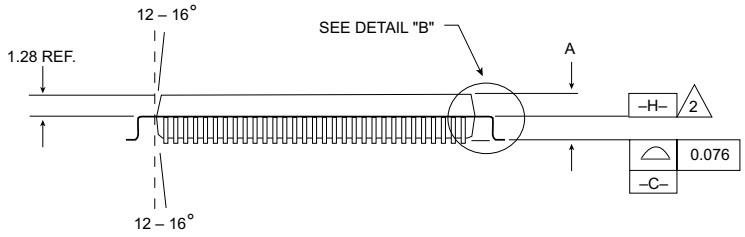
## Package Information *(continued)*

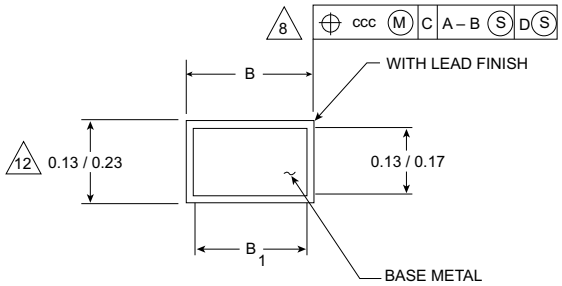



DETAIL "A"




DETAIL "B"




SECTION C–C

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined where centerline between leads exits plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
8. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lowerradius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outlines MS-108 and MS-022.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

**Variations**
**(all dimensions in millimeters)**

| Symbol | Min | Nom | Max | Note | Comments |
|---|---|---|---|---|---|
| A | | 3.04 | 3.40 | | Height above PCB |
| A1 | 0.25 | 0.33 | | | Gap above PCB |
| A2 | 2.57 | 2.71 | 2.87 | | Body Thickness |
| D | | 23.20 BSC | | 4 | |
| D1 | | 20.00 BSC | | 5 | Body Dimension |
| D2 | | 18.85 REF | | | |
| ZD | | 0.58 REF | | | |
| E | | 17.20 | | 4 | |
| E1 | | 14.00 BSC | | 5 | Body Dimension |
| E2 | | 12.35 REF | | | |
| ZE | | 0.83 REF | | | |
| L | 0.73 | 0.88 | 1.03 | | |
| N | | 100 | | 6 | Pin Count |
| e | | 0.65 BSC | | | Lead Pitch |
| B | 0.22 | | 0.38 | 8 | Pad Dimension |
| B1 | 0.22 | 0.30 | 0.33 | | Pad Dimension |
| ccc | | 0.13 | | | |
| ND | | 30 | | | Side Pin Count |
| NE | | 20 | | | Side Pin Count |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Total Analog Supply | VCC - VEE | 12.0 | | 18.0 | V |
| Ambient Operating Temperature | TA | | | +70 | °C |
| Junction Temperature | TJ | | | +125 | °C |
| Thermal Resistance of Package (Junction to Still Air) | $\theta_{JA}$ | | 32.2 | | °C/W |
| Thermal Resistance of Package (Junction to Case) | $\theta_{JC}$ | | 12.4 | | °C/W |

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Total Power Supply | VCC - VEE | -0.5 | 19.0 | V |
| Digital Input Voltages | DATA, EN* | VEE - .5 | VCC + .5 | V |
| Analog Input Voltages | VH, VL, CVA, CVB, VINP, VBB | VEE - .5 | VCC + .5 | V |
| Analog Output Voltages | DOUT, COMP HIGH, COMP LOW | VEE - .5 | VCC + .5 | V |
| Ambient Operating Temperature | TA | -50 | +125 | °C |
| Storage Temperature | TS | -65 | +150 | °C |
| Junction Temperature | TJ | | +150 | °C |
| Soldering Temperature (5 seconds, .25" from the pin) | TSOL | | +260 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## DC Characteristics

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Driver*** | | | | | |
| High Voltage | VH | VEE | | VCC | V |
| Low Voltage | VL | VEE | | VCC | V |
| Output Swing | VH – VL | VEE | | VCC | V |
| HiZ Leakage Current | Ileak | –2.0 | 0 | +2.0 | nA |
| Output Impedance | Rout | 9.0 | 12 | 15 | Ω |
| DC Output Current (Note 1) | Iout DC | –125 | | +125 | mA |
| AC Output Current (Note 2) | Iout AC | –400 | | +400 | mA |
| ***Receiver*** | | | | | |
| Input Voltage Range | VINP | VEE | | VCC | V |
| Threshold Voltage Range | CVA, CVB | VEE + 3.0 | | VCC – 3.0 | V |
| Offset Voltage (Note 3) | Vos | –200 | | +100 | mV |
| Input Bias Current | Ibias | –10 | 0 | +10.0 | nA |
| Output Voltage Range | COMP HIGH | –2.0 | | +5.0 | V |
| | COMP LOW | –2.0 | | +5.0 | V |
| QA, QB Output Impedance | Rout | 30 | 40 | 50 | Ω |
| DC Output Current Capability | | -50 | | 50 | mA |
| ***Digital Inputs*** | | | | | |
| Input High Voltage | EN*, DATA - VBB | 1.0 | | | V |
| Input Low Voltage | VBB - EN*, DATA | 1.0 | | | V |
| Input Current | Iin | –100 | 0 | +100 | nA |
| ***Power Supplies*** | | | | | |
| Positive Supply Current (Note 4) | ICC | 36 | 57 | 78 | mA |
| Negative Supply Current (Note 4) | IEE | 36 | 57 | 78 | mA |

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

*Note 1:* DC output current is specified per individual driver.
*Note 2:* Surge current capability for durations of < 2 seconds.
*Note 3:* Offset voltage is tested at CVA, CVB = 1.5V.
*Note 4:* Power supply current tested with VCC = +15V, VEE = –3V.

## AC Characteristics

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Driver*** | | | | | |
| DATA to DOUT | Tpd | 9.5 | 14.5 | 19.5 | ns |
| EN* to DOUT (Active to HiZ) (Note 1) | Tpd | 10 | 20 | 30 | ns |
| EN* to DOUT (HiZ to Active) | Tpd | 11 | 16 | 21 | ns |
| Rise/Fall Times (Note 2) | | | | | |
| 1V Swing (20% - 80%) | Tr/Tf | | 1.5 | | ns |
| 3V Swing (10% - 90%) | Tr/Tf | | 1.9 | | ns |
| 5V Swing (10% - 90%) | Tr/Tf | | 2.0 | | ns |
| 10V Swing (10% - 90%) | Tr/Tf | | 2.5 | | ns |
| 15V Swing (10% - 90%) | Tr/Tf | | 3.2 | | ns |
| Maximum Operating Frequency (Note 3) | Fmax | 50 | | | MHz |
| Minimum Pulse Width | | | 8 | 11 | ns |
| ***Receiver*** | | | | | |
| Comparator (Note 4) | | | | | |
| Tpd+ | Tpd | 11.5 | 17.5 | 19.5 | ns |
| Tpd- | | 14.5 | 20.5 | 23.5 | ns |
| Maximum Operating Frequency (Note 3) | Fmax | 50 | | | MHz |
| Minimum Pulse Width | | | 10 | 15 | ns |

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

*Note 1:* Load = 10 mA and measured when a 1V change at the output is detected. (VH = 3V, VL = 0V, VFLOAT = 1.5V, tested at 1V and 2V.)

*Note 2:* Into 18 cm of 50 Ω transmission line terminate with 1 KΩ, with proper series termination resistor.Guaranteed by characterization. This parameter is not tested in production.

*Note 3:* This parameter is production tested at 40 MHz.

*Note 4:* Tested under no-load conditions.

## Ordering Information

| Model Number | Package |
|---|---|
| E818AHF | 100 Lead MQFP<br>14 mm x 20 mm Body Size<br>w/Internal Heat Spreader |
| EVM818AHF | Edge818 Evaluation Board |

## Contact Information

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## Revision History

**Current Revision Date:** December 3, 2001
**Previous Revision Date:** March 13, 2001

| Page # | Section Name | Previous Revision | Current Revision |
|---|---|---|---|
| 5 | Receiver Headroom | There is ~2V of headroom ...<br><br>VEE + 2.0 <= CVA,CVB <= VCC – 2.0 | There is ~3V of headroom ...<br><br>VEE + 3.0 <= CVA,CVB <= VCC – 3.0 |
| 9 | Recommended Operating Conditions | | *Add:* Thermal Resistance of Package (Junction to Still Air)<br>Thermal Resistance of Package (Junction to Case) |
| 10 | DC Characteristics | | *Delete:* Positive & Negative Supply Levels<br>*Add:* Note 4 |

**Current Revision Date:** March 13, 2001
**Previous Revision Date:** May 23, 2000

| Page # | Section Name | Previous Revision | Current Revision |
|---|---|---|---|
| 11 | AC Characteristics | Comparator, Symbol: 700 ps | Comparator, Symbol: Tpd<br><br>*Add:* Note 4 |