Programmable Encoder/Decoder

Ordering Information

Device	Package			
	Plastic DIP (#Pins)	J-Lead PLCC (# pins)	Plastic SOW Gullwing (# pins)	Die
ED5	ED5P (18)	—	—	—
ED9	ED9P (18)	—	ED9WG (20)	—
ED10	—	—	ED10WG (20)	—
ED11	ED11P (28)	—	ED11WG (28)	—
ED15	ED15P (28)	ED15PJ (28)	ED15WG (28)	ED15X

Features

- Manchester phase encoding
- Encoder/decoder in one circuit
- Schmitt Trigger Input for excellent noise rejection
- Built-in oscillator using non-critical RC components
- Zener diode to regulate the power supply
- Low power, high noise immunity CMOS technology
- Ability to decode original signals
- Automatic preamble generation

Applications

- Smoke & fire alarm control systems
- Security systems
- Theft alarm systems
- Digital locks
- Digital paging systems
- Garage door openers
- Systems that require a special identification code
- Pocket pagers
- Recognition or transmission

General Description

The ED series is a single monolithic chip using metal-gate CMOS technology for low cost, low power, high yield and high reliability. It is a dual purpose circuit, capable of working either as an encoder, or as decoder of its own transmissions, in applications where exclusive recognition of a special code is required. It will decode up to1 of 32,768 codes. In the transmit mode, each circuit is capable of generating the possible codes by connecting the Data Inputs to V_{DD} or GND for a "1" or a "0". In the receive mode, each circuit is capable of decoding the transmitted signal and simultaneously making a comparison to the local address code for identification.

Absolute Maximum Ratings

Supply Voltage with respect to GND	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GND = 0V; T_A = 25°C)

Symbol	Parameter	Min	Typ Note 1	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	GND- 0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for pins T/R, SDI
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, D1-D15
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{OUT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GND all outputs floating

Notes:

1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.
2. This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ Note1	Max	Unit	Conditions
f_c	Clock Frequency	0		20	kHz	R= 150k, C= 100pF; Clock Period (t_c)=1/f_C
t_{SDI}	Start Pulse Width	500			ns	
t_{DDO}	DDO Delay from SDI		5		µs	
t_{DC}	Data Clock Pulse Width		.5t_C		sec	
t_{WORD}	Full Cycle Word Length		130t_C		sec	
R_R	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
C_R	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor (C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note: This pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.

RS	Reset Input	This input pin may be used to override the data transmission cycle or to inhibit an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pf) to V_{DD} may be added for power-up reset. The Reset function is activated when this input is connected to V_{DD}.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And in the receive mode, this input receives the serial coded information for processing and comparison.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
D1-D15	Data Bit Inputs	These Inputs provide parallel input data to be sequentially transmitted. The 18-pin package options have some pins omitted and hence these data positions will have logical zeros transmitted. In the receive mode, these inputs become the parallel local address code for comparison with the incoming data. Note that with the ED11 and ED5 options, the data bits 11-15 are not used in the comparison when in the receive mode.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmitt Trigger, a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of a 16-bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered regardless of its comparison to a preset address word.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this Output signal pulse indicates that a new word has just begun processing.
DC	Data Clock Output	The Data Clock output may be used in a receive system since it is the recovered data sync pulses. Also, this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode; a logic low puts it in the receive mode.
V_{DD}	V_{DD}	Positive Supply Potential: This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Operation

ED15 General Description

The ED15 mode of operation is controlled by the Transmit/ Receive control input (T/R). When switched from V_{DD} to GND, the circuit will automatically change the oscillator, Start/Data input, and Data/Decoder Output from Transmit to Receive mode.

The circuit contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5% in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1 - D_{15} drives, the resistors should be tied to a voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

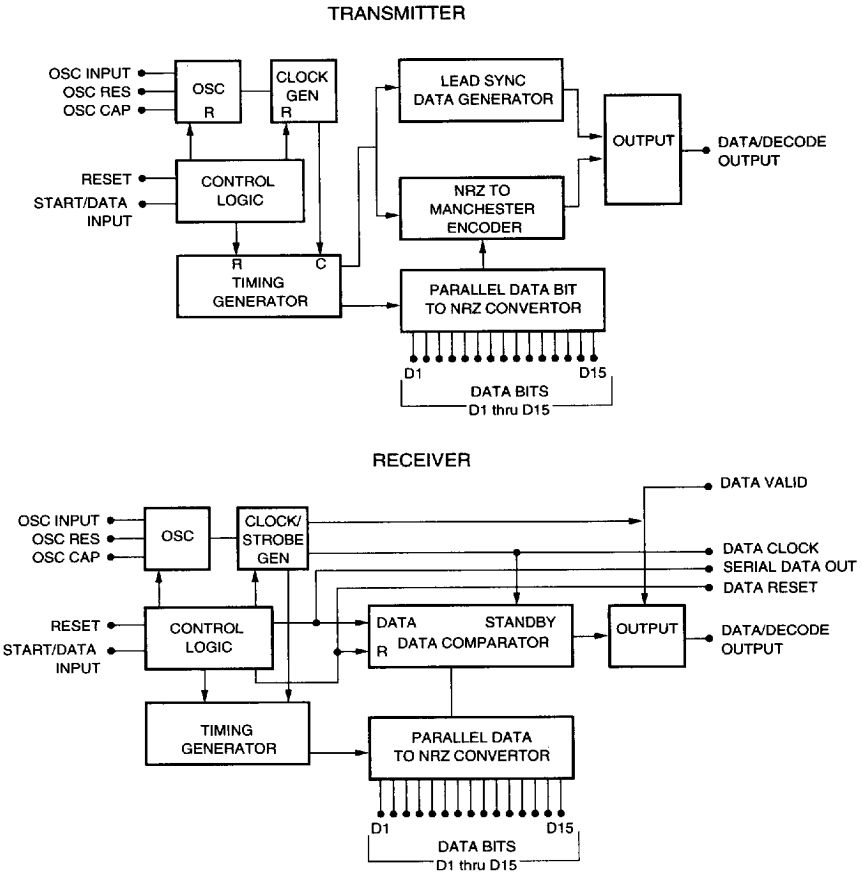
Output drivers are capable of sinking or sourcing 1.0 mA minimum at 1.0 volt V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The Data Inputs each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The Transmit/Receive input does not have a pull up or pull down resistor. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger Input circuit to improve noise rejection.

Encoder Function

This function is selected by connecting the Transmit/Receive control input to V_{DD}. This enables the Transmit mode and the circuit to function as an encoder, sampling the 15 Data Input pins' digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded), and presenting it to the D/DO pin for transmission (usually to another ED device used as the decoder circuit). The encoder will transmit the serial data each time the Start/Data input is activated.

This encoded Data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1's", then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 15 bits of addresses and/or controls.

Block Diagrams



Decoder Function

The receive mode is selected by connecting the Transmit/Receive control input to ground. In this mode the circuit will work as a decoder, receiving the serial data in Manchester Encoded format and recovering the clock. The incoming data is converted to a 15-bit serial word. It is compared with the local data word by sampling the Data Inputs (15-bits). These bits are usually programmed to the expected Data that will be decoded. If the two data words match, the decoded output will become logic "1" state, but if the two words do not match the decoded output will stay low. Also, if the words do not match but the bit stream was valid (i.e., 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12 bits will be recognized. But during the 13th interval where no bit transition occurs, the circuit times out and awaits the start bit of the data sequence.

ED5 Option

The 18-pin packaging option of the ED11 die is called ED5. In the transmit mode it is only capable of 5 bits of programmable code. All the other bits are held at zero. But in the receive mode, the circuit has the five (32) unlock code bits plus the last four transparent bits of the ED11. The ED5 also supplies the necessary output signals to process the 4 bits of control data.

ED9 Option

The ED9 is an 18-pin packaging of the ED15 die. The operation and function of this circuit is the same as the ED15; the only difference being the available pins. In the transmit mode the circuit is only capable of encoding 9 bits of data, the other 6 bits are not programmable and remain zeros. The pin configuration also drops DV, DC, DRS, and SDO such that the circuit can now only respond to a data match condition on the only output, #D/DO. In the receive mode the circuit can decode the same 9 bits of data, enabling up to 512 possible addresses.

ED10 Option

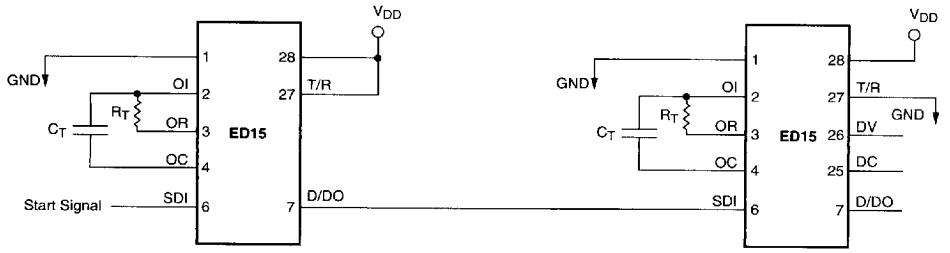
The ED10 is an ED9 in the 20-pin package. The 2 additional pins are one more data pin (hence ED10) and the DRS pin. The latter is useful for multiple transmissions as shown in the Figures below. This can lead to more reliable reception in some circumstances.

ED11 Option

The ED11 differs from the ED15 in that in the receive mode the ED11 will only compare the first 11 bits and ignore the state of the last 4 bits; that is, 2048 distinct address codes with 4 bits may be used for control data transmission.

Transmit and Receive Data Patterns of ED-Series Devices

ED15



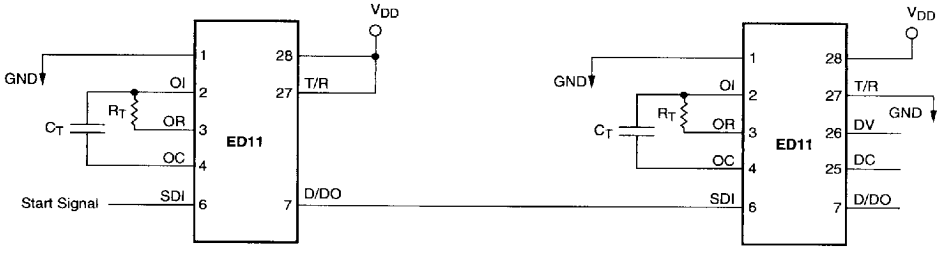
Transmitted Bit Sequence

1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D1															D15

Received Address Code

1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D1															D15

ED11 to ED11



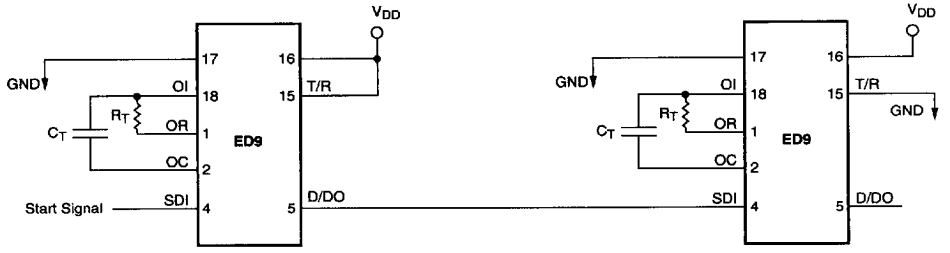
Transmitted Bit Sequence

1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D1															D15

Received Address Code

1	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D
D1															D15

ED9



Transmitted Bit Sequence

1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

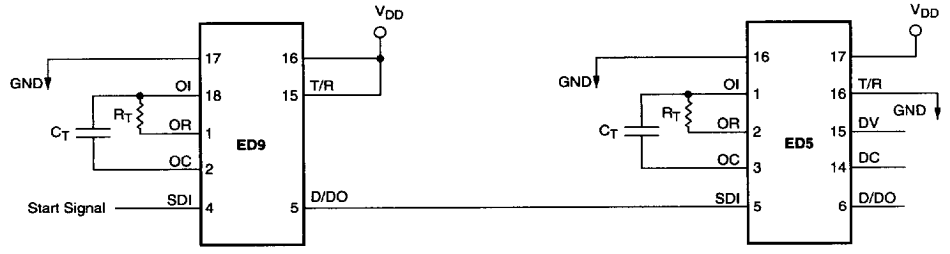
D1 D15

Received Address Code

1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

D1 D15

ED9 to ED5



Transmitted Bit Sequence

1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

D1 D15

Received Address Code

1	0	0	0	X	X	X	X	0	X	0	0	D	D	D	D

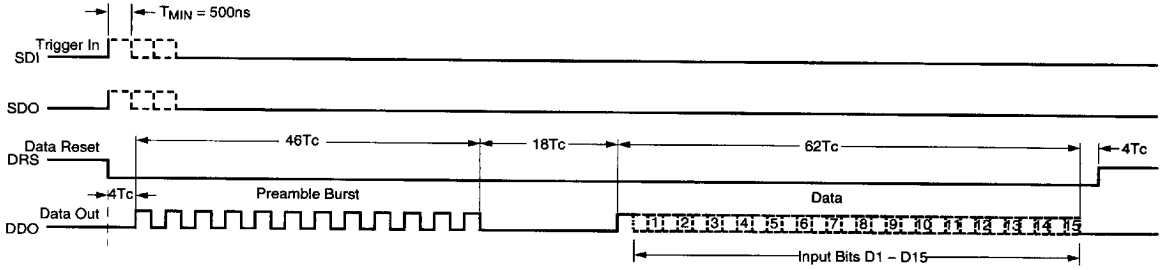
D1 D15

Notes:

Bit Sequence Code Format
- X = Programmable
- 0 = Hardwired Internally Zero
- 1 = Hardwired Internally One
- D = Don't Care in Receive Mode

When unused, the DV, DC, DRS and SDO pins should be left floating and **must not** be tied to either a power supply or to ground.

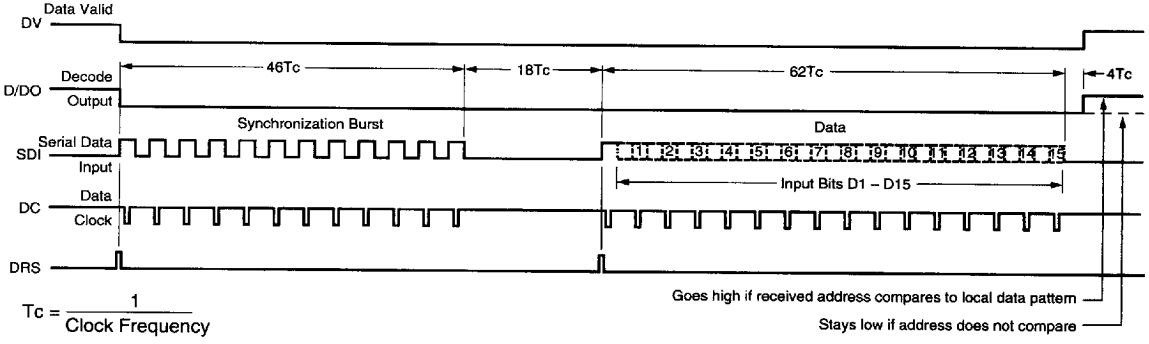
Timing Diagram – Transmit Mode



Total Time Required for Transmission of One Sequence = (DRS – 4Tc) =130Tc

$$Tc = \frac{1}{\text{Clock Frequency}}$$

Timing Diagram – Receive Mode

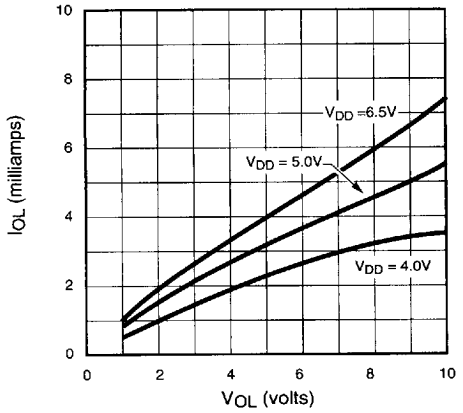


$$Tc = \frac{1}{\text{Clock Frequency}}$$

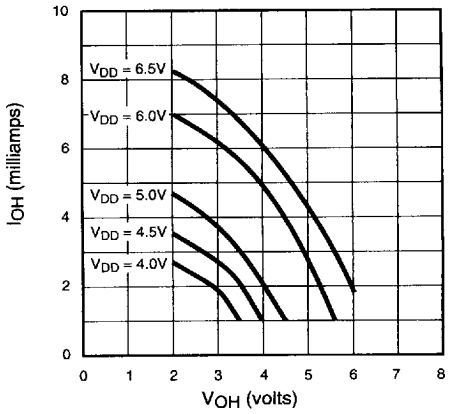
i5

Typical Performance Curves (T_A = 25°C unless otherwise noted)

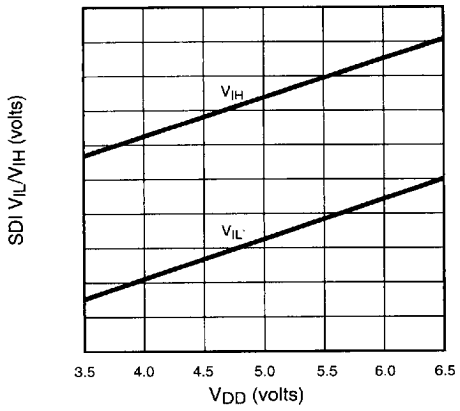
I_{OL} vs V_{DD} vs D_{OL}



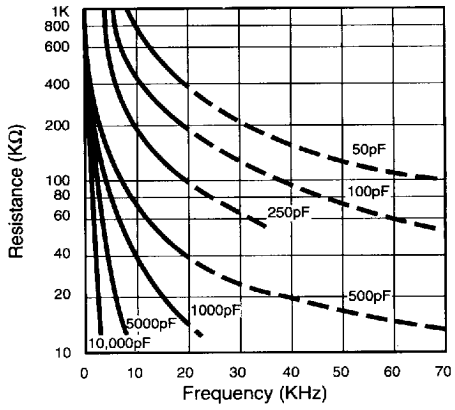
On-Resistance vs. Drain Current



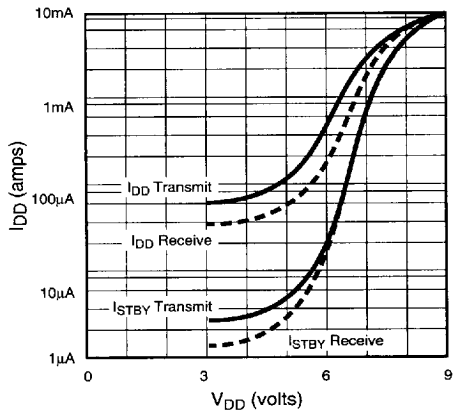
SDI Input
V_{IL}/V_{IH} vs V_{DD}



Resistance vs Oscillator Frequency – ED's



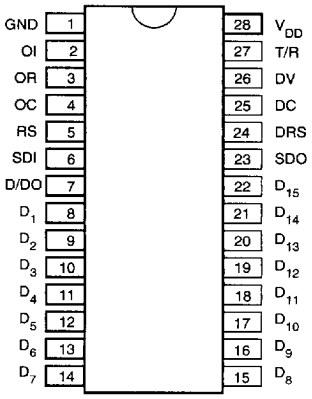
I_{DD} vs V_{DD}



Note: Operation is not guaranteed if the oscillation frequency is higher than 20KHz

Pin Configuration

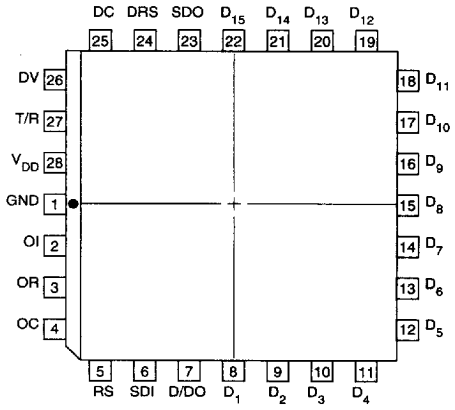
ED11 and ED15



top view

28-pin DIP

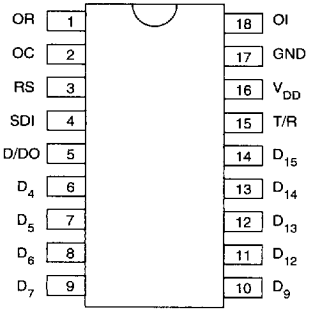
ED15



top view

28-pin J-Lead Package

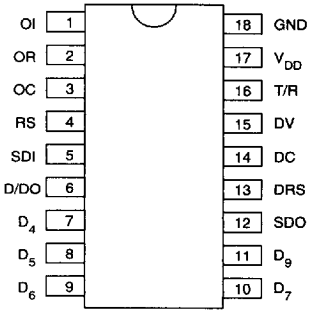
ED9



top view

18-pin DIP

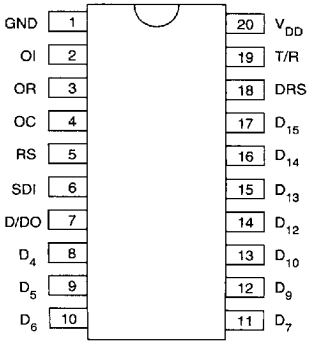
ED5



top view

18-pin DIP

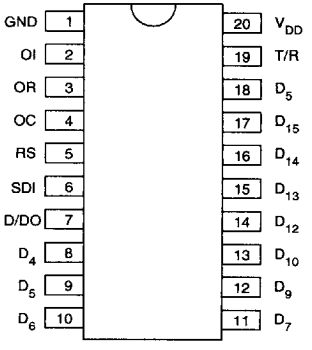
ED9



top view

20-pin DIP/SOW 20

ED10



top view

20-pin DIP/SOW 20