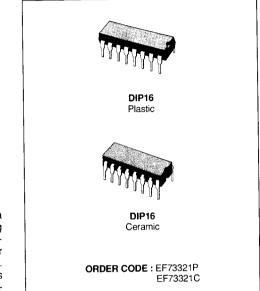
SGS-THOMSON MICROELECTRONICS

EF73321

PCM LINE TRANSCEIVER

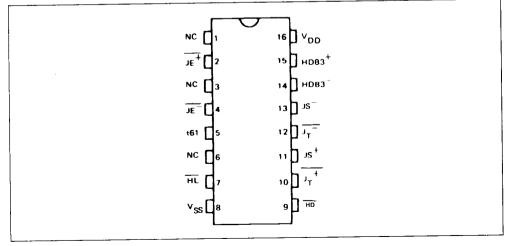
- NMOS TECHNOLOGY
- OPERATES FROM + 5 V SUPPLY
- DIGITAL TECHNOLOGY THROUGHOUT
- EXTRACTS DISTANT CLOCK TRANSMITTED BY A PCM TRUNK
- CAN HANDLE PEAK TO PEAK JITTER AMPLI-TUDE UP TO 0.25 BIT FOR AN 8-BIT PERIOD
- INTEGRATED TRANSMIT AND RECEIVE AM-PLIFIERS
- TTL-COMPATIBLE INPUT/OUTPUT



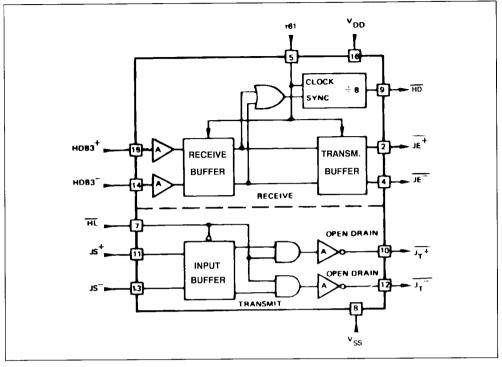
DESCRIPTION

The EF73321 provides the interface between a 2.048 or 1.544 Mbits/s PCM trunk and the switching equipment. The receiving side amplifies and reshapes the bipolar signals from a receive transformer and extracts from the signals the distant clock HD. On the transmitting side it calibrates pulses in terms of duration and amplitude by means of transistor circuits directly coupled to a transmit transformer.

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY

N°	Name	Туре	Function	Description
8	Vss	S	Supply	Ground
16	VDD	S	Зарріу	+ 5 V ± 5 %



RECEIVE

N°	Name	Туре	Function	Description
5	t61	1	-	16384 kHz or 12352 kHz Clock. Synchronises outputs JE_+ ; JE and HD.
15 14	HDB3+ HDB3-	1	Data Input	Bipolar signals in HDB3 code received from the receive transformer. The amplitude of these signals is between -5 V and $+5 \text{ V}$. Each positive pulse on HDB3+ (HDB3-) resynchronises the circuit clock and is reconstituted in calibrated form on output $JE+(JE-)$. Negative pulses have no effect on the circuit as the inputs are protected.
2 4	JE+ JE-	0 0	Data Output	Received HDB3 signals are resynchronised with $\overline{\text{HD}}$ and calibrated in terms of amplitude (TTLLS compatible levels).
9	HD	0	Distant Clock Output	The distant clock recovered from the signal on HDB3+, HBD3 The nominal frequency is 2048 kHz or 1544 kHz in the absence of jitter.

TRANSMIT

N°	Name	Туре	Function	Description
7	HL	1	Clock	Local clock, nominal frequency 2048 kHz or 1544 kHz.
11 13	JS+ JS–	1	Data Input	The data is recognised on the falling edge of HL.
10 12	- <u>T</u> + JT–	0 0	Data Output	These open drain outputs are connected to the windings of the transmit transformer. Recognition of a "1" on <u>JS</u> + (<u>JS</u> -) grounds the winding of the transformer connected to JT + (JT-) for the duration of "1" level of HL. These outputs are protected against short-circuits by current limiting internal to the circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage	$-0.3 V \le V_{DD} \le 7 V$	٧
Vi	Input Voltage Range (except inputs HDB3 + and HBD3 -)	$- 0.3 V \le V_1 \le V_{DD} + 0.3 V$	V
Р	Maximum Power	P _{max} = 250 mW in 0 °C to 70 °C Range	mW
T _{stg}	Storage Temperature Range	- 55 °C to + 150 °C	°C



FUNCTIONAL DESCRIPTION

RECEIVE PATH

The PCM Line Transceiver receives directly from the receive transformer on inputs HDB3 + and HDB3data in HDB3 code. It synchronizes this data by means of the clock on input t61 and converts <u>it to</u> voltage pulses of calibrated duration on outputs JE+ and JE-. To be recognized correctly by this circuit the received data must satisfy minimum and maximum duration conditions (Refer to timing diagrams).

Distant clock \overline{HD} is provided by a counter which divides by 8 the frequency of the clock t61. This counter is resynchronized with the data of the PCM trunk on each positive-going edge at HDB3 + or HDB3-. The period of HD may vary by 0.25 bit within a period of 8 bits without degradation of the phase relationships between JE+, JE- and HD (Cf. fig.1). If the variation occurs in an interval exceeding 4 bits but

RECEIVE TIMING DIAGRAM

Figure 1 : External Signals with Jitter < 0.25 Bit within 8-Bit Period.

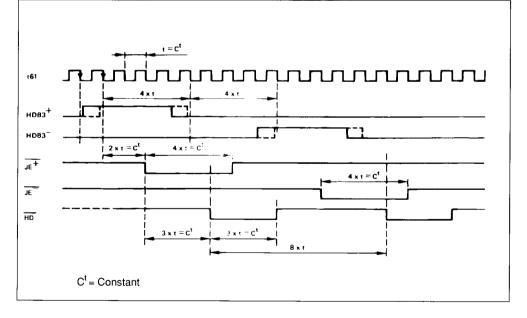
<u>less</u> than <u>8 b</u>its the phase relationships between \overline{JE} +, \overline{JE} – and \overline{HD} are modified (Cf. fig. 2 and fig. 3).

In all cases outputs \overline{JE}_+ and \overline{JE}_- remain stable on either side of the falling edge of HL so as to be sampled correctly by the EF7333.

TRANSMIT PATH

The signals JS+ and JS- to transmit are sampled on the falling edge of clock signal HL and calibrated by the duration for which this signal is high.

Open drain outputs JT+ and JT- drive the primary windings of the transmit transformer directly. They are protected against overcurrents occurring should the secondary windings of this transformer be shortcircuited, in which case the primary behaves as a very low resistance connecting the output to supply rail V_{DD}.





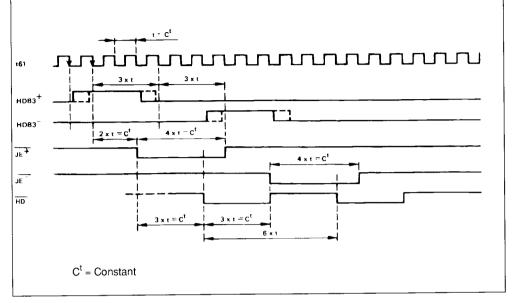
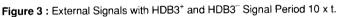
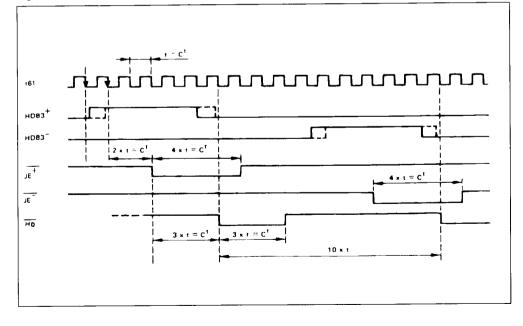


Figure 2 : External Signals with HDB3⁺ and HDB3⁻ Signal Period 6 x t.



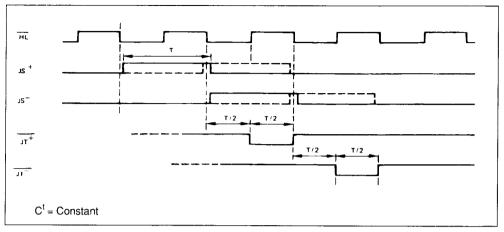


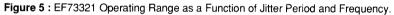


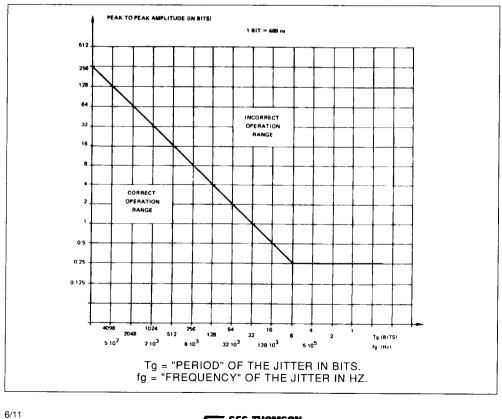
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TRANSMIT

Figure 4.







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MICROELECTROMICS

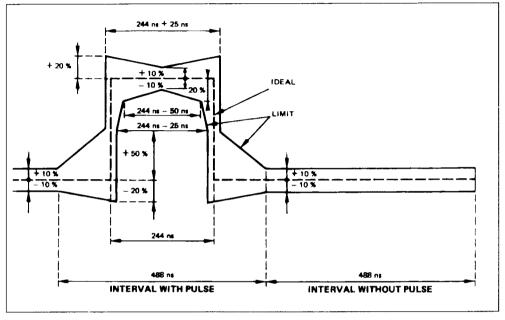
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TRANSMIT PATH

Pulse limiting curves for 2 048 kbit/s CEPT PCM trunk.

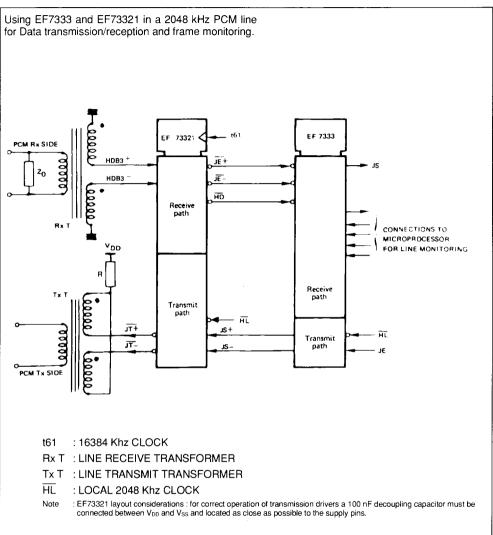
The limiting curves below are for a resistive load of 120 Ω connected across the secondary winding of the transmit transformer.

Figure 6 .





TYPICAL APPLICATION





STATIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to + 70 °C - Typical Values at + 25 °C

Symbol	Parameter	Min.	Тур.	Max.	Unit
V _{DD}	Positive Power Supply	4.75	5	5.25	V
I _{DD}	Supply Current	-	20	40	mA
	Stray Capacitance between one Input and Ground (outputs loaded with C_L = 25 pF)	_	5	10	pF

INPUTS

Symbol	Parameter	Min.	Тур.	Max.	Unit
	Voltage at Input HDB3+/HDB3 When Low When High	- 5 2.2		0.6 5	V V
	Resistance at Input HDB3+/HDB3- (inverse voltage V ₁ = - 5 V)	-	10		kΩ
	Voltage at input JS+/JS-/HL When Low When High	- 0.3 2.2		0.6 V _{DD}	V V
	Voltage at Input t61 When Low When High	0 2.6		0.6 V _{DD}	V V

OUTPUTS

Symbol	Parameter	Min.	Тур.	Max.	Unit
	Voltage at Output HD/JE+/JE-				
	When Low (I _{OL} = 0.4 mA)	0	-	0.4	V
	When High ($I_{OH} = -40 \ \mu A$)	2.6	_	VDD	V
	Voltage at Output \overline{JT} +/ \overline{JT} - when Low (R _L = 175 Ω to V _{DD})	250	450	750	mV
	Current at Output \overline{JT} +/ \overline{JT} - when High Impedance (V _{OH} = 12 V)	- T	_	100	μA
	Current at Output JT+/JT- (output current protection)	—	_	35	mA

DYNAMIC CHARACTERISTICS

Typical values at + 25 °C (0 °C < T_A < + 70 °C).

CLOCKS

Symbol	Parameter	Min.	Тур.	Max.	Unit
	Clock t61 (fig.8)		12352	_	kHz
		_	16384	16500	kHz
t _{PL}	when Low	20	_	_	ns
t _{PH}	when High	20	-		ns
	Clock HL (fig. 10)	_	1544	_	kHz
			2048	2200	kHz
t _{THL}	Fall Time	_	_	30	ns
t _{TLH}	Rise Time	-	-	30	ns



EF73321

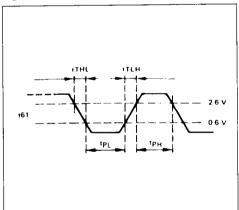
INPUTS

Symbol	Parameter	Min.	Тур.	Max.	Unit
t∺ t∟	Inputs HDB3+/HDB3- (fig. 9) Min. Pulse Duration Max. Pulse Duration	t		4 x t	ns ns
t _{set-up} thold	Inputs JS+/JS- (fig. 10) Set up Time Hold Time	20 30			ns ns

OUTPUTS

Symbol	Parameter	Min.	Тур.	Max.	Unit
t _{set-up} t _{hold} tтн⊾ tтгн	Outputs \overline{JE} +/ \overline{JE} - Relative to \overline{Hd} (CL = 25 pF, fig. 11) Set up Time Hold Time Fall Time Rise Time	150 30	3 x t t 15 20		ns ns ns ns
t _{wм}	Outputs $\overline{JT}+/\overline{JT}-$ (R _L = 175 Ω = to V _{DD} , fig. 12) Pulse Duration (C _L = 25 pF) HL = 2048 kHz	219	244	269	ns

Figure 8.



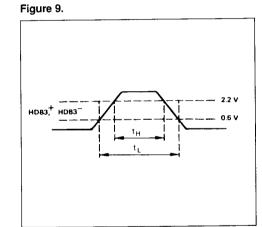




Figure 10.

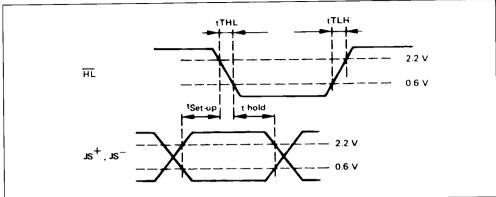


Figure 11.

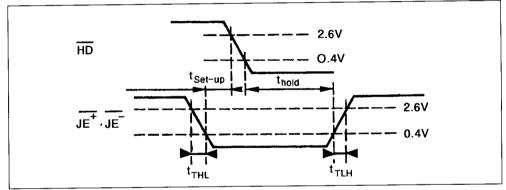
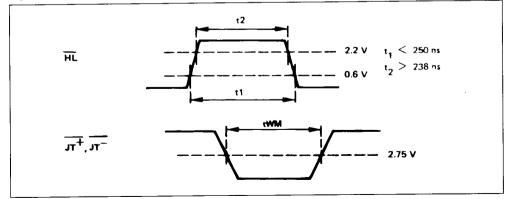
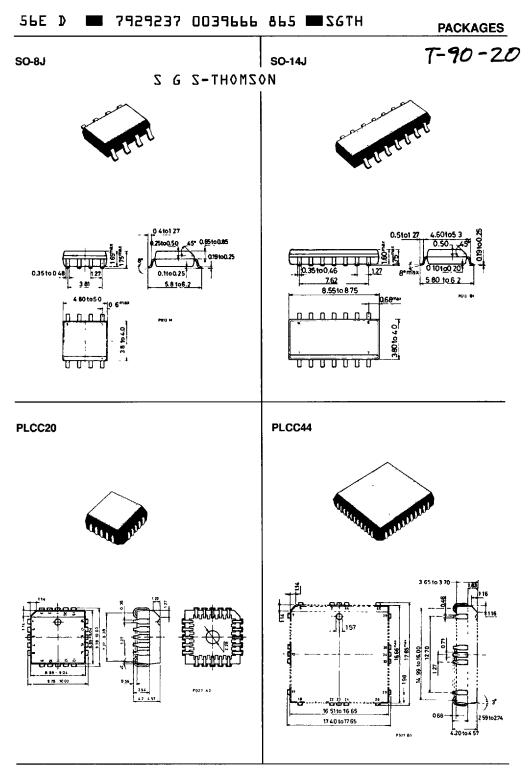
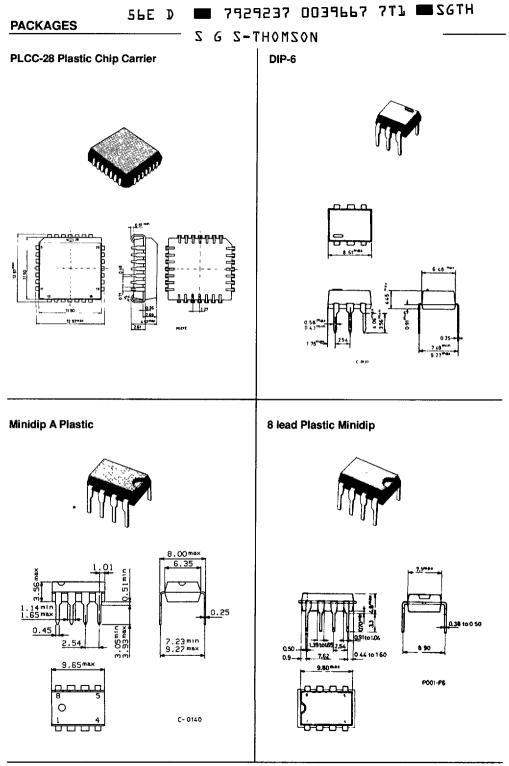


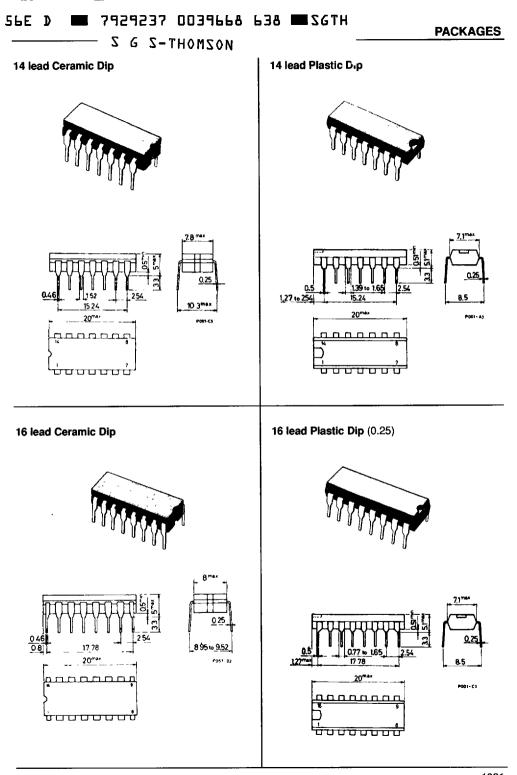
Figure 12.

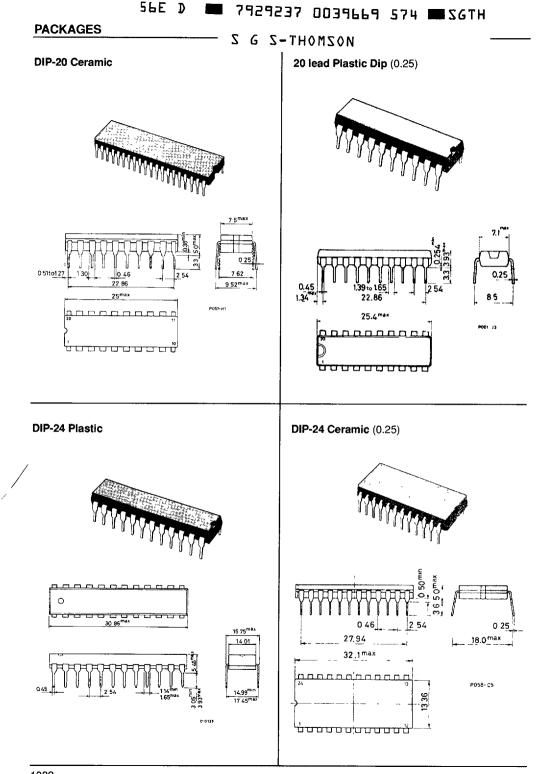


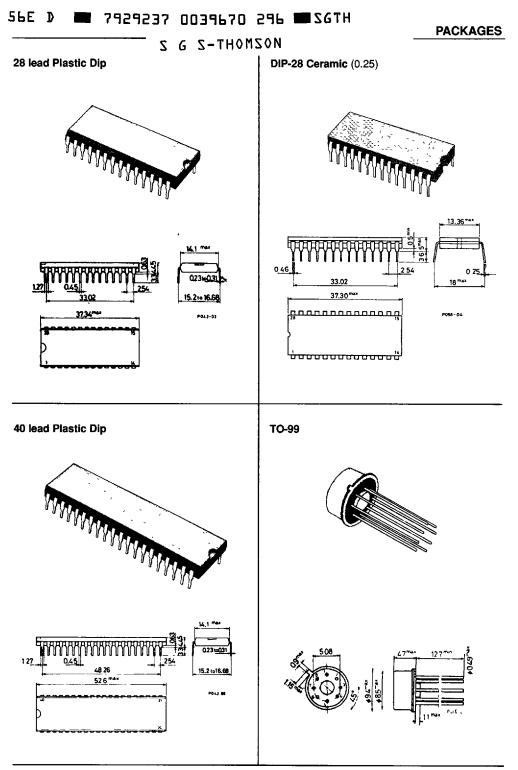










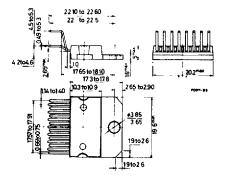


PACKAGES

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MULTIWATT-15





FLEXIWATT-15

