

élantec
 HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2001/EL2001C

Low Power, 70 MHz Buffer Amplifier

ELANTEC INC

T-52-07

Features

- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/ μ s slew rate
- Low bias current, 1 μ A typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ± 5 V to ± 15 V
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2001ACJ	0°C to +75°C	CerDIP	MDP0010
EL2001ACN	0°C to +75°C	P-DIP	MDP0031
EL2001AJ	-55°C to +125°C	CerDIP	MDP0010
EL2001AJ/883B	-55°C to +125°C	CerDIP	MDP0010
EL2001AL	-55°C to +125°C	20-Pad LCC	MDP0007
EL2001AL/883B	-55°C to +125°C	20-Pad LCC	MDP0007
EL2001CJ	0°C to +75°C	CerDIP	MDP0010
EL2001CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2001CN	0°C to +75°C	P-DIP	MDP0031
EL2001J	-55°C to +125°C	CerDIP	MDP0010
EL2001J/883B	-55°C to +125°C	CerDIP	MDP0010
EL2001L	-55°C to +125°C	20-Pad LCC	MDP0007
EL2001L/883B	-55°C to +125°C	20-Pad LCC	MDP0007

5962-9153401/2 are the SMD versions of this device.

General Description

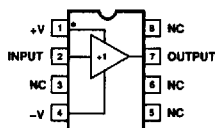
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a -3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from ± 15 V power supplies but will work with as little as ± 5 V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing, Monolithic Integrated Circuits*.

Connection Diagrams

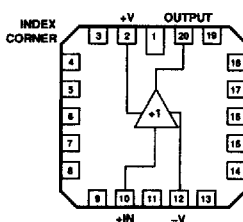
EL2001 DIP Pinout



2001-1

Top View

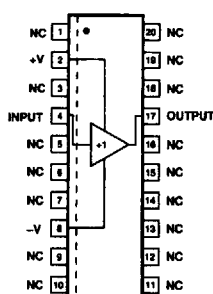
EL2001 LCC Pinout



2001-3

Top View

EL2001 SOL Pinout



2001-2

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

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EL2001/EL2001C

Low Power, 70 MHz Buffer Amplifier

EL2001/EL2001C

Absolute Maximum Ratings

V_S	Supply Voltage ($V^+ - V^-$)	$\pm 18V$ or $36V$	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage (Note 1)	$\pm 15V$ or V_S		Ceramic Packages	175°C
I_{IN}	Input Current (Note 1)	± 50 mA		Plastic Packages	150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{ST}	Storage Temperature	-65°C to +150°C
	Output Short Circuit			Lead Temperature	
	Duration (Note 3)	Continuous		DIP Package (Soldering, < 10 seconds)	300°C
T_A	Operating Temperature Range			SOL Package	
	EL2001A/EL2001	-55°C to +125°C		Vapor Phase (60 seconds)	215°C
	EL2001AC/EL2001C	0°C to +75°C		Infrared (15 seconds)	220°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$. T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2001A EL2001	EL2001AC EL2001C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	Test Level	
V_{OS}	Offset Voltage EL2001A/EL2001AC EL2001/EL2001C	0	∞	25°C	-10	2	+10	I	I	mV
				T_{MIN}, T_{MAX}	-15		+15	I	III	mV
		0	∞	25°C	-30	2	+30	I	I	mV
				T_{MIN}, T_{MAX}	-40		+40	I	III	mV
I_{IN}	Input Current EL2001A/EL2001AC EL2001/EL2001C	0	∞	25°C	-3	1	+3	I	I	μA
				T_{MIN}, T_{MAX}	-6		+6	I	III	μA
		0	∞	25°C	-5	1	+5	I	I	μA
				T_{MIN}, T_{MAX}	-10		+10	I	III	μA
R_{IN}	Input Resistance	$\pm 12V$	100 Ω	25°	3	8		I	I	M Ω
				T_{MIN}, T_{MAX}	1			I	III	M Ω

EL2001/EL2001C

ELANTEC INC

Low Power, 70 MHz Buffer Amplifier**Electrical Characteristics** $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2001A EL2001	EL2001AC EL2001C	Units
		V_{in}	Load	Temp	Min	Typ	Max	Test Level	Test Level	
A_{V1}	Voltage Gain	$\pm 12V$	∞	25°C	0.990	0.998		I	I	V/V
				T_{MIN}, T_{MAX}	0.985			I	III	V/V
A_{V2}	Voltage Gain	$\pm 10V$	100 Ω	25°C	0.83	0.93		I	I	V/V
				T_{MIN}, T_{MAX}	0.80			I	III	V/V
A_{V3}	Voltage Gain with $V_S = \pm 5V$	$\pm 3V$	100 Ω	25°C	0.82	0.89		I	I	V/V
				T_{MIN}, T_{MAX}	0.79			I	III	V/V
V_O	Output Voltage Swing	$\pm 12V$	100 Ω	25°C	± 10	± 11		I	I	V
				T_{MIN}, T_{MAX}	± 9.5			I	III	V
R_{OUT}	Output Resistance	$\pm 2V$	100 Ω	25°C		10	15	I	I	Ω
				T_{MIN}, T_{MAX}			18	I	III	Ω
I_{OUT}	Output Current	$\pm 12V$	(Note 4)	25°C	± 100	± 160		I	I	mA
				T_{MIN}, T_{MAX}	± 95			I	III	mA
I_S	Supply Current	0	∞	25°C		1.3	2.0	I	I	mA
				T_{MIN}, T_{MAX}			2.5	I	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	I	dB
				T_{MIN}, T_{MAX}	50			I	III	dB
t_r	Rise Time	0.5V	100 Ω	25°C		4.2		V	V	ns
t_d	Propagation Delay	0.5V	100 Ω	25°C		2.0		V	V	ns
SR	Slew Rate, (Note 6)	$\pm 10V$	100 Ω	25°C	1200	2000		IV	IV	V/ μ s

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds $\pm 7.5V$ then the input current must be limited to ± 50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to $\pm 12V$ and the output to $\pm 10V$ and measure the output current. Repeat with $-12V_{IN}$ and $-10V$ on the output.

Note 5: V_{OS} is measured at $V_{S+} = +4.5V$, $V_{S-} = -4.5V$ and at $V_{S+} = +18V$, $V_{S-} = -18V$. Both supplies are changed simultaneously.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

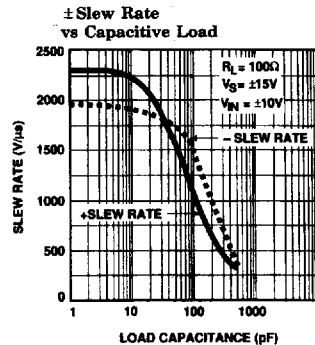
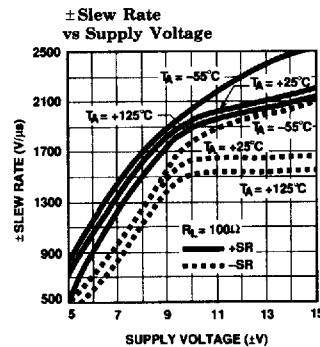
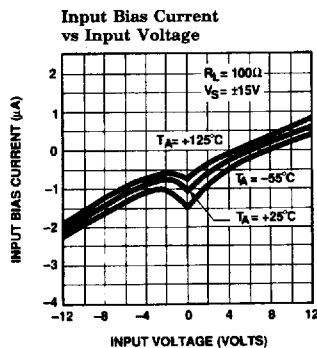
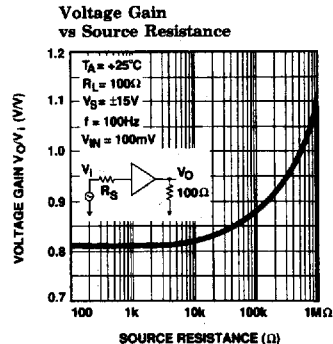
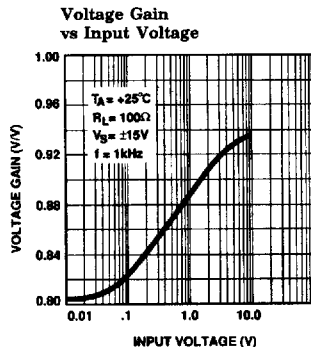
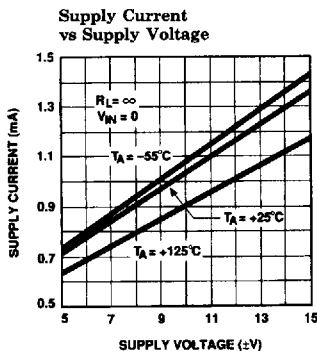
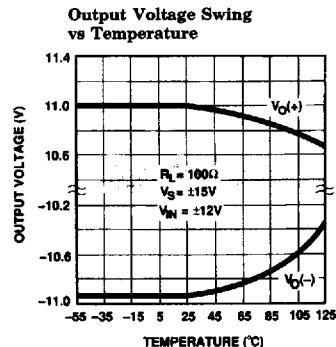
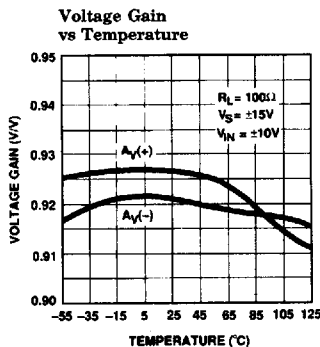
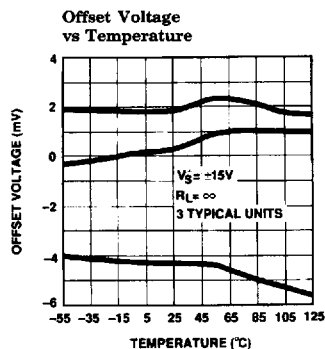
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EL2001/EL2001C

Low Power, 70 MHz Buffer Amplifier

EL2001/EL2001C

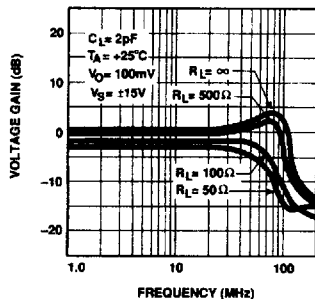
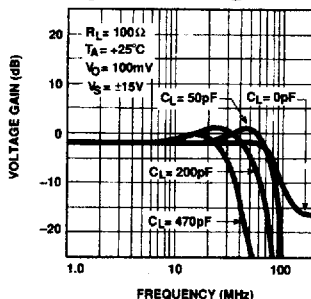
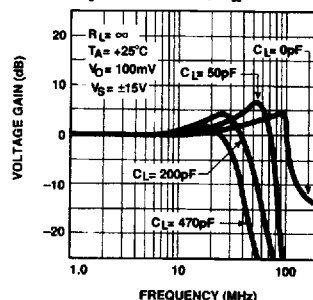
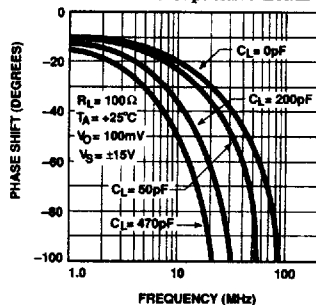
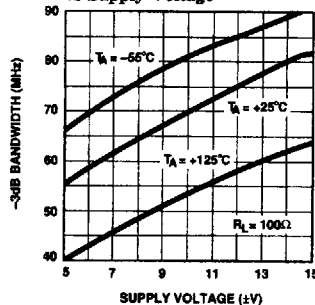
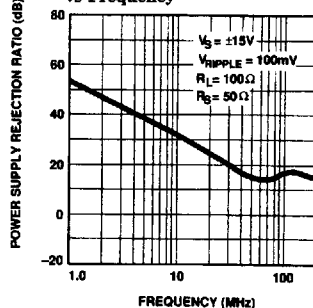
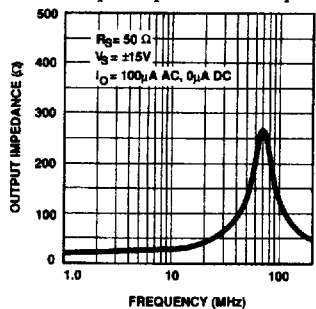
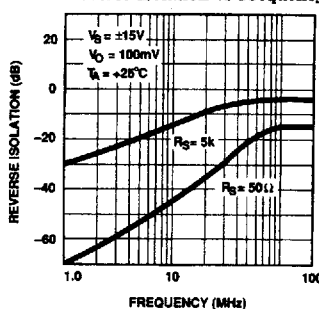
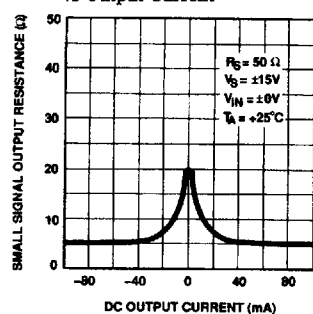
Typical Performance Curves



2001-4

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Low Power, 70 MHz Buffer Amplifier**Typical Performance Curves — Contd.****Voltage Gain vs Frequency for Various Resistive Loads****Voltage Gain vs Frequency for Various Capacitive Loads; $R_L = 100\Omega$** **Voltage Gain vs Frequency for Various Capacitive Loads; $R_L = \infty$** **Phase Shift vs Frequency for Various Capacitive Loads****-3 dB Bandwidth vs Supply Voltage****Power Supply Rejection Ratio vs Frequency****Output Impedance vs Frequency****Reverse Isolation vs Frequency****Small Signal Output Resistance vs Output Current**

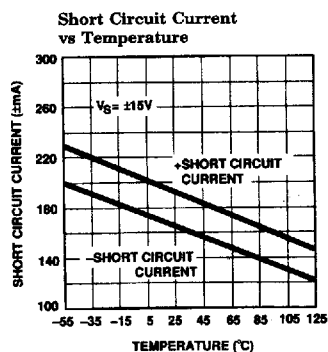
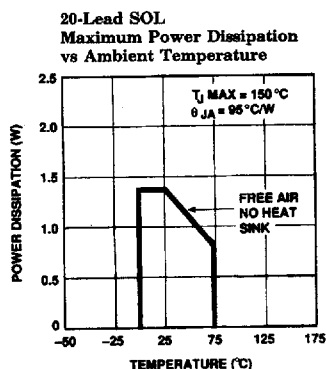
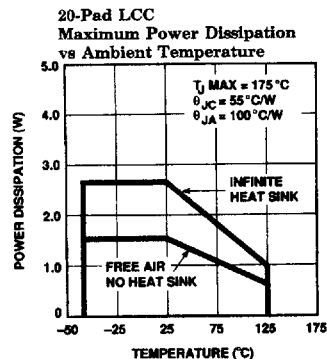
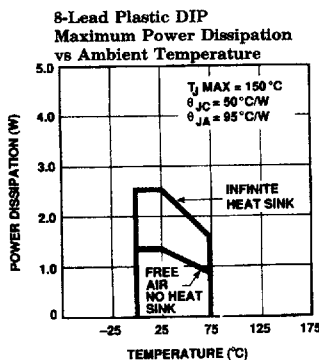
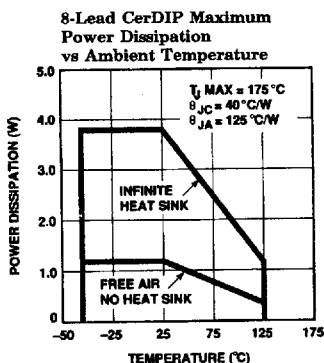
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EL2001/EL2001C

Low Power, 70 MHz Buffer Amplifier

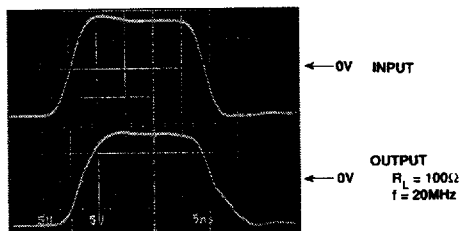
EL2001/EL2001C

Typical Performance Curves — Contd.



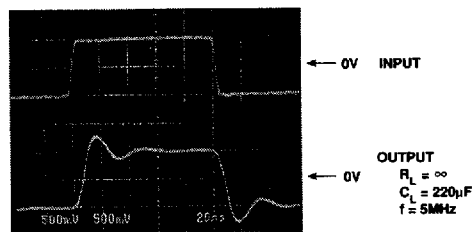
2001-6

Large Signal Response



2001-7

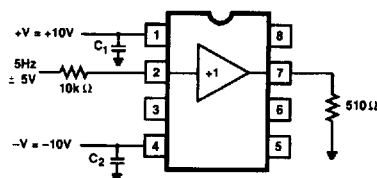
Small Signal Response



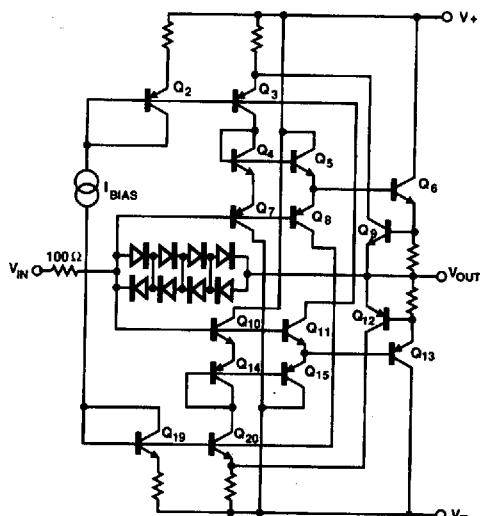
2001-8

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Low Power, 70 MHz Buffer Amplifier**Burn-In Circuit**

2001-9

Simplified Schematic

2001-10

Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/ μ s slew rates with 100 Ω loads possible with very low supply current.

Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10V (± 5 V) and 36V (± 18 V). It is not necessary to use equal split value supplies. For example -5V and +12V would be excellent for signals from -2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μ F tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ± 2.5 V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20 Ω . There is also 100 Ω in series with the input that limits input current. Above ± 7.5 V differential input to output, additional series resistance should be added.

Source Impedance

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances ($R_S > 100$ k Ω), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

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EL2001/EL2001C
Low Power, 70 MHz Buffer Amplifier

EL2001/EL2001C

EL2001 Macromodel

*Connections: + input

*				+ Vsupply
*				- Vsupply
*				output
*				

.subckt M2001 2 1 4 7

* Input Stage

el 10 0 2 0 1.0

r1 10 0 1K

rh 10 11 150

ch 11 0 9pF

rc 11 12 100

cc 12 0 4pF

e2 13 0 12 0 1.0

* Output stage

q1 4 13 14 qp

q2 1 13 15 qn

q3 1 14 16 qn

q4 4 15 19 qp

r2 16 7 1

r3 19 7 1

i1 1 14 0.9mA

i2 15 4 0.9mA

* Bias Current

iin + 2 0 1uA

* Models

.model qn npn(is = 5e-15 bf = 150 rb = 200 ptf = 45 tf = 0.1nS)

.model qp pnp(is = 5e-15 bf = 150 rb = 200 ptf = 45 tf = 0.1nS)

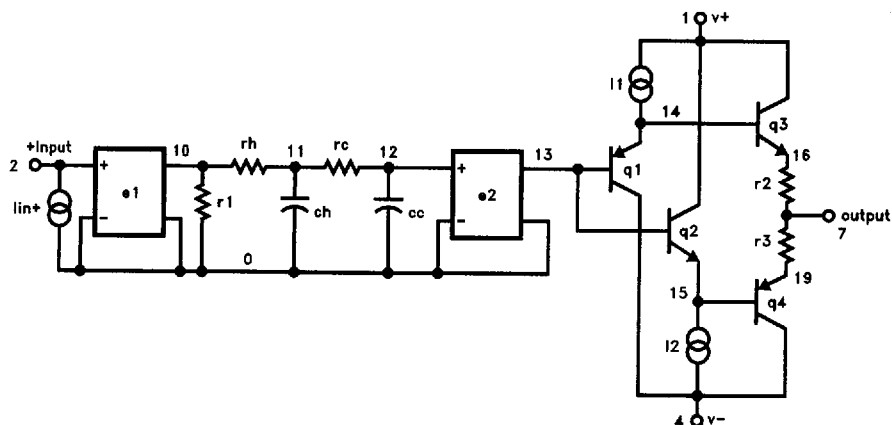
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Low Power, 70 MHz Buffer Amplifier

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EL2001 Macromodel — Contd.

2001-11