EL2125C

Ultra-Low Noise, Low Power, Wideband Amplifier

EL2125C

Features

- Voltage noise of only 0.83nV/√Hz
- Current noise of only 2.4pA/√Hz
- 200µV offset voltage
- 175MHz -3dB BW for A_V=10
- Low supply current - 10mA
- SOT-23 package available
- ±2.5V to ±15V operation

Applications

- Ultrasound input amplifiers
- Wideband instrumentation
- Communication equipment
- AGC & PLL active filters
- Wideband sensors

Ordering Information

Part No	Package	Tape & Reel	Outline #
EL2125CW-T7	5-Pin SOT-23*	7”	MDP0038
EL2125CW-T13	5-Pin SOT-23*	13”	MDP0038
EL2125CS	8-Pin SO	-	MDP0027
EL2125CS-T7	8-Pin SO	7”	MDP0027
EL2125CS-T13	8-Pin SO	13”	MDP0027

*EL2125CW symbol is .Fxxx where xxx represents date code

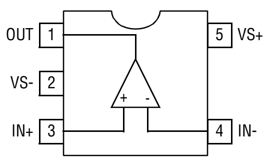
General Description

The EL2125C is an ultra-low noise, wideband amplifier that runs on half the supply current of competitive parts. It is intended for use in systems such as ultrasound imaging where a very small signal needs to be amplified by a large amount without adding significant noise. Its low power dissipation enables it to be packaged in the tiny SOT-23 package, which further helps systems where many input channels create both space and power dissipation problems.

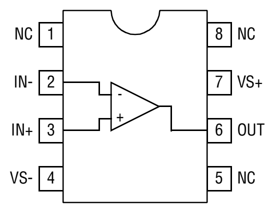
The EL2125C is stable for gains of 10 and greater and uses traditional voltage feedback. This allows the use of reactive elements in the feedback loop, a common requirement for many filter topologies. It operates from ±2.5V to ±15V supplies and is available in the 5-pin SOT-23 and 8-pin SO packages.

The EL2125C is fabricated in Elantec’s proprietary complementary bipolar process, and is specified for operation from -45°C to +85°C.

Connection Diagrams



EL2125CW
(5-Pin SOT-23)



EL2125CS
(8-Pin SO)

November 14, 2002

EL2125C

Ultra-Low Noise, Low Power, Wideband Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S+ to V_S-	33V	Operating Temperature	-45°C to +85°C
Continuous Output Current	40mA	Storage Temperature	-60°C to +150°C
Any Input	V_S- - 0.3V to V_S+ + 0.3V	Maximum Die Junction Temperature	+150°C
Power Dissipation	See Curves		

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Characteristics

V_S = ±5V, T_A = 25°C, R_F = 180Ω, R_G = 20Ω, R_L = 500Ω unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
DC Performance						
V_{OS}	Input Offset Voltage (SO8)			0.2	2	mV
	Input Offset Voltage (SOT23-5)				3	mV
T_{CVOS}	Offset Voltage Temperature Coefficient			1.8		µV/°C
I_B	Input Bias Current		-30	-22		µA
I_{OS}	Input Bias Current Offset			0.4	2	µA
T_{CIB}	Input Bias Current Temperature Coefficient			0.09		µA/°C
C_{IN}	Input Capacitance			2.2		pF
A_{VOL}	Open Loop Gain		80	87		dB
PSRR	Power Supply Rejection Ratio [1]		80	97		dB
CMRR	Common Mode Rejection Ratio	at CMIR	80	106		dB
CMIR	Common Mode Input Range		-4.6		3.8	V
V_{OUTH}	Output Voltage Swing High	No load, R_F = 1kΩ	3.5	3.65		V
V_{OUTL}	Output Voltage Swing Low	No load, R_F = 1kΩ		-3.87	-3.7	V
V_{OUTH2}	Output Voltage Swing High	R_L = 100Ω	3	3.3		V
V_{OUTL2}	Output Voltage Swing Low	R_L = 100Ω		-3.5	-3	V
I_{OUT}	Output Short Circuit Current [2]		80	100		mA
I_S	Supply Current			10.1	11	mA
AC Performance - R_G = 20Ω, C_L = 5pF						
BW	-3dB Bandwidth			175		MHz
BW ±0.1dB	±0.1dB Bandwidth			34		MHz
BW ±1dB	±1dB Bandwidth			150		MHz
Peaking	Peaking			0.4		dB
SR	Slew Rate	V_{OUT} = 2V_{PP}, measured at 20% to 80%	150	185		V/µs
OS	Overshoot, 4Vpk-pk Output Square Wave	Positive		0.6		%
		Negative		2.7		%
t_S	Settling Time to 0.1% of ±1V Pulse			42		ns
V_N	Voltage Noise Spectral Density			0.83		nV/√Hz
I_N	Current Noise Spectral Density			2.4		pA/√Hz
HD2	2nd Harmonic Distortion [3]			-74		dBc
HD3	3rd Harmonic Distortion [4]			-91		dBc

1. Measured by moving the supplies from ±4V to ±6V
2. Pulse test only
3. Frequency = 1MHz, V_{OUT} = 2Vpk-pk, into 500Ω and 5pF load

Electrical Characteristics

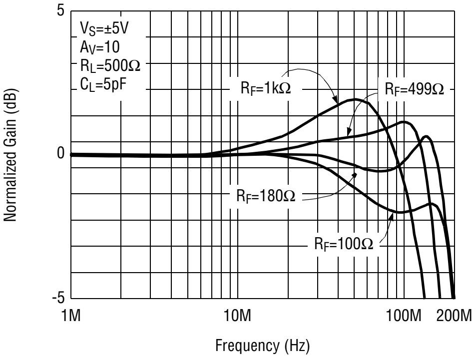
V_S = ±15V, T_A = 25°C, R_F = 180Ω, R_G = 20Ω, R_L = 500Ω unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
DC Performance						
V_{OS}	Input Offset Voltage (SO8)			0.6	3	mV
	Input Offset Voltage (SOT23-5)				3	mV
T_{CVOS}	Offset Voltage Temperature Coefficient			4.9		µV/°C
I_B	Input Bias Current		-30	-24		µA
I_{OS}	Input Bias Current Offset			0.4	2	µA
T_{CIB}	Input Bias Current Temperature Coefficient			0.08		µA/°C
C_{IN}	Input Capacitance			2.2		pF
A_{VOL}	Open Loop Gain		80	87		dB
PSRR	Power Supply Rejection Ratio [1]		80	97		dB
CMRR	Common Mode Rejection Ratio	at CMIR	75	105		dB
CMIR	Common Mode Input Range		-14.6		13.8	V
V_{OUTH}	Output Voltage Swing High	No load, R_F = 1kΩ	13.35	13.5		V
V_{OUTL}	Output Voltage Swing Low	No load, R_F = 1kΩ		-13.6	-13	V
V_{OUTH2}	Output Voltage Swing High	R_L = 100Ω	11	11.6		V
V_{OUTL2}	Output Voltage Swing Low	R_L = 100Ω		-10.4	-9.8	V
I_{OUT}	Output Short Circuit Current [2]		120	250		mA
I_S	Supply Current			10.8	12	mA
AC Performance - R_G = 20Ω, C_L = 5pF						
BW	-3dB Bandwidth			220		MHz
BW ±0.1dB	±0.1dB Bandwidth			23		MHz
BW ±1dB	±1dB Bandwidth			63		MHz
Peaking	Peaking			2.5		dB
SR	Slew Rate	V_{OUT} = 2V_{PP}, measured at 20% to 80%	180	225		V/µs
OS	Overshoot, 4Vpk-pk Output Square Wave			0.6		%
t_S	Settling Time to 0.1% of ±1V Pulse			38		ns
V_N	Voltage Noise Spectral Density			0.95		nV/√Hz
I_N	Current Noise Spectral Density			2.1		pA/√Hz
HD2	2nd Harmonic Distortion [3]			-73		dBc
HD3	3rd Harmonic Distortion [4]			-96		dBc

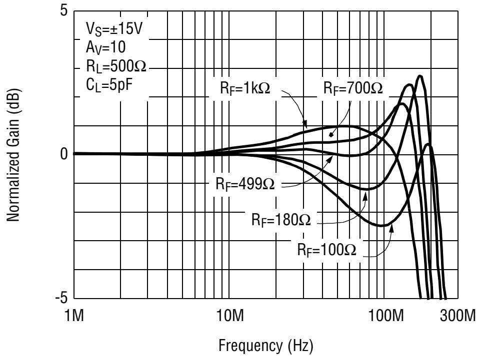
1. Measured by moving the supplies from ±13.5V to ±16.5V
2. Pulse test only
3. Frequency = 1MHz, V_{OUT} = 2Vpk-pk, into 500Ω and 5pF load

Typical Performance Curves

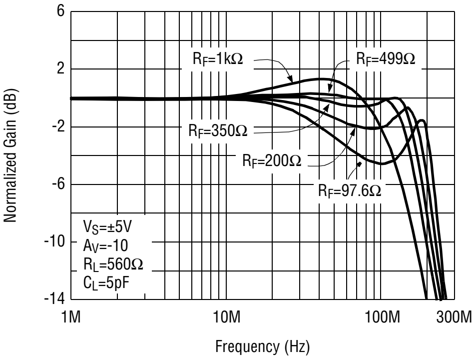
Non-Inverting Frequency Response for Various R_F



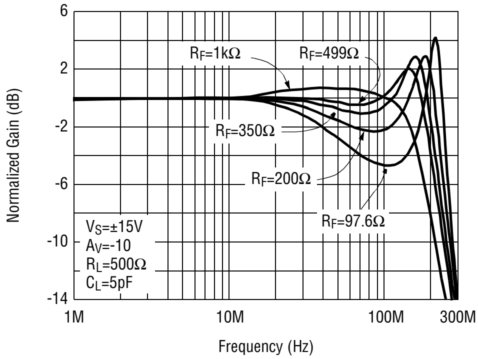
Non-Inverting Frequency Response for Various R_F



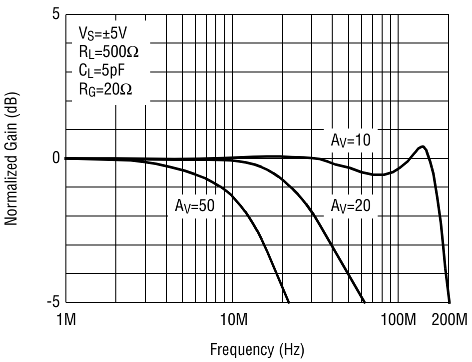
Inverting Frequency Response for Various R_F



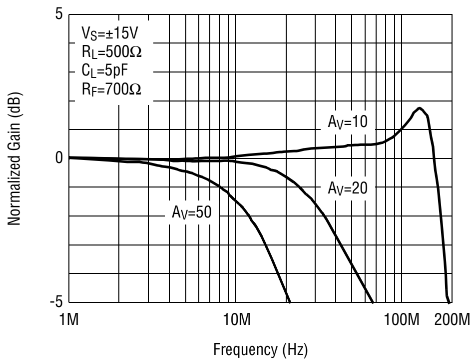
Inverting Frequency Response for Various R_F



Non-Inverting Frequency Response vs Gain



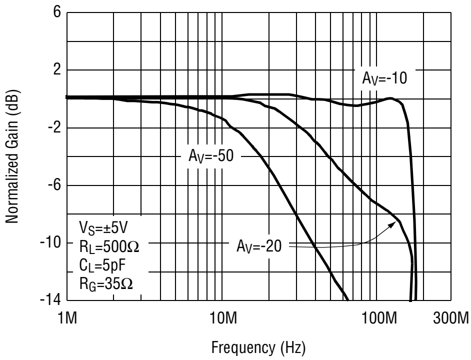
Non-Inverting Frequency Response for Various Gain



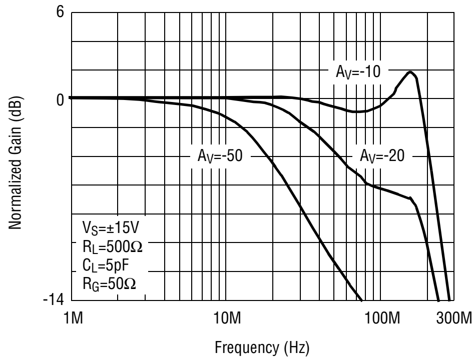
EL2125C

Typical Performance Curves

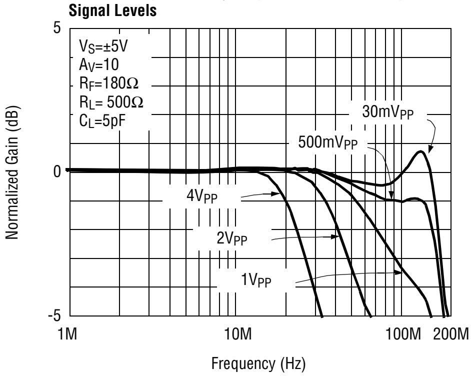
Inverting Frequency Response vs Gain



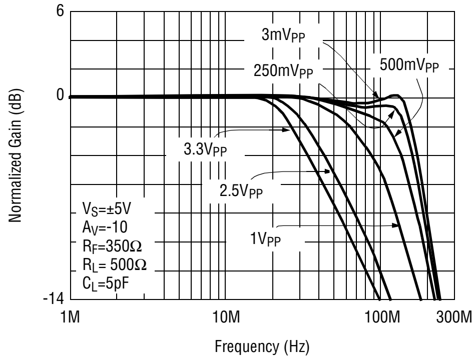
Inverting Frequency Response vs Gain



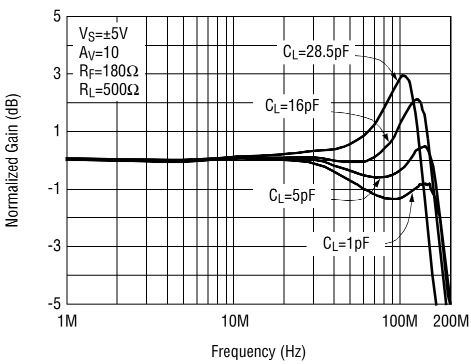
Non-Inverting Frequency Response for Various Output Signal Levels



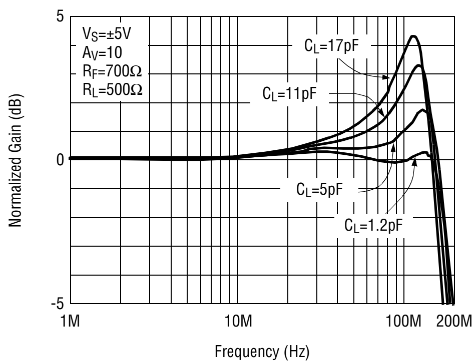
Inverting Frequency Response for Various Output Signal Levels



Non-Inverting Frequency Response for Various C_L

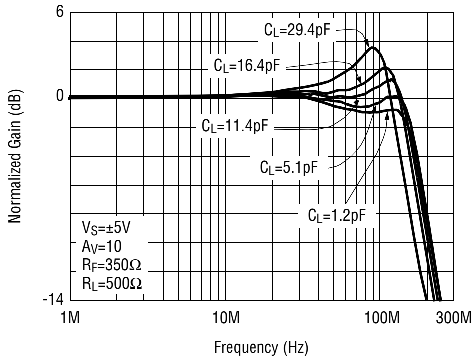


Non-Inverting Frequency Response for Various C_L

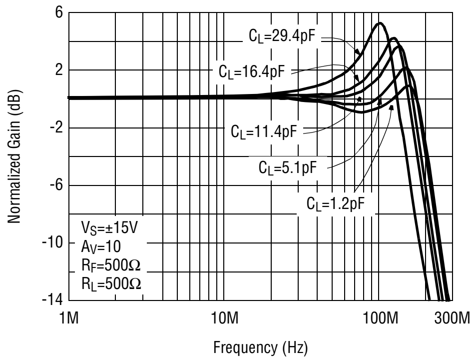


Typical Performance Curves

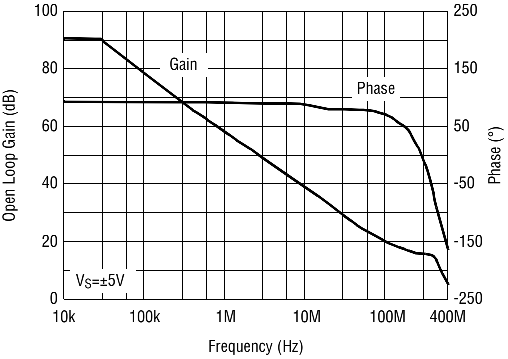
Inverting Frequency Response for Various C_L



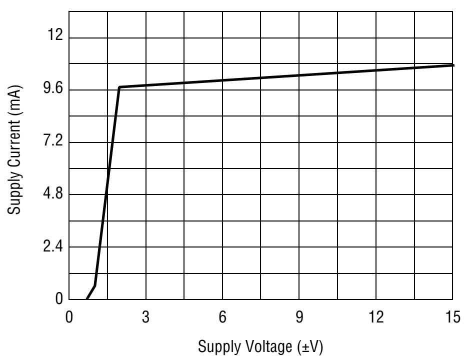
Inverting Frequency Response for Various C_L



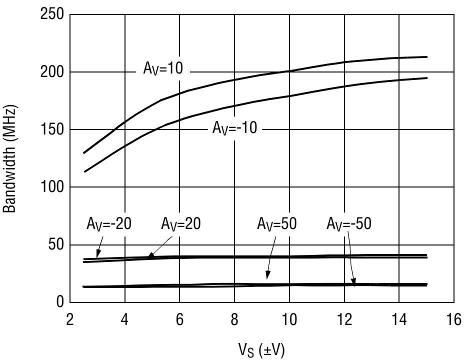
Open Loop Gain and Phase



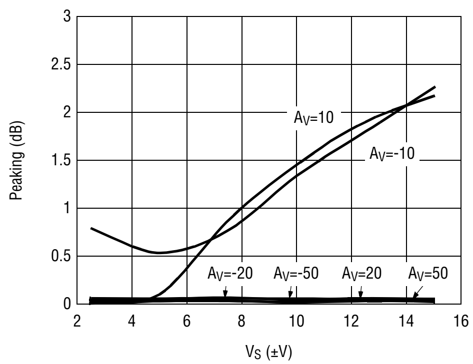
Supply Current vs Supply Voltage



3dB Bandwidth vs Supply Voltage

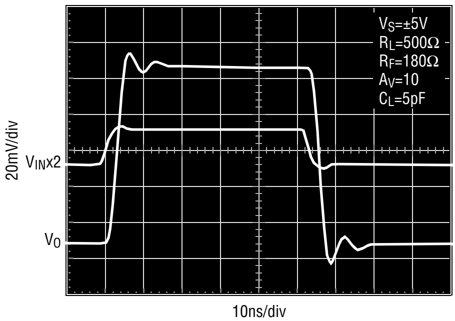


Peaking vs Supply Voltage

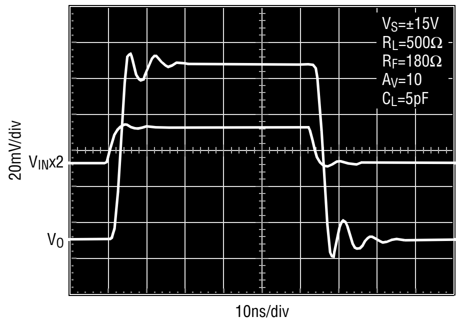


Typical Performance Curves

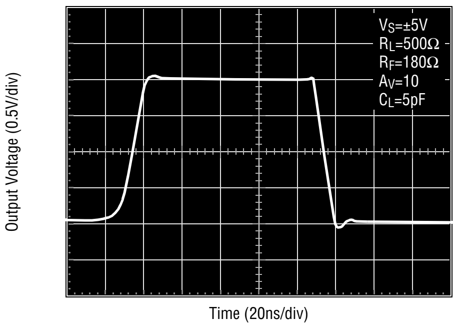
Small Signal Step Response



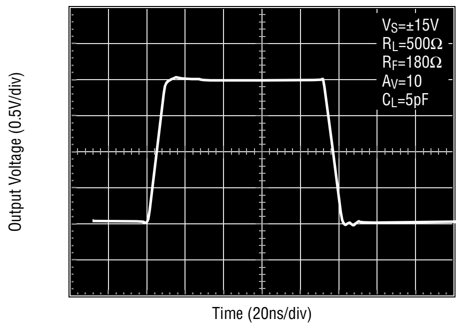
Small Signal Step Response



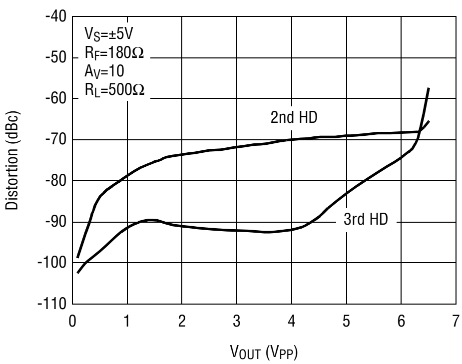
Large-Signal Step Response



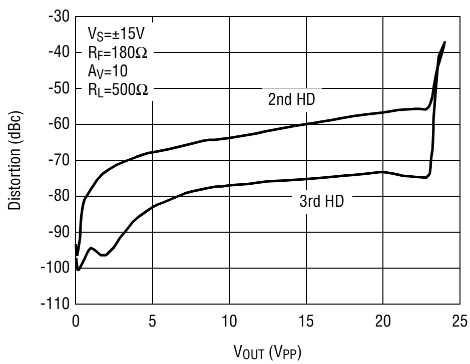
Large-Signal Step Response



1MHz Harmonic Distortion vs Output Swing

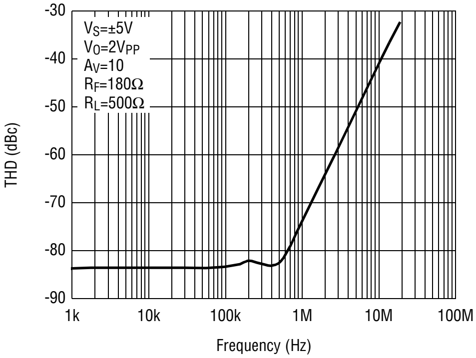


1MHz Harmonic Distortion vs Output Swing

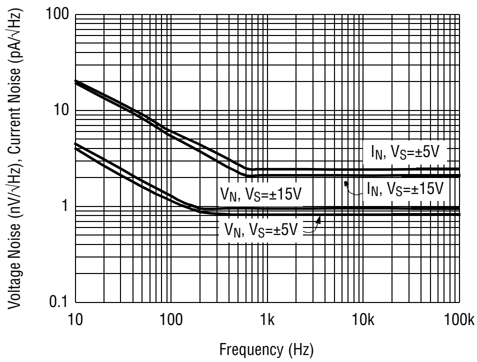


Typical Performance Curves

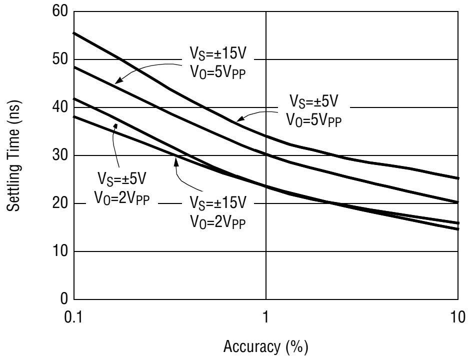
Total Harmonic Distortion vs Frequency



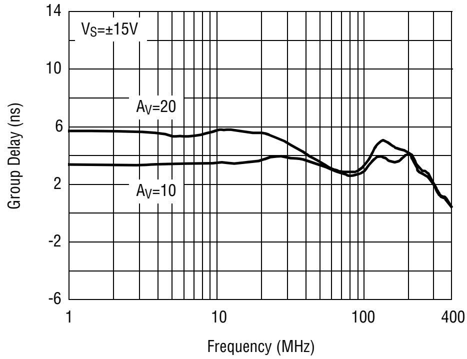
Voltage and Current Noise vs Frequency



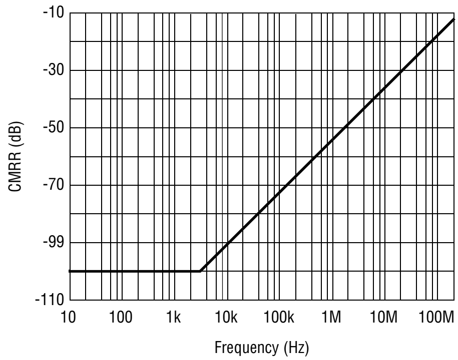
Settling Time vs Accuracy



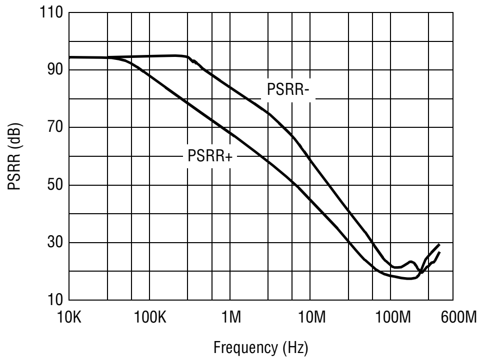
Group Delay



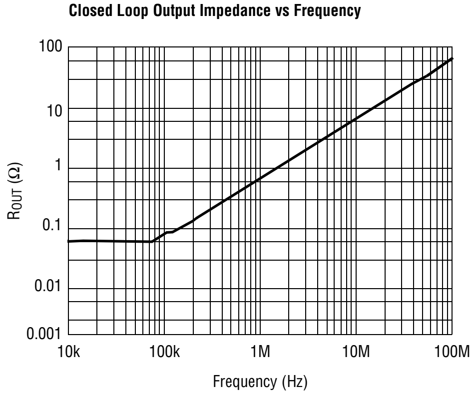
CMRR

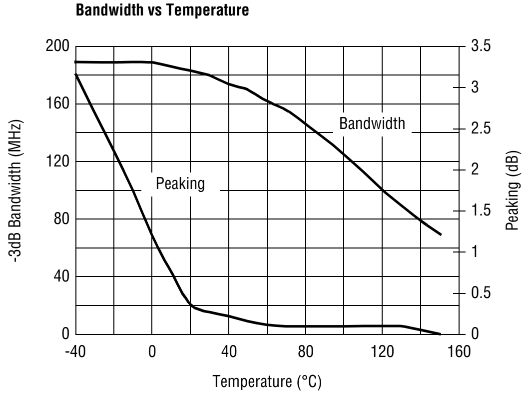


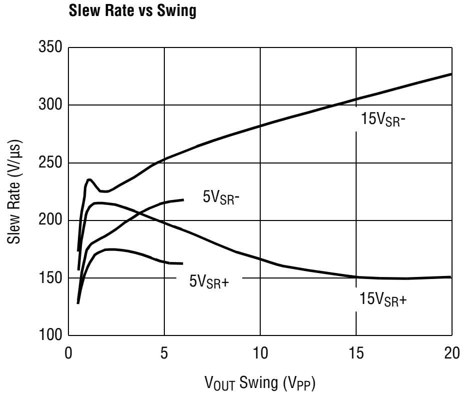
PSRR

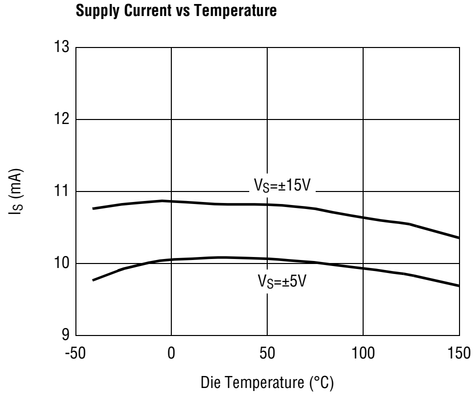


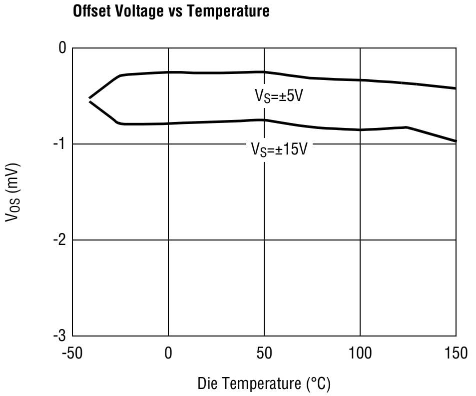
Typical Performance Curves

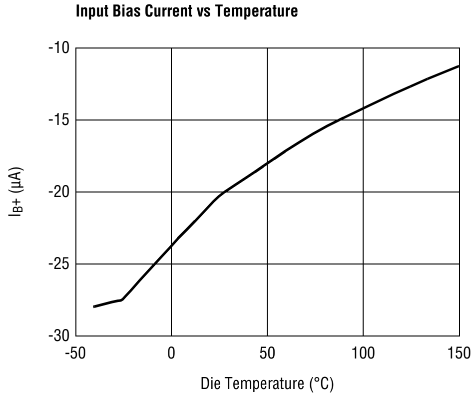






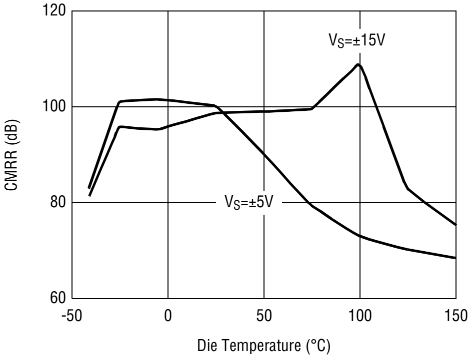




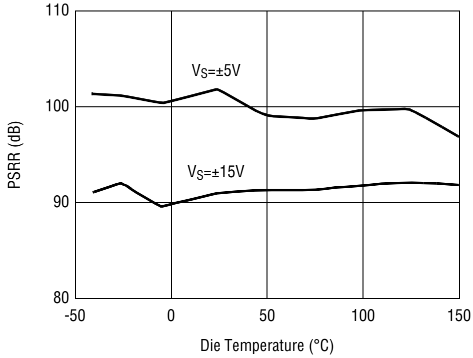


Typical Performance Curves

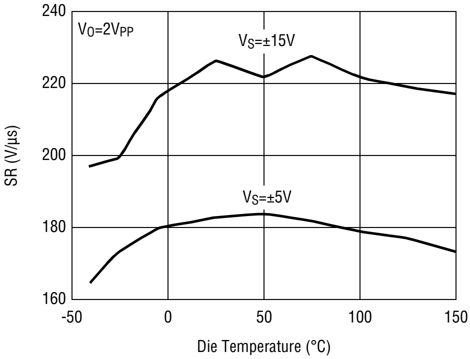
CMRR vs Temperature



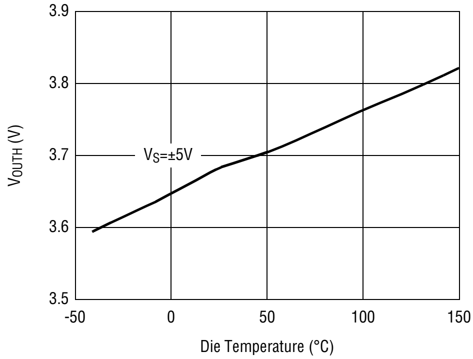
PSRR vs Temperature



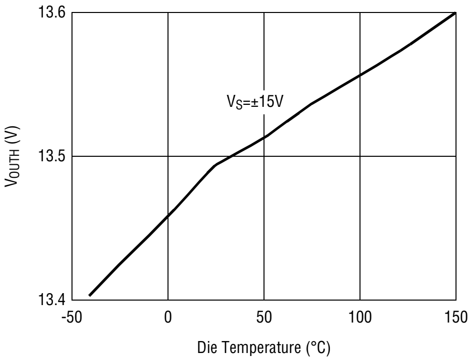
Slew Rate vs Temperature



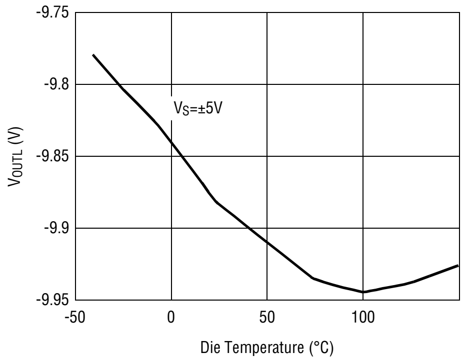
Positive Output Swing vs Temperature



Positive Output Swing vs Temperature

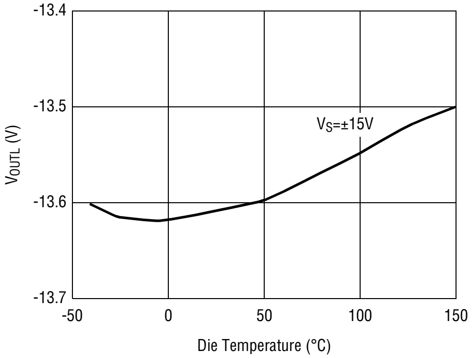


Negative Output Swing vs Temperature

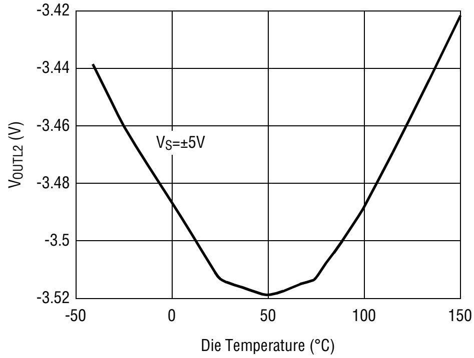


Typical Performance Curves

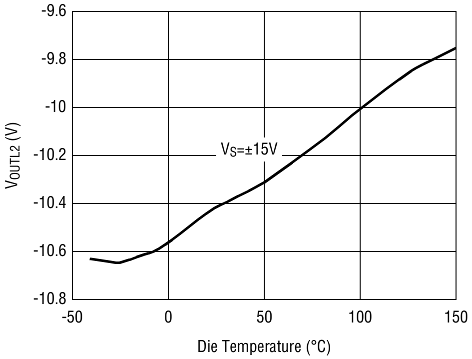
Negative Output Swing vs Temperature



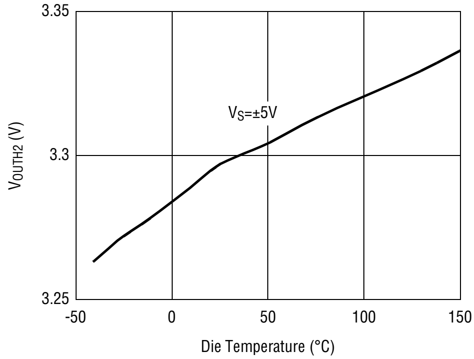
Loaded Negative Output Swing vs Temperature



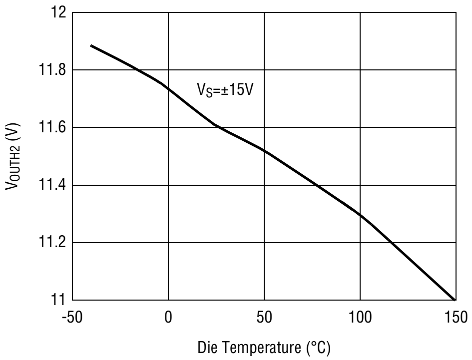
Negative Output Swing vs Temperature



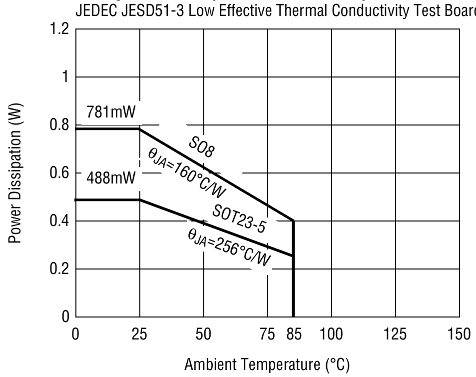
Loaded Positive Output Swing vs Temperature



Loaded Positive Output Swing vs Temperature



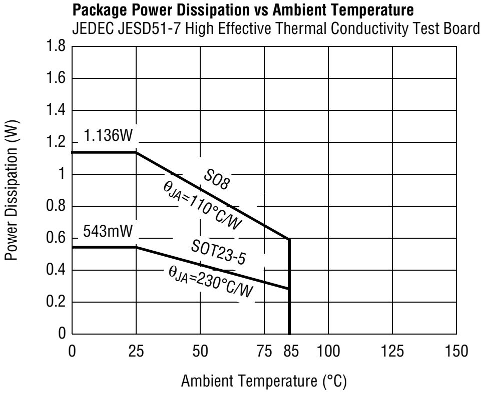
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 Low Effective Thermal Conductivity Test Board



EL2125C

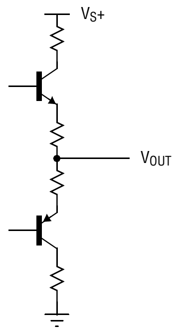
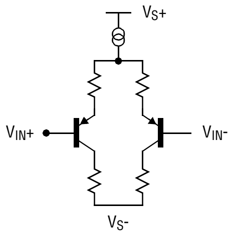
Ultra-Low Noise, Low Power, Wideband Amplifier

Typical Performance Curves



EL2125C

Pin Descriptions

EL2125CW (5-Pin SOT-23)	EL2125CS (8-Pin SO)	Pin Name	Pin Function	Equivalent Circuit
1	6	VOUT	Output	 Circuit 1
2	4	VS-	Supply	
3	3	VINA+	Input	 Circuit 2
4	2	VINA-	Input	Reference Circuit 2
5	7	VS+	Supply	

Applications Information

Product Description

The EL2125C is an ultra-low noise, wideband monolithic operational amplifier built on Elantec's proprietary high speed complementary bipolar process. It features 0.83nV/√Hz input voltage noise, 200µV offset voltage, and 73dB THD. It is intended for use in systems such as ultrasound imaging where very small signals are needed to be amplified. The EL2125C also has excellent DC specifications: 200µV V_{OS}, 22µA IB, 0.4µA I_{OS}, and 106dB CMRR. These specifications allow the EL2125C to be used in DC-sensitive applications such as difference amplifiers.

Gain-Bandwidth Product

The EL2125C has a gain-bandwidth product of 800MHz at ±5V. For gains greater than 20, its closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the small signal gain of the circuit. For gains less than 20, higher-order poles in the amplifier's transfer function contribute to even higher closed-loop bandwidths. For example, the EL2125C has a -3dB bandwidth of 175MHz at a gain of 10 and decreases to 40MHz at gain of 20. It is important to note that the extra bandwidth at lower gain does not come at the expenses of stability. Even though the EL2125C is designed for gain > 10 with external compensation, the device can also operate at lower gain settings. The RC network shown in Figure 1 reduces the feedback gain at high frequency and thus maintains the amplifier stability. R values must be less than RF divided by 9 and 1 divided by 2πRC must be less than 400MHz.

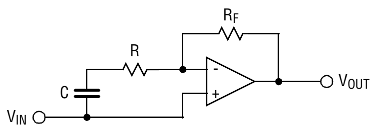


Figure 1.

Choice of Feedback Resistor, RF

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, RF has some maximum value which should not be exceeded for optimum performance. If a large value of RF must be used, a small capacitor in the few pF range in parallel with RF can help to reduce this ringing and peaking at the expense of reducing the bandwidth. Frequency response curves for various RF values are shown the in typical performance curves section of this data sheet.

Noise Calculations

The primary application for the EL2125C is to amplify very small signals. To maintain the proper signal-to-noise ratio, it is essential to minimize noise contribution from the amplifier. Figure 2 below shows all the noise sources for all the components around the amplifier.

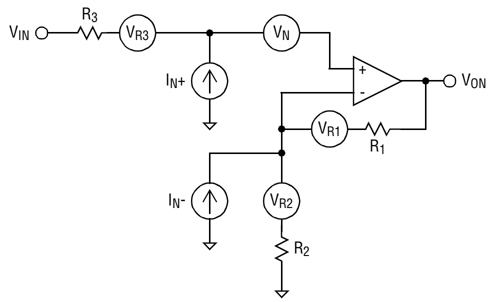


Figure 2.

V_N is the amplifier input voltage noise

I_N+ is the amplifier positive input current noise

I_N- is the amplifier negative input current noise

V_{RX} is the thermal noise associated with each resistor:

$$V_{RX} = \sqrt{4kTRx}$$

where:

- k is Boltzmann's constant = 1.380658×10^{-23}
- T is temperature in degrees Kelvin (273+ °C)

The total noise due to the amplifier seen at the output of the amplifier can be calculated by using the following equation:

$$V_{ON} = \sqrt{BW} \times \sqrt{\left(VN^2 \times \left(1+\frac{R_1}{R_2}\right)^2 + IN\text{-}^2 \times R_1^{\,2} + IN\text{+}^2 \times R_3^{\,2} \times \left(1+\frac{R_1}{R_2}\right)^2 + 4 \times K \times T \times R_1 + 4 \times K \times T \times R_2 \times \left(\frac{R_1}{R_2}\right)^2 + 4 \times K \times T \times R_3 \times \left(1+\frac{R_1}{R_2}\right)^2\right)}$$

As the above equation shows, to keep noise at a minimum, small resistor values should be used. At higher amplifier gain configuration where R_2 is reduced, the noise due to IN-, R_2, and R_1 decreases and the noise caused by IN+, VN, and R_3 starts to dominate. Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be ignored. This can greatly simplify the formula and make noise calculation much easier to calculate.

Output Drive Capability

The EL2125C is designed to drive low impedance load. It can easily drive $6V_{P-P}$ signal into a 100Ω load. This high output drive capability makes the EL2125C an ideal choice for RF, IF, and video applications. Furthermore, the EL2125C is current-limited at the output, allowing it to withstand momentary short to ground. However, the power dissipation with output-shorted cannot exceed the power dissipation capability of the package.

Driving Cables and Capacitive Loads

Although the EL2125C is designed to drive low impedance load, capacitive loads will decreases the amplifier's phase margin. As shown the in the performance curves, capacitive load can result in peaking, overshoot and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated with a series resistor between 5Ω to 20Ω. When driving coaxial cables, double termination is always recommended for reflection-free performance. When properly terminated, the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency devices, good printed circuit board layout is essential for optimum performance. Ground plane construction is highly recommended. Lead lengths should be kept as short as possible. The power supply pins must be closely bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with 0.1µF ceramic capacitor has been proven to work well when placed at each supply pin. For single supply operation, where pin 4 (V_S-) is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor across pins 7 (V_S+) and pin 4 (V_S-) will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction again should be used. Small chip resistors are recommended to minimize series inductance. Use of sockets should be avoided since they add parasitic inductance and capacitance which will result in additional peaking and overshoot.

Supply Voltage Range and Single Supply Operation

The EL2125C has been designed to operate with supply voltage range of ±2.5V to ±15V. With a single supply, the EL2125C will operate from +5V to +30V. Pins 4 and 7 are the power supply pins. The positive power supply is connected to pin 7. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

As the power supply voltage decreases from +30V to +5V, it becomes necessary to pay special attention to the input voltage range. The EL2125C has an input voltage range of 0.4V from the negative supply to 1.2V from the positive supply. So, for example, on a single +5V supply, the EL2125C has an input voltage range which spans from 0.4V to 3.8V. The output range of the EL2125C is also quite large, on a +5V supply, it swings from 0.4V to 3.6V.

EL2125C

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Effective May 15, 2002, Elantec, a leader in high performance analog products, is now a part of Intersil Corporation.

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