EL400/EL400C T.79.07-10 200 MHz Current Feedback Amplifier

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Features

- 200 MHz -3 dB bandwidth, $A_V = 2$
- 12 ns settling to 0.05%
- $V_S = \pm 5V @ 15 mA$
- Low distortion: HD2, HD3 @ -60 dBc at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- ±1 to ±8 closed-loop gain range
- Low cost
- Direct replacement for CLC400

Applications

- · Video gain block
- Video distribution
- HDTV amplifier
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Tem	p. Ras	nge	P	ackage	Outl	ine #
EL400CN	-40°C	to +8	35°C	8-P	in P-DIP	MD	P0031
EL400CS	-40°C	to +8	35°C	8-1	Lead SO	MD:	P0027
EL400J/883E	3 – 55°C	to +1	25°C	8-Pi	n CerDIP	MD	P0010
5962-89970 device.	001 is	the	SM	ID	version	of	this

General Description

The EL400 is a wide bandwidth, fast settling monolithic amplifier built using an advanced complementary bipolar process. This amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ± 1 to ± 8 , the EL400 has a 200 MHz -3 dB bandwidth (A_V = +2), and 12 ns settling to 0.05% while consuming only 15 mA of supply current.

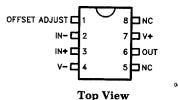
The EL400 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current, differential gain/phase of 0.02%/0.01°, and a minimum 50 mA output drive, performance in these areas is assured.

The EL400's settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL400, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: Elantec's Military Processing, Monolithic Integrated Circuits.

Connection Diagram

DIP and SO Package



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Absolute Maximum Ratings (TA = 25°C)

Supply Voltage (V_S)

 $\pm 7V$

Output Current

Output is short-circuit protected to ground, however, maximum reliability is obtained if

I_{OUT} does not exceed 70 mA.

Common-Mode Input Voltage Differential Input Voltage ±V_S 5V See Curves

Power Dissipation

Operating Temperature

EL400 EL400C -55°C to +125°C -40C to +85C Lead Temperature (Soldering, 5 Seconds)

Junction Temperature
Storage Temperature
Thermal Resistance

 300° C 175° C -60° C to $+150^{\circ}$ C $\theta_{JA} = 95^{\circ}$ C/W P-DIP $\theta_{JA} = 125^{\circ}$ C/W CerDIP $\theta_{JA} = 175^{\circ}$ C/W SO-8

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore T_J = T_C = T_A.

Test Level I

п

Test Procedure

100% production tested and QA sample tested per QA test plan QCX0002.

100% production tested at $T_A=25^{\circ}\mathrm{C}$ and QA sample tested at $T_A=25^{\circ}\mathrm{C}$,

T_{MAX} and T_{MIN} per QA test plan QCX0002.

III QA sample tested per QA test plan QCX0002.

IV Parameter is guaranteed (but not tested) by Design and Characterization Data.

V Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics $V_S = \pm 5V$, $R_L = 100\Omega$ unless otherwise specified

	D	Test	Temp Min	Min	Тур	Max	Test Level		Units
Parameter	Description	Conditions	remp	141111	тур	Max	EL400	ELAGOC II III III III III III III III III I	CIII
v _{os}	Input Offset Voltage		25°C		2.0	5.5	1	1	mV
00			T _{MIN}			8.7	1	ELAOCC I III III III III III III III III II	mV
			T _{MAX}			9.5	1		mV
d(V _{OS})/dT	Average Offset Voltage Drift	(Note 1)	All		10.0	40.0	ΙV	ΤV	μV/°C
+ I _{IN}	+ Input Current		25°C, T _{MAX}		10.0	25.0	1	11	μΑ
			T _{MIN}			41.0	1	Ш	μΑ
$d(+I_{IN})/dT$	Average + Input Current Drift	(Note 1)	All		50.0	200.0	IV	IV	nA/°C
-I _{IN}	-Input Current		25°C		10.0	25.0	1	1	μA
			T _{MIN}			41.0	1	ELAOOC I III III III III III III III III I	μΑ
			T _{MAX}			35.0	1		μΑ
$d(-I_{IN})/dT$	Average — Input Current Drift	(Note 1)	All		100.0	200.0	ΙV	IV	nA/°C
PSRR	Power Supply Rejection Ratio		All	40.0	50.0		1	π	dB
CMRR	Common-Mode Rejection Ratio		All	40.0	50.0		1	п	dB
I _S	Supply Current—Quiescent	No Load	All		15.0	23.0	1	п	mA

200 MHz Current Feedback Amplifier

Open Loop DC Electrical Characteristics

 $V_S = \pm 5V$, $R_L = 100\Omega$ unless otherwise specified — Contd.

Parameter	Description	Test	Temp	Min	Тур Мах	Mov	Test Level		Units
	Description	Conditions	Temp	WAITI		EL400	EL400C		
+R _{IN}	+Input Resistance		25°C, T _{MAX}	100.0	200.0		I	11	kΩ
			T _{MIN}	50.0			1	111	kΩ
C _{IN}	Input Capacitance		All		0.5	2.0	IV	IV	pF
R _{OUT}	Output Impedance (DC)		All		0.1	0.2	IV	IV	Ω
CMIR	Common-Mode Input	(Note 2)	25°C, T _{MAX}	2.0	2.1		IV	EL400C II III IV IV IV IV II III III V V	v
	Range		T _{MIN}	1.2			· IV	IV	v
I _{OUT}	Output Current		25°C, T _{MAX}	50.0	70.0		1	n	mA
			T _{MIN}	35.0			1	ш	mA
V _{OUT}	Output Voltage Swing	No Load	Ali	3.2	3.5		1	п	v
V _{OUT} L	Output Voltage Swing	100Ω	25°C	3.0	3.4		1	1	v
R _{OL}	Transimpedance		25°C	30.0	125,0		I	11	V/mA
			T _{MIN}		80.0		v	٧	V/mA
			T _{MAX}		140.0		v	V IV V IV V IV V IV II II I II I II V V	V/mA

Closed-Loop AC Electrical Characteristics

 $V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test	Temp	Min	Тур	Max	Test Level		Units
rarameter	Description	Conditions	Temp		130		EL400	EL400C	Cirius
FREQUENCY	RESPONSE								
SSBW	-3 dB Bandwidth		25°C	150.0	200.0		I	ш	MHz
	$(V_{OUT} < 0.5 V_{PP})$		T _{MIN}	150.0			14	EL400C	MHz
			T _{MAX}	120.0			IV	IV	MHz
LSBW	-3 dB Bandwidth (V _{OUT} < 5.0 V _{PP})	$A_{V} = +5$	All	35.0	50.0		IV	īV	MHz
GAIN FLATI	NESS								
GFPL	Peaking	<40 MHz	25°C		0.0	0.3	1	111	dB
	$V_{OUT} < 0.5 V_{PP}$		T _{MIN} , T _{MAX}			0.4	IV	IV	đВ
GFPH	Peaking	>40 MHz	25°C		0.0	0.5	1	ш	dB
	$V_{\rm OUT} < 0.5 V_{\rm PP}$		T _{MIN} , T _{MAX}			0.7	IV	IV	dВ
GFR	Rolloff	<75 MHz	25°C		0.6	1.0	1	111	dΒ
	$V_{OUT} < 0.5 V_{PP}$		T _{MIN}			1.0	IV	IV	dB
			T _{MAX}			1.3	IV	IV	dΒ
LPD	Linear Phase Deviation	<75 MHz	25°C, T _{MIN}		0.2	1.0	īV	IV	۰
	$V_{OUT} < 0.5 V_{PP}$		T _{MAX}			1.2	IV	IV	۰

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200 MHz Current Feedback Amplifier

Closed-Loop AC Electrical Characteristics — Contd. $V_S=\pm5V, R_F=250\Omega, A_V=+2, R_L=100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Тур	Max			Units
TIME-DOM	AIN RESPONSE		<u> </u>	L	l ana 	L			
t _{r1} , t _{f1}	Rise Time, Fall Time	0.5V Step	25°C, T _{MIN}		1.6	2.4	ΙV	ΙV	ns
			T _{MAX}			2.9	IA	IV I	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	A 11		6.5	10.0	ΙV	IV	ns
t _{s1}	Settling Time to 0.1%	2.0V Step	All		10.0	13.0	īV	IV	ns
t _{s2}	Settling Time to 0.05%	2.0V Step	All		12.0	15.0	TV	IV	ns
os	Overshoot	0.5V Step	25°C		0.0	10.0	IV	IV	%
			T _{MIN} , T _{MAX}			15.0	IV	IV	%
SR	Slew Rate	$A_V = +2$	All	430.0	700.0		ΙΛ	IV	V/μs
		$A_V = -2$	All		1600.0		٧	v	V/μs
DISTORTIC)N								
HD2	2nd Harmonic Distortion at 20 MHz	2 V _{PP}	25°C		-60.0 -	-45.0	1	ш	dBc
			T _{MIN}			-40.0	ΙV	IV	dBc
			T _{MAX}			-45.0	ıv	IV I	dBc
HD3	3rd Harmonic Distortion	2 Vpp	25°C		-60.0	-50.0	1	111	dBc
i	at 20 MHz		T _{MIN, TMAX}			-50.0	ΙV	ΙV	₫ B c
EQUIVALE	NT INPUT NOISE								
NF	Noise Floor	(Note 3)	25°C		-157.0	-154.0	IV	ΙV	dBm (1 Hz)
	>100 kHz		T _{MIN}			-154.0	IV	IV	dBm (1Hz)
			T _{MAX}			-153.0	IV	ľV	dBm (1Hz)
INV	Integrated Noise	(Note 3)	25°C		40.0	57.0	īV	ΙV	μV
	100 kHz to 200 MHz		T _{MIN}		-	57.0	ΙV	IV	μV
			T _{MAX}			63.0	ΙV	17	μV
VIDEO PER	FORMANCE								
d _G	Differential Gain (Note 4)	NTSC/PAL	25°C		0.02		ν	V	% pp
d₽	Differential Phase (Note 4)	NTSC/PAL	25°C		0.01		٧	Ý	° pp
d _G	Differential Gain (Note 4)	30 MHz	25°C		0.05	*****	٧	v	% pp
dр	Differential Phase (Note 4)	30 MHz	25°C		0.05		٧	٧	° pp
VBW	-0.1 dB Bandwidth (Note 4)		25°C		60.0		٧	٧	MHz

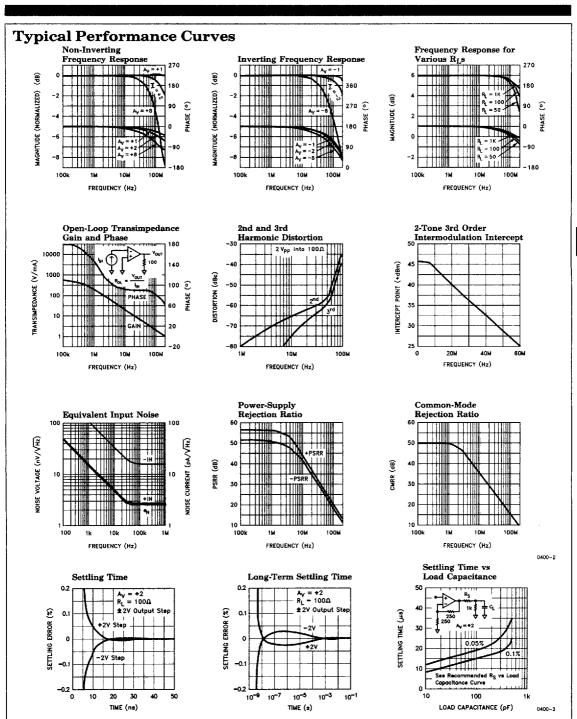
Note 1: Measured from T_{MIN} to T_{MAX}.

Note 2: Common-Mode Input Range for Rated Performance.

Note 3: Noise Tests are Performed from 5 MHz to 200 MHz.

Note 4: Differential Gain/Phase Tests are $R_L = 100\Omega$. For other values of R_L , see curves.

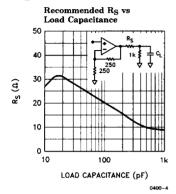
200 MHz Current Feedback Amplifier

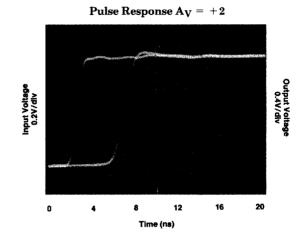


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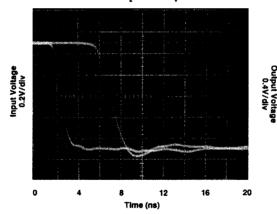
200 MHz Current Feedback Amplifier

Typical Performance Curves - Contd.

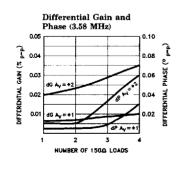


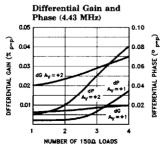


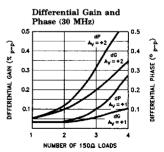
Pulse Response $A_V = +2$



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0400-7

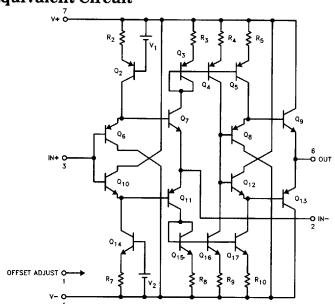
0400-5

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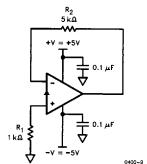
EL400/EL400C

200 MHz Current Feedback Amplifier

Equivalent Circuit



Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL400 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL400 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transim-pedance (R_{OL}) of the EL400 [$V_{OUT} = (R_{OL})^*$ ($-I_{IN}$)]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

- The voltage across the inputs is approximately 0V.
- 2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the

EL400. The nominal value for the feedback resistor is 250Ω , which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower -3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase

An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IREpp reference signal is applied to the device with 0V DC offset (0IRE) at 3.58 MHz for NTSC, 4.43 MHz for

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Applications Information — Contd.

PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75 Ω in series at the drive end and 75 Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 Vpp, with each back-terminated load at 150 Ω . The EL400 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL400 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the tech-

nique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Offset Adjustment Pin

Output offset voltage of the EL400 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to $\pm 5V$ results in an offset voltage adjustment of at least ± 10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL400 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

EL400 Macromodel

- * Revision A. March 1992
- * Enhancements include PSRR, CMRR, and Slew Rate Limiting
- * Connections: +input -input + Vsupply -Vsupplyoutput .subckt M400
- * Input Stage
- e1 10 0 3 0 1.0
- vis 10 9 0V
- h2 9 12 vxx 1.0
- r1 2 11 50
- 11 11 12 48nH
- $iinp 308 \mu A$ iinm 208 µA
- * Slew Rate Limiting
- h1 13 0 vis 600
- r2 13 14 1K
- d1 14 0 dclamp
- d2 0 14 dclamp
- * High Frequency Pole
- *e2 30 0 14 0 0.00166666666 13 30 17 0.1 µH
- c5 17 0 0.1pF
- r5 17 0 500
- * Transimpedance Stage
- g1 0 18 17 0 1.0
- rol 18 0 150K
- cdp 18 0 2.8pF
- * Output Stage
- q1 4 18 19 qp
- q2 7 18 20 qn
- q3 7 19 21 qn
- q4 4 20 22 qp
- r7 21 6 2
- r8 22 6 2

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EL400 Macromodel - Contd.

ios1 7 19 2.5mA ios2 20 4 2.5mA

* Supply Current

ips 7 4 9mA

1ps / 4 9m.A

* Error Terms

* ivos 0 23 5mA vxx 23 0 0V e4 24 0 6 0 1.0 e5 25 0 7 0 1.0 e6 26 0 4 0 1.0

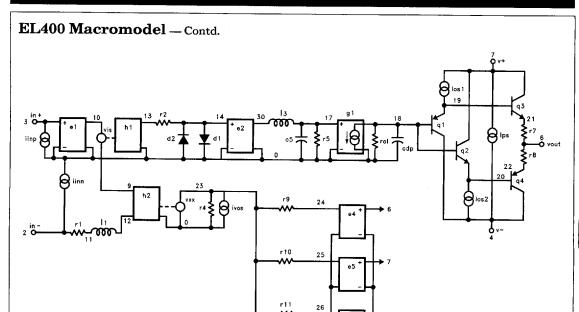
r9 24 23 3K r10 25 23 1K

r11 26 23 1K

* Models

.model qn npn (is = 5e - 15 bf = 200 tf = 0.5nS) .model qp pnp (is = 5e - 15 bf = 200 tf = 0.5nS) .model dclamp d(is = 1e - 30 ibv = 0.266 bv = 1.3 n = 4) .ends

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