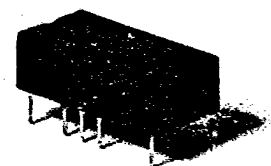


**SERIES EL5110 ECL DIGITAL DELAY MODULES**

- 5 Taps 16 Pin DIP Package
- Input & Output Buffered
- 5 Equally Spaced Taps

**Specifications:**

- Supply Voltage : -5.2v
- Logic 1 Voltage : -.96v
- Logic 1 Current : .26mA
- Logic 0 Current : .5 $\mu$ A
- Logic 0 Voltage : -1.65v
- Operating Temperature : -30°C to 85°C
- Power Dissipation : 200mW Typ. (No load)

**Input Test Conditions:**

- Input Pulse-Width : Min. 40% of Total Delay
- Input Pulse Rise : 2NS
- Input Pulse Voltage : -.7v
- Vee Supply Voltage : -5.2VDC
- Vee Supply Current : 40mA Typ.

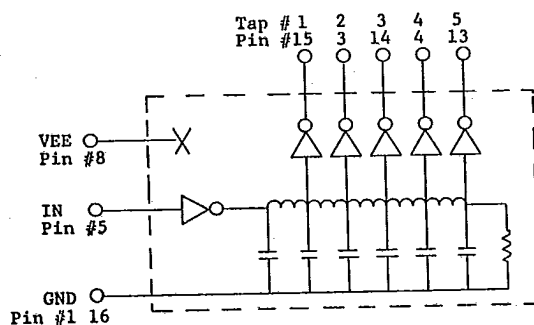
Electrical Specifications at 25°C

| Part Number | Total Delay NSEC $\pm 5\%$ | Tap to Tap Delay NS (1) | Rise Time NS Max(2) |
|-------------|----------------------------|-------------------------|---------------------|
| EL5110*     | 5                          | 1                       | 4                   |
| EL5111*     | 10                         | 2                       | 4                   |
| EL5112*     | 15                         | 3                       | 4                   |
| EL5113*     | 20                         | 4                       | 4                   |
| EL5114      | 25                         | 5                       | 4                   |
| EL5115      | 30                         | 6                       | 4                   |
| EL5116      | 35                         | 7                       | 4                   |
| EL5117      | 40                         | 8                       | 4                   |
| EL5118      | 45                         | 9                       | 5                   |
| EL5119      | 50                         | 10                      | 5                   |
| EL5120      | 60                         | 12                      | 5                   |
| EL5121      | 75                         | 15                      | 8                   |
| EL5122      | 100                        | 20                      | 10                  |
| EL5123      | 125                        | 25                      | 15                  |
| EL5124      | 150                        | 30                      | 15                  |
| EL5125      | 200                        | 40                      | 20                  |
| EL5126      | 250                        | 50                      | 20                  |
| EL5127      | 300                        | 60                      | 28                  |
| EL5128      | 400                        | 80                      | 38                  |
| EL5129      | 500                        | 100                     | 45                  |

Note: (1) Measured at 50% leading edge, Tol.  $\pm 5\%$  or  $\pm 2$ NS whichever is greater.

(2) Measured from 20% to 80% of leading edge.

\* Time Delay measurements referenced to 1st Tap



SCHEMATIC

INCHES .XXX  $\pm .010$   
MILLIMETERS .XX  $\pm .25$

