SERIES EL512 ECL (10K COMPATIBLE) LOGIC DELAY MODULES – 10 TAPS

- 10 Taps 32 Pin DIP Package • ECL Input & Output Levels • 10 Equally Spaced Taps
- 70 ECL DC Fan-out Capacity

Specifications:

- Supply Voltage : –5.2VDC to Vee
- Logic 1 Voltage(3) : –.96v
- Logic 1 Current : 265μA Max
- Logic 0 Voltage : –1.65v
- Logic 0 Current : 1.0μA
- Operating Temperature : –30°C to 85°C
- Power Dissipation : 400mW Typ. (No load)
- Temperature Coefficient : ⩾300PPM/°C

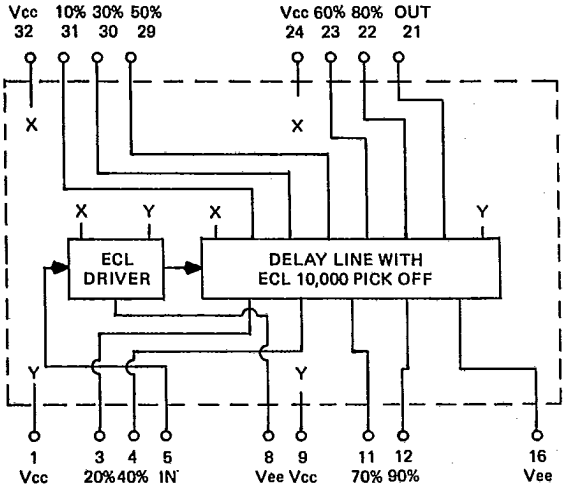
Test Conditions:

- Input Pulse-Width : Min. 40% of Total Delay
- Input Pulse Rise Time : 2NSEC Max
- Input Pulse Voltage : 1v (–0.75vH to –1.75vL)
- Vee Supply Voltage : –5.2VDC
- Vee Supply Current : 40mA Typ.

Electrical Specifications at 25°C

Part Number	Total Delay NSEC (1)	Tap to Tap Delay NS (1)	Rise Time NS Max (2)
EL512–10*	9	1	2.5
EL512–20*	18	2	2.5
EL512–25*	22.5	2.5	2.5
EL512–40*	36	4	3
EL512–50*	45	5	4
EL512–60	60	6	4
EL512–75	75	7.5	5
EL512–100	100	10	5
EL512–150	150	15	7
EL512–200	200	20	8
EL512–250	250	25	10
EL512–300	300	30	16
EL512–400	400	40	18
EL512–500	500	50	20
EL512–750	750	75	25
EL512–1000	1000	100	30
EL512–1500	1500	150	40

Note: (1) Measured at –1.3v level leading edge, Tol. ±5% or ±1NS whichever is greater.
(2) Measured from 20% to 80% Pulse Amplitude.
*Time Delay measurements referenced to 1st Tap.
(3) Outputs terminated through 270 ohms to –5.2VDC.



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