PLESSEY Semiconductors

AUGUST 1987

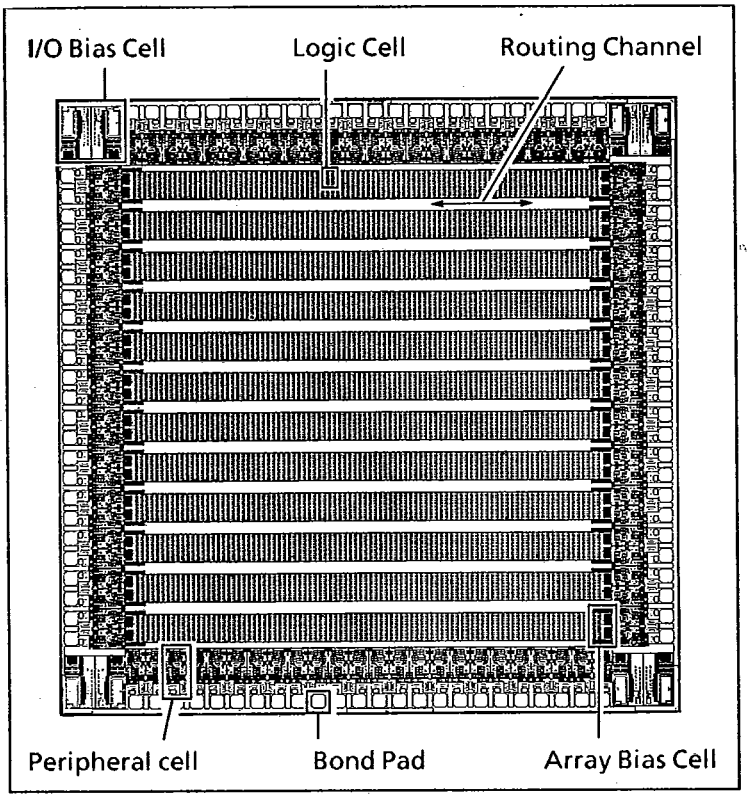
ELA 60000 SERIES

ECL GATE ARRAYS

(SUPERSEDES NOVEMBER 1986 AND APRIL 1987 EDITIONS)

The **ELA60000** series of ECL gate arrays is a very high performance family of Semi-Custom products based on an advanced 1.5 micron bipolar process. There are four members of the family, covering the range from 660 to 4500 equivalent gates. Each is capable of operating at a system clock speed of 1 GHz. All arrays use the same cell structures, and contain pre-defined reference voltage and band-gap generation cells.

A particular advantage of this family is that none of the peripheral connections are fixed. So the designer may freely assign power and signals to any of the package pins, with the freedom to make any signal pin compatible with ECL 10K, ECL100K, TTL or CMOS. Customisation is accomplished with three layers of metallisation; the first two carry signals and the third (which is standard) is used for power and bias voltage distribution. The use of three layers enables a high degree of gate utilisation, and enhances noise immunity by reducing local voltage fluctuations.



ELA63000 ARRAY STRUCTURE

FEATURES

- Typical system clock rate 1 GHz
- Internal toggle rate 2 GHz
- Typical OR-gate delay 180 psec
- Programmable speed-power
- 660, 1400, 2900, or 4500 gates
- Macro libraries
- Military, Industrial and Commercial grades
- Three layer metallisation
- All peripheral cells fully programmable
- ECL10K , ECL100K, TTL, CMOS I/O compatible
- Fully supported by PLESSEY CAE Software

ELA 60000 FAMILY SUMMARY

ARRAY CHARACTERISTIC	ELA61000	ELA62000	ELA63000	ELA65000
Number of array cells	240	512	1056	1680
Equivalent Gate Complexity (approximate)	660	1400	2900	4500
Total I/O Cells (including power pins)	48	68	96	120
Typical I/O Usage For Power Supplies	4-8	8-12	12-16	20-24

ECL 10K INPUT/OUTPUT VOLTAGE/CURRENT CHARACTERISTICS (DC to 100MHz) 1

SYMBOL	$T_{ambient}$ (T_j = Ambient + 50°C)				T_{case}	UNIT
	-55°C	0°C	25°C	70°C	125°C	
$V_{OH_{max}}$	-850	-770	-730	-650	-575	mV
$V_{IH_{max}}$	-800	-720	-680	-600	-525	mV
$V_{OH_{min}}$	-1080	-1000	-980	-920	-850	mV
$V_{IH_{min}}$	-1255	-1145	-1105	-1045	-1000	mV
$V_{IL_{max}}$	-1510	-1490	-1475	-1450	-1400	mV
$V_{OL_{max}}$	-1655	-1625	-1620	-1585	-1545	mV
$V_{OL_{min}}$	-1980	-1980	-1980	-1980	-1980	mV
$V_{IL_{min}}$	-2000	-2000	-2000	-2000	-2000	mV
$I_{IH_{max}}$	30	30	30	30	30	uA
$I_{IL_{min}}$	0.5	0.5	0.5	0.5	0.5	uA

ECL10K TIMING CHARACTERISTICS 1,2,4,5

SYMBOL	PARAMETER	TEST CONDITIONS	COMM (0°C / +70°C)			MIL (-55°C / +125°C)			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{IPD}	Input Propagation Delay	-		0.2			0.2		nS
t_{OPD}	Output Propagation Delay	C_L = 5pF 3		0.8			0.8		nS
F_{MAX_T}	Internal Flip-Flop Toggle Frequency	Low speed			320			320	MHz
		Med speed			640			640	MHz
		High speed			1000			1000	MHz

ECL 100K INPUT/OUTPUT VOLTAGE/CURRENT CHARACTERISTICS (DC to 100MHz) 4,6,7

SYMBOL	PARAMETER	TEST CONDITIONS	COMM (0°C / +70°C) V_{EE} = -4.2v to -4.8v			MIL (-55°C / +125°C) V_{EE} = -4.2v to -4.8v			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output Voltage HIGH	-	-1035		-850	-1080		-835	mV
V_{OL}	Output Voltage LOW	-	-1830		-1605	-1880		-1595	mV
V_{IH}	Input Voltage HIGH	-	-1145		-800	-1145		-800	mV
V_{IL}	Input Voltage LOW	-	-1950		-1475	-1950		-1475	mV
I_{IN}	Input Current	$V_{in} = V_{IL_{min}}$	0.5			0.5			uA

ECL100K TIMING CHARACTERISTICS 2,4,6

SYMBOL	PARAMETER	TEST CONDITIONS	COMM (0°C / +70°C)			MIL (-55°C / +125°C)			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{IPD}	Input Propagation Delay	-		0.2			0.2		nS
t_{OPD}	Output Propagation Delay	C_l = 5pF 3		1.1			1.1		nS
F_{MAX_T}	Internal Flipflop Toggle Rate	Low speed			320			320	MHz
		Med speed			640			640	MHz
		High speed			1000			1000	MHz

TTL INPUT/OUTPUT DC CHARACTERISTICS 4,7,8,10 V_{cc}(nominal) = +5.0v GND = 0

(Input: DC to 100MHz. Output: DC to 25 MHz) 9

SYMBOL	PARAMETER	TEST CONDITIONS	COMM (0°C / +70°C)			MIL (-55°C / +125°C)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output Voltage HIGH	V_{CC} = Min I_{OH} = -0.4mA	2.5	3.0		2.4	3.0		V
V_{OL}	Output Voltage LOW	V_{CC} = Min I_{OL} = 4.0mA			0.4			0.4	V
V_{IH}	Input Voltage HIGH	-	2.0			2.0			V
V_{IL}	Input Voltage LOW	-			0.8			0.8	V
I_{IN}	Input Current	Vin = GND to V_{CC}	-50		50	-50		50	uA
I_{OZH}	3-state 'off' HIGH	V_{CC} = Max V_O = 2.4V	-50		50	-50		50	uA
I_{OZL}	3-state 'on' LOW	V_{CC} = Max V_O = 0.4V	-50		50	-50		50	uA
I_{OS}	Output S/C Current	V_{CC} = Max V_O = 0V	-25		-100	-25		-100	mA

CMOS INPUT DC CHARACTERISTICS 4,7,8,10 V_{cc}(nominal) = +5.0v GND = 0

(DC to 100MHz.)

SYMBOL	PARAMETER	TEST CONDITIONS	COMM (0°C / +70°C)			MIL (-55°C / +125°C)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input Voltage HIGH	-	$0.7V_{CC}$			$0.7V_{CC}$			V
V_{IL}	Input Voltage LOW	-			$0.3V_{CC}$	-50		$0.3V_{CC}$	V
I_{IN}	Input Current	V_{in} = GND to V_{CC}	-50		50			50	uA

TTL/CMOS AC CHARACTERISTICS 8,10 V_{cc}(nominal) = +5.0v GND = 0

SYMBOL	PARAMETER	TEST CONDITIONS	COMM (0°C / +70°C)			MIL (-55°C / +125°C)			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{IPD}	Input Propagation Delay	-		1.5			1.5		nS
t_{OPD}	Output Propagation Delay	C_L = 15pF 3,9		4.0			4.0		nS
F_{MAX_T}	Max. Internal Flip-Flop Toggle Rate 11	-			As ECL			As ECL	MHz

Notes

1 Load = 50Ω /5pF to -2v. V_{EE} = -5.2v, GND = 0v.
2 Typical figures are for T_J = 27°C.
3 C_L includes probe and jig capacitances.
4 Minimum and Maximum figures include both V_{EE} tolerances (± 0.3v) and process variations
5 V_{EE} = -4.9v to -5.5v
6 Load = 50Ω /5pF to -2v V_{EE} = -4.5v, GND = 0v.
7 Measured at thermal equilibrium, with T_J not exceeding 170°C.
8 V_{cc} limits are + 4.75V to + 5.75V (Commercial Grade) and + 4.5V to + 5.5V (Military Grade)
9 One standard TTL load circuit used when testing TTL outputs.
10 Typical figures are for T_J = 27°C and V_{cc} = 5.0v
11 Internal toggle rates are identical to ECL data on facing page as same internal cells are used.

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	(V_{CC}-GND) = +6.0v	(V_{EE}-GND) = -6.0v
Storage Temperature Range:	-55°C to + 150°C	
Maximum Junction Temperature:	175°C	

INTERNAL FUNCTION LIBRARY (Excluding Macros)

CELL DESCRIPTION	SIZE 1	TYPE	CODE	STATIC CURRENT I_{ee} (-mA) Typ.	STATIC CURRENT I_{cc} (+mA) Typ
Buffer	1	H	HBUF	1.6	-
		M	MBUF	0.8	-
		L	LBUF	0.4	-
Inverter	1	H	HINV	1.6	-
		M	MINV	0.8	-
		L	LINV	0.4	-
Buffer/Inverter	1	H	HBUFN	2.4	-
		M	MBUFN	1.2	-
		L	LBUFN	0.6	-
2-input OR	1	H	HOR2	1.6	-
		M	MOR2	0.8	-
		L	LOR2	0.4	-
2-input NOR	1	H	HNOR2	1.6	-
		M	MNOR2	0.8	-
		L	LNOR2	0.4	-
2-input OR/NOR	1	H	HORN2	2.4	-
		M	MORN2	1.2	-
		L	LORN2	0.6	-
3-input OR	1	H	HOR3	1.6	-
		M	MOR3	0.8	-
		L	LOR3	0.4	-
3-input NOR	1	H	HNOR3	1.6	-
		M	MNOR3	0.8	-
		L	LNOR3	0.4	-
3-input OR/NOR	2	H	HORN3	2.4	-
		M	MORN3	1.2	-
		L	LORN3	0.6	-
Dual 3-input OR/NOR	3	H	H2ORN3	4.8	-
4-input OR	1	H	HOR4	1.6	-
		M	MOR4	0.8	-
		L	LOR4	0.4	-
4-input NOR	1	H	HNOR4	1.6	-
		M	MNOR4	0.8	-
		L	LNOR4	0.4	-
4-input OR/NOR	2	H	HORN4	2.4	-
		M	MORN4	1.2	-
		L	LORN4	0.6	-
Dual 4-input OR/NOR	3	H	H2ORN4	4.8	-
5-input OR	1	H	HOR5	1.6	-
5-input NOR	1	H	HNOR5	1.6	-
2-input AND	1	H	HAND2	2.4	-
2-input NAND	1	H	HNAND2	2.4	-
2-input AND/NAND	2	H	HANDN2	3.2	-
		M	MANDN2	1.6	-
		L	LANDN2	0.8	-
Dual 2-input AND/NAND	3	H	H2ANDN2	6.4	-
		M	M2ANDN2	3.2	-
		L	L2ANDN2	1.6	-
2-input EXOR/EXNOR	2	H	HXORN2	3.2	-
		M	MXORN2	1.6	-
		L	LXORN2	0.8	-
2:1:MUX	2	H	HMUX2	3.2	-
		M	MMUX2	1.6	-
		L	LMUX2	0.8	-
2-input, Or-input 2:1:MUX	2	H	HOR2M2	3.2	-
		M	MOR2M2	1.6	-
		L	LOR2M2	0.8	-
D-type Latch	2	L	LDL	0.8	-
RESET D-type Latch	2	L	LRDL	0.8	-
SET D-type Latch	2	L	LSDL	0.8	-
2-input OR D-type Latch	2	L	LOR2DL	0.8	-
D-type Flip-flop	3	H	HDF	6.4	-
		M	MDF	2.4	-
		L	LDF	1.2	-
OR input D-type Flip-flop	3	H	HOR2DF	6.4	-
		M	MOR2DF	2.4	-
		L	LOR2DF	1.2	-
RESET D-type Flip-flop	3	H	HRDF	5.6	-
		M	MRDF	2.4	-
		L	LRDF	1.2	-
SET D-type Flip-flop	3	H	HSDF	5.6	-
		M	MSDF	2.4	-
		L	LSDF	1.2	-
OR input RESET D-type	3	H	HOR2RDF	5.6	-
	4	M	MOR2RDF	2.4	-
	4	L	LOR2RDF	1.2	-
OR input SET D-type	3	H	HOR2SDF	5.6	-
	4	M	MOR2SDF	2.4	-
	4	L	LOR2SDF	1.2	-
Static '1' & '0'	1	H	HOZ	2.4	-

INPUT/OUTPUT FUNCTION LIBRARY

CELL DESCRIPTION	SIZE [1]	TYPE	CODE	STATIC CURRENT I_{ee} (-mA) Typ.	STATIC CURRENT I_{cc} (+mA) Typ.
ECL10K Input	1	P	PEXI	2.4	-
ECL10K Buffer Output	1	P	PEXO	4.8	-
ECL10K Inverting Output	1	P	PEXON	4.8	-
ECL10K Differential Input	2	P	PEXDI	2.4	-
ECL10K Differential Output	2	P	PEXDO	4.8	-
ECL100K Input	1	P	PECI	2.4	-
ECL100K Buffer Output	1	P	PECO	4.8	-
ECL100K Inverting Output	1	P	PECON	4.8	-
ECL100K Differential Input	2	P	PECDI	2.4	-
ECL100K Differential Output	2	P	PECDO	4.8	-
TTL Input	1	P	PTI	4.0	3.3
TTL Buffer Output	1	P	PTO	4.8	4.4
TTL I/O 3-state	1	P	PTIOZ	13.5	10.8
CMOS Input	1	P	PCI	4.0	3.3
ECL Positive Power	1	P	PPEPOS	-	-
ECL Negative Power	1	P	PPENEG	-	-
TTL/CMOS Positive Power	1	P	PPTPOS	-	-
TTL/CMOS Negative Power	1	P	PPTNEG	-	-

1 Sizes are expressed in Array Cells for internal functions, and in Peripheral Cells for I/O functions.

INTERNAL LOGIC CELL PERFORMANCE [1]

CELL DESCRIPTION	NOTES	TIME DELAY (ps)					
		Minimum [2]		Typical [3]		Maximum [4]	
		Rising	Falling	Rising	Falling	Rising	Falling
Low speed Inverter	A to FN	300	330	500	550	775	852
Medium speed Inverter	A to FN	132	216	220	360	341	558
High speed Inverter	A to FN	102	123	170	205	263	317
Low speed 2-input NOR	A or B to FN	420	405	700	675	1085	1046
Medium speed 2-input NOR	A or B to FN	162	246	270	410	418	635
High speed 2-input NOR	A or B to FN	123	147	205	245	317	379
Low speed D-type Flipflop	CL to Q CL to QN	600 600	600 420	1000 1000	1000 700	1550 1550	1550 1085
Medium speed D-type Flipflop	CL to Q CL to QN	300 300	378 318	500 500	630 530	775 775	976 821
High speed D-type Flipflop	CL to Q CL to QN	195 192	222 219	325 320	370 365	503 496	573 566

SET-UP AND HOLD TIMES [1]

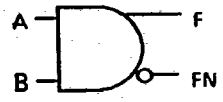
CELL DESCRIPTION	NOTES	SET-UP AND HOLD TIMES (ps)					
		Minimum [2]		Typical [3]		Maximum [4]	
		Set-up	Hold	Set-up	Hold	Set-up	Hold
Low speed D-type Flipflop	D input	480	270	800	450	1240	697
Medium speed D-Flipflop	D input	240	210	400	350	620	542
High speed D-type Flipflop [5]	D input	48	78	80	130	124	200

Notes:

1 All values are for fan-in = 3 and fan-out = 3 (at the same power level)
2 Best case performance, with maximum power supply (Nominal + 0.3v), and T_j = -55°C
3 Typical performance, with nominal power supply and T_j = + 27°C
4 Worst case performance, with minimum power supply (Nominal -0.3v), and T_j = + 170°C
5 The high speed D-type requires a differential clock. Maximum permissible clock skew = 220ps

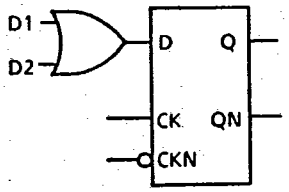
TYPICAL CELL PERFORMANCE (Fanin = Fanout = 3 high speed cells)

HANDN 2



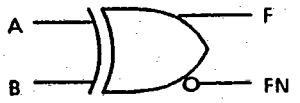
TYPICAL PERFORMANCE
A to F,FN t_{pd} = 230ps
B to F,FN t_{pd} = 300ps

HOR2DF



TYPICAL PERFORMANCE
CK to Q t_{pd} = 350ps
CK to QN t_{pd} = 350ps

HXORN2



TYPICAL PERFORMANCE
A to F,FN t_{pd} = 270ps
B to F,FN t_{pd} = 375ps

SOFTWARE DESIGN SUPPORT

Plessey's own CAD software runs on VAX equipment under VMS, and has been developed through several generations of Semi-Custom products to provide advanced tools for schematic input, logic simulation, timing verification and fault analysis. It has recently been extended to cover the ELA60000 family of ECL gate arrays, to provide up to 20 levels of hierarchy, and to incorporate a graphic layout editor offering interactive placement and three powerful autorouting algorithms. The ELA60000 Cell Library already contains over 80 low-level functions, plus an ever-increasing range of macros of higher complexity.
A list of the cells and macros which are undergoing development and testing can be supplied on request.

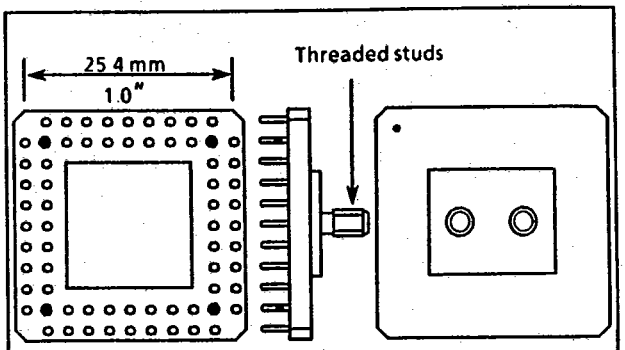
DESIGN INTERFACES

Plessey Semiconductors are able to offer many ways of interfacing with their customers during the process of designing for ECL gate arrays. These range from Plessey performing all the necessary design steps between logic diagram and final design acceptance through to the customer licensing CAD software from Plessey and performing all these steps on his own VAX equipment. In all cases Plessey receive the final, approved data tapes, from which they make the metallisation masks and a small batch of tested prototypes for acceptance testing prior to full scale production. It is also intended to develop libraries for several popular CAE workstations . This will allow customers to design and simulate their ECL gate arrays on these general purpose systems prior to commencing chip layout with the Plessey suite of software.

Note: VAX and VMS are trademarks of Digital Equipment Corporation

PACKAGING

ELA60000 arrays are available in a variety of ceramic packages. The smallest packages (for ELA61000) are 22 pin DIL and 28 way leadless chip carrier. Larger arrays can be supplied in chip carriers up to 84 ways. Use of such packages is, however, subject to Plessey's assessment of power dissipation relative to the customer's operating environment. For high power/high temperature applications, studded, high power pin grid arrays, with 68 or 120 pins, are available. These have been selected for low thermal resistance and lead impedance, and are ideal for large arrays operating at high speeds.



OUTLINE OF 68 PIN PACKAGE

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