



HSIN-CHU : NO. 12, INNOVATION 1ST. RD.,
SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU CITY, TAIWAN, R.O.C.
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TITLE: **EM61000 RAM & Register DEFINE**

RAM register :		b7	b6	b5	b4	b3	b2	b1	b0
R0	IAR	Indirect RAM data							
R1	TCC	Timer up Counter							
R2	PC	Program Counter, 13bit 8K ROM max.							
R3	SF	PS2	PS1	PS0	T	P	Z	DC	C
R4	RSR	RAM Bank 0-7			Indirect RAM address 0x20-0x3F for R0				
R5	INTC	ENI	-	TC2IE	TC2IF-	MIE	TCIE	MIF	TCIF
R6	MTC	Melody Time down Counter							
R7	TCC2	Timer 2 up Counter							
R8	WDT	-	PL1	PL2H	PL2L	-	WAKEH	WAKEL	WTE
R9	Mapping	-	-	-	DA SEL	DA SET	CH2	CH1	CH0
RA	MODE	Speech Melody interface Register							
RB	Port 1	Port 1 Read data							
RC	Port 2	Port 2 R/W data							
RD	Port 3	Port 3 R/W data							
RE	Port 4	Port 4 R/W data							
RF	Port 5	Port 5 Write data							
R10	MULT	Multiplier							
R11	PRODL	Multiplication result Low							
R12	PRODH	Multiplication result High							



RAM register :		b7	b6	b5	b4	b3	b2	b1	b0
R13	<i>Acc_Buf</i>								
R14	<i>SF_Buf</i>								
R15	<i>RSR_Buf</i>								
R16	<i>R9_Buf</i>								
R17	<i>Ch_Flag</i>	<i>FMch8</i>	<i>FMch7</i>	<i>FMch6</i>	<i>FMch5</i>	<i>FMch4</i>	<i>FMch3</i>	<i>FMch2</i>	<i>FMch1</i>
R18									
R19									
R1A									
R1B									
R1C									
R1D									
R1E									
R1F									

Notes: EM61001 not support Port4 & port5.
EM61002 not support Port1 , Port3, Port4 & Port5.
EM61100, EM61200, EM61300 not support Port5.

Notes: **Red Name** = initial is **HIGH** after RESET
Blue name = initial is **LOW** after RESET
Black name = initial is **Un-Know** after RESET.



Bank 0 (RSR=000x-xxxx)

Bank 1 (RSR=001x-xxxx)

R20		
R21		
R22		
R23		
R24		
R25		
R26		
R27		
R28		
R29		
R2A		
R2B		
R2C		
R2D		
R2E		
R2F		
R30	<i>MchStatus for MCH1</i> <i>FPaus FNote FEnv1 Fenv0 Flton directi lTstr FTone</i>	<i>MchStatus for MCH2</i> <i>FPaus FNote FEnv1 Fenv0 Flton directi lTstr FTone</i>
R31	<i>Inst = 0III III ,</i>	<i>Inst = 0III III ,</i>
R32	<i>Beat0</i>	<i>Beat0</i>
R33	<i>Beat1</i>	<i>Beat1</i>
R34	<i>Envelope</i>	<i>Envelope</i>
R35	<i>Volum = 0VVV VVVV</i>	<i>Volum = 0VVV VVVV</i>
R36	<i>Env_Type = 000E EEEE</i>	<i>Env_Type = 000E EEEE</i>
R37	<i>Env_Index</i>	<i>Env_Index</i>
R38	<i>Env_M1</i>	<i>Env_M1</i>
R39	<i>Env_N1</i>	<i>Env_N1</i>
R3A	<i>Env_Dest</i>	<i>Env_Dest</i>
R3B	<i>Env_Count</i>	<i>Env_Count</i>
R3C	<i>Note_buf</i>	<i>Note_buf</i>
R3D		
R3E		
R3F		



Bank 2 (RSR=010x-xxxx)

Bank 3 (RSR=011x-xxxx)

R20		
R21		
R22		
R23		
R24		
R25		
R26		
R27		
R28		
R29		
R2A		
R2B		
R2C		
R2D		
R2E		
R2F		
R30	<i>MchStatus for MCH3</i> <i>FPaus FNote FEnv1 Fenv0 Flton directi lTstr FTone</i>	<i>MchStatus for MCH4</i> <i>FPaus FNote FEnv1 Fenv0 Flton directi lTstr FTone</i>
R31	<i>Inst = 0III III ,</i>	<i>Inst = 0III III ,</i>
R32	<i>Beat0</i>	<i>Beat0</i>
R33	<i>Beat1</i>	<i>Beat1</i>
R34	<i>Envelope</i>	<i>Envelope</i>
R35	<i>Volum = 0VVV VVVV</i>	<i>Volum = 0VVV VVVV</i>
R36	<i>Env_Type = 000E EEEE</i>	<i>Env_Type = 000E EEEE</i>
R37	<i>Env_Index</i>	<i>Env_Index</i>
R38	<i>Env_M1</i>	<i>Env_M1</i>
R39	<i>Env_N1</i>	<i>Env_N1</i>
R3A	<i>Env_Dest</i>	<i>Env_Dest</i>
R3B	<i>Env_Count</i>	<i>Env_Count</i>
R3C	<i>Note_buf</i>	<i>Note_buf</i>
R3D		
R3E		
R3F		



Bank 4 (RSR=100x-xxxx)

Bank 5 (RSR=101x-xxxx)

R20		
R21		
R22		
R23		
R24		
R25		
R26		
R27		
R28		
R29		
R2A		
R2B		
R2C		
R2D		
R2E		
R2F		
R30	<i>MchStatus for MCH5</i> <i>FPaus FNote FEnv1 Fenv0 Flton directi lTstr FTone</i>	<i>MchStatus for MCH6</i> <i>FPaus FNote FEnv1 Fenv0 Flton directi lTstr FTone</i>
R31	<i>Inst = 0III III ,</i>	<i>Inst = 0III III ,</i>
R32	<i>Beat0</i>	<i>Beat0</i>
R33	<i>Beat1</i>	<i>Beat1</i>
R34	<i>Envelope</i>	<i>Envelope</i>
R35	<i>Volum = 0VVV VVVV</i>	<i>Volum = 0VVV VVVV</i>
R36	<i>Env_Type = 000E EEEE</i>	<i>Env_Type = 000E EEEE</i>
R37	<i>Env_Index</i>	<i>Env_Index</i>
R38	<i>Env_M1</i>	<i>Env_M1</i>
R39	<i>Env_N1</i>	<i>Env_N1</i>
R3A	<i>Env_Dest</i>	<i>Env_Dest</i>
R3B	<i>Env_Count</i>	<i>Env_Count</i>
R3C	<i>Note_buf</i>	<i>Note_buf</i>
R3D		
R3E		
R3F		



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Bank 7 (RSR=111x-xxxx)

R20		<i>MchCtrl</i>
		<i>FchInst</i>
R21		<i>MchNumber</i>
R22		<i>Bank-No</i>
R23		<i>Temp0</i>
R24		<i>Temp1</i>
R25		<i>Temp2</i>
R26		<i>Freq1</i>
R27		<i>Freq2</i>
R28		<i>DataPtrL</i>
R29		<i>DataPtrM</i>
R2A		<i>DataPtrH</i>
R2B		
R2C		
R2D		
R2E		
R2F		<i>DAC_Status</i>
R30	<i>MchStatus for MCH7</i>	<i>MchStatus for MCH8</i>
	<i>FPaus</i> <i>FNote</i> <i>FEnv1</i> <i>Fenv0</i> <i>Flton</i> <i>directi</i> <i>lTstr</i> <i>FTone</i>	<i>FPaus</i> <i>FNote</i> <i>FEnv1</i> <i>Fenv0</i> <i>Flton</i> <i>directi</i> <i>lTstr</i> <i>FTone</i>
R31	<i>Inst = 0III III ,</i>	<i>Inst = 0III III ,</i>
R32	<i>Beat0</i>	<i>Beat0</i>
R33	<i>Beat1</i>	<i>Beat1</i>
R34	<i>Envelope</i>	<i>Envelope</i>
R35	<i>Volum = 0VVV VVVV</i>	<i>Volum = 0VVV VVVV</i>
R36	<i>Env_Type = 000E EEEE</i>	<i>Env_Type = 000E EEEE</i>
R37	<i>Env_Index</i>	<i>Env_Index</i>
R38	<i>Env_M1</i>	<i>Env_M1</i>
R39	<i>Env_N1</i>	<i>Env_N1</i>
R3A	<i>Env_Dest</i>	<i>Env_Dest</i>
R3B	<i>Env_Count</i>	<i>Env_Count</i>
R3C	<i>Note_buf</i>	<i>Note_buf</i>
R3D		
R3E		
R3F		



義隆電子股份有限公司
ELAN MICROELECTRONICS CORP.

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EM61000 I/O Register List :

		b7	b6	b5	b4	b3	b2	b1	b0
IOC 5	Prescaler	TCC2 Prescaler 1/8- 1/1024			TCC Prescaler 1/2- 1/256			WDT rate 1:1-1:8	
		P2S2	P2S1	P2S0	TSR2	TSR1	TSR0	WSR1	WSR0
IOC 6...IOC C		Melody interface Register							
IOC D	P2 I/O	Port 2 Input/Output set. 1=input, 0=output (init = 0xFFh)							
IOC E	P3 I/O	Port 3 Input/Output set. 1=input, 0=output (init = 0xFFh)							
IOC F	P4 I/O	Port 4 Input/Output set. 1=input, 0=output (init = 0xFFh)							

Notes: EM61001 not support IOCF
EM61002 not support IOCE & IOCF .

Notes: Red Name = initial is HIGH after RESET
Blue name = initial is LOW after RESET
Black name = initial is Un-Know after RESET.



EM61000 Melody Register List :

R9 Mapped Type		RA MODE								IOC 6	IOC 7	IOC 8	IOC 9	IOC A	IOC B	IOC C	IOC F
		b7	b6	b5	b4	b3	b2	b1	b0								
0	read ROM data	-	-	-	-	-	-	-	-	ADD L	ADD M	ADD H (4bit 1M)	ROM DATA (IOR only)	Melody Precaler 1/2- 1/256 (b2-b0)		-	Port4 I/O
1	M ch1	MSB	-	INLOOP WTADR		PENV	LENA	LOOPB	MENA	ADD L	ADD M	ADD H (4bit 1M)	LBIT Start Loop Addr -Mid	ENV Envelop (b6-b0)	F1 Frequency Fractional (b7-b2)	F2 Frequency Integer (b7-b0)	LBIT Start Loop Addr -Hi
2	M ch2	-		In Loop Area Write Address		Pass Envelope type	Load Enable	Loop Disable	Melody Enable Active								
3	M ch3																
4	M ch4																
5	M ch5																
6	M ch6																
7	M ch7																
8	M ch8																
9	DAC 1	-	Volume 0-7 step			DA range 0=b7-b0 1=b8-b1 2=b9-b2 3=b7-b0		-	DAC_ON	DA mixer Ch En b0=Mch1 b1=Mch2 ... b7=Mch8	-		-	-	-	Port 4 I/O	
A	DAC 2																

Notes: EM61001 & EM61002 not support Mch5 ~ Mch8 & DAC2
EM61001 ~ EM61100 not support IOC8 (Voice Rom size below 64Kbyte)

Notes: **Red Name** = initial is **HIGH** after RESET, **Blue name** = initial is **LOW** after RESET, **Black name** = initial is **Un-Know** after RESET.