Digitally Programmable 8 to 25 Multiplex LCD Controller & Driver

Features

- Slim IC for chip-on-board, with gold bumps for Chip-On-Glas and Chip-On-Flex technologies
- Very simple 2-wire interface
- Digitally programmable multiplex rates: 8 x 113, 9 x 112, 16 x 105, 17 x 104, 20 x 101, 21 x 100, 24 x 97, 25 x 96
- No lost pads while row driver from 8 up to 25
- On chip: Voltage multiplier, V_{LCD} up to 7 V (3 to 6 V at 25 °C), 64 V_{LCD} digitally programming steps, 4 V_{LCD} temperature compensation factors, bias generation, V_{ON} / V_{OFF} generation, frame frequency, display refresh RAM
- No busy state
- High noise immunity in inputs
- No external components needed, except a V_{LCD} capacitor
- Digitally reversing row data
- Digitally reversing column data
- Inverting data function
- Blank function
- Set function
- Checker and Inverted Checker functions
- Sleep modes
- Low LCD operating current consumption
- Wide V_{DD} voltage supply range, 2 to 5 V
- Wide temperature range: -40 to + 85 °C
- Direct display of RAM data through the display data RAM

(To cascade ICs, please see Fig. 19 and contact EM-Marin.)

Description

The EM6124 is a low power CMOS LCD controller and driver. The 8, 16, 20 and 24 way multiplex are digitally programmable by the command byte. One additional line can be added for Icons or Inverted Video by programming 9, 17, 21 or 25 way multiplex. The display refresh is handled on chip by an internal RC oscillator via one selectable 25 x 116 RAM which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 25 x 116 bit RAM (a set bit corresponds to an activated LCD pixel). The EM6124 has very low dynamic current consumption, typically 70 μA at V_{DD} = 2 V, V_{LCD} = 7 V making it particularly attractive for portable and battery powered products. The wide operating range on supply voltages and temperature offers much application flexibility. The LCD voltage, bias generation and frame frequency are generated on chip. The clock signal can be used to shift and to latch the data into the RAM.

Applications

- Mobile phones (GSM, DECT)
- Smart cards
- Automotive displays
- Portable, battery operated products
- Balances and scales, utility meters

Typical Operating Configuration

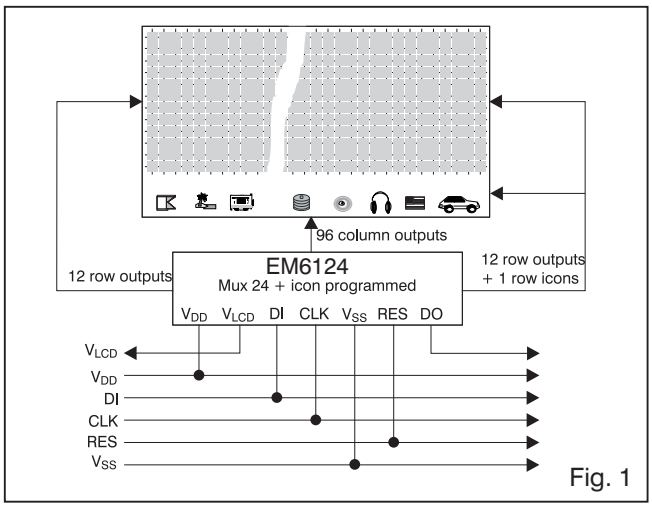
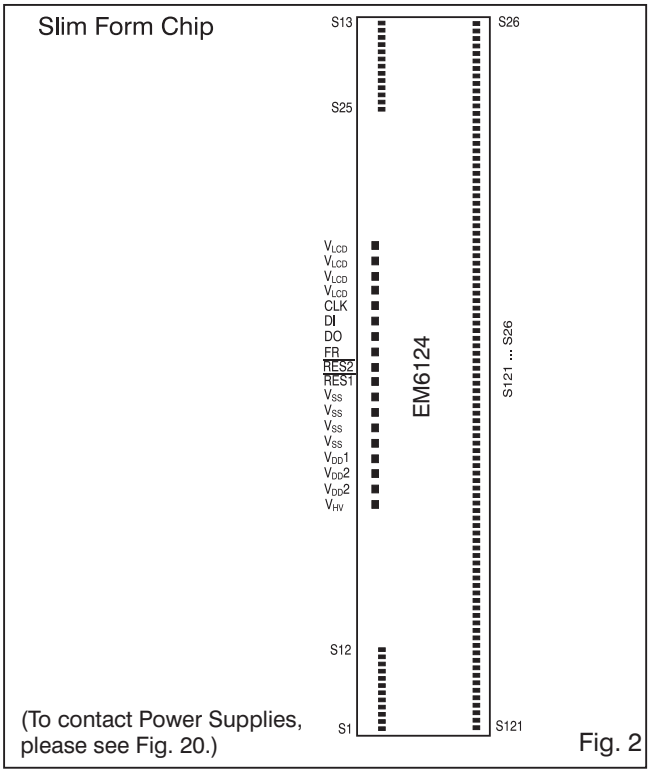


Fig. 1

Pad Assignment



(To contact Power Supplies, please see Fig. 20.)

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	$V_{DD1,2}$	-0.3 V to 6 V
Supply high voltage range	V_{HV}	-0.3 V to 6 V
Internal generated V_{LCD}	V_{LCD}	7 V
Voltage at DI, DO, CLK, FR, RES	V_{LOGIC}	-0.3 V to V_{DD} +0.3 V
Voltage at S1 to S121	V_{DISP}	-0.3 V to V_{LCD} +0.3 V
Storage temperature range	T_{STO}	-65 to +150 °C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Maximum soldering conditions	T_{Smax}	250 °C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	T_A	-40		+85	°C
Logic supply voltage	$V_{DD1,2}$	2	3	5.5	V
Supply high voltage	V_{HV}	2.5	3	5.5	V

Table 2

Electrical Characteristics

$V_{DD1} = V_{DD2} = 3$ V, $V_{HV} = 2.5$ to 5 V, and $T_A = -40$ to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby supply current	I_{DD}	See note 1)		16	22	µA
Standby supply current	I_{HV}	See note 1), V_{LCD} step 30 (hexa)		65	170	µA
Dynamic supply current	I_{DD}	See note 2)		57	75	µA
Standby supply current	I_{HV}	See note 3), V_{LCD} step 00 (hexa)		35	140	µA
Sleep mode supply current	I_{DD}			0.1		µA
Sleep mode supply current	I_{HV}			0.1		µA
Control Signals DI, CLK, FR, RES1,RES2						
Input leakage	I_{IN}	$V_{DD1,2}$ or V_{SS}	-1		1	µA
Input capacitance	C_{IN}	at T_A = 25 °C		8		pF
Low level input voltage	V_{IL}		0		0.3 $V_{DD1,2}$	V
High level input voltage	V_{IH}		0.7 $V_{DD1,2}$		$V_{DD1,2}$	V
DC output component	± VDC	See table 4		30	100	mV
V_{LCD} (internally generated)	V_{LCD}	See note 4)		6.15		
V_{LCD}	V_{LCD}	See note 5)		3.15 - 7.09		V
	V_{LCD} step			62.5		mV

Table 3

1) All outputs open, DI and CLK at V_{SS}, mux ratio = 24, checker pattern.
2) All outputs open, DI at V_{SS}, f_{CLK} = 1 MHz, mux ratio = 24, checker pattern.
3) DI and CLK at V_{SS}, checker pattern, mux ratio = 8.
4) Initialization bits 18 to 23 = 110000 and initialization bits 10, 11 = 00; laser trimming on request.
5) Initialization bits 18 to 23 = 000000/111111.

DC Output Component

Output	Frame	Logic Data	Measured*	Guaranteed
Row Driver	n	0L	$\lvert V_{LCD} - V_1 \rvert$	$V_1 = 0.83 \times V_{LCD} \pm 100$ mV
	n + 1	0L	$\lvert V_4 - V_{SS} \rvert$	$V_2 = 0.66 \times V_{LCD} \pm 100$ mV
Column Driver	n	0L	$\lvert V_{LCD} - V_2 \rvert$	$V_3 = 0.34 \times V_{LCD} \pm 100$ mV
	n + 1	0L	$\lvert V_3 - V_{SS} \rvert$	$V_4 = 0.17 \times V_{LCD} \pm 100$ mV

Table 4

$*V_X = \frac{V_X (\text{load} = +1\,\mu A) + V_X (\text{load} = -1\,\mu A)}{2}$, mux 24 or 25 programmed, V_{LCD} = 6 V, T_A = 25 °C.

Test is performed for multiplex rate = 25. All multiplex rate ≠ 25 are guaranteed by design. If multiplex rate ≠ 25, test will be performed on request.

Timing Characteristics

$V_{DD1} = V_{DD2} = 2$ to 3 V, $V_{HV} = 2.5$ to 5 V, and $T_A = -40$ °C to +85 °C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		70			ns
Clock low pulse width	t_{CL}		110			ns
Clock period	t_{per}		550			ns
Reset 1 pulse width	$t_{\overline{RES1}}$		10			µs
Reset 2 pulse width	$t_{\overline{RES2}}$		130			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20			ns
Data input hold time	t_{DH}		260			ns
FR (internal frame frequency)	f_{FR} [1)]			75		Hz

[1)] EM6124 (n), FR = n times the desired LCD refresh rate where n is the EM6124 mux mode number; laser trimming on request.
See Fig. 17.01 and 17.02 for more details concerning the frame frequency

Table 5a

$V_{DD1} = V_{DD2} = 3$ to 5 V, $V_{HV} = 2.5$ to 5 V, and $T_A = -40$ °C to +85 °C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		50			ns
Clock low pulse width	t_{CL}		55			ns
Clock period	t_{per}		350			ns
Reset 1 pulse width	$t_{\overline{RES1}}$		10			µs
Reset 2 pulse width	$t_{\overline{RES2}}$		80			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20			ns
Data input hold time	t_{DH}		140			ns
FR (internal frame frequency)	f_{FR} [1)]			75		Hz

[1)] EM6124 (n), FR = n times the desired LCD refresh rate where n is the EM6124 mux mode number; laser trimming on request.

Table 5b

Timing Waveforms

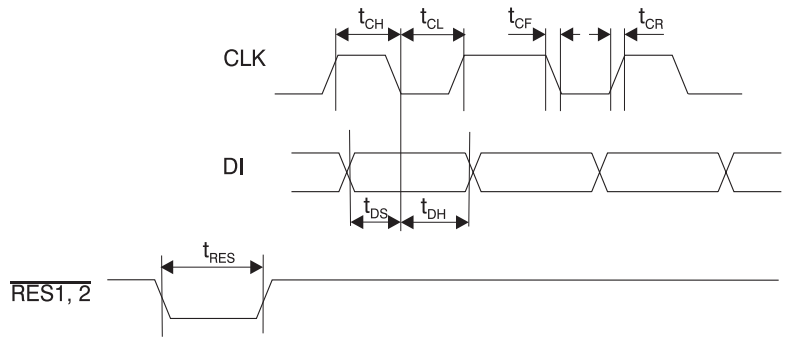


Fig. 3

1 Bit Interface Description

This 1 bit interface is very simple to use. There are three modes to load data into the EM6124.

Command byte only mode

To validate this mode, 8 bits must be shifted with bit 3 to bit 7 setted to 1L. This mode is used for blank, set or sleep mode functions.

Command byte and initialization mode

To validate this mode, 32 bits must be shifted with bit 0 and bit 1 setted to 1L. Bit 2 (sleep) can be active or inactive. Bit 3 to bit 7 (RAM address) can be in any state but it is important that they are not all simultaneously setted to 1L, otherwise the chip will be in command byte only mode.

Command byte and display information mode

To validate this mode, 128 bits must be shifted, eight first bits are for command byte, all the other are RAM data depending of col bit mode and multiplex ratio. There are also x bits don't care in each loading depending on the programmation of the chip (see Fig. 4 for more details).
In each RAM's data loading, the command byte has to be introduced for the RAM address. Before loading any data into the RAM the chip has to be initialized.

Command Byte

Commmand Bits 0 to 7							
0	1	2	3	4	5	6	7
Blank	Set	Sleep	RAM address				

Table 6

Cmdbit 0: Blank bit forces all column outputs off.
Cmdbit 1: Set bit forces all column output on.
Note: If bit 0 and bit 1 are both to 1L, the chip will be in initialization mode. See remarks below.
Cmdbit 2: Sleep mode bit, stops the voltage booster and the internal oscillator, active bit $\overline{col}$ forces all outputs to V_{SS}.
Cmdbits 3-7: RAM address bits. See table 6.
If Cmdbits 3-7 are set to 1L, EM6124 is in Cmd byte only mode.

Initialization Bits

Initialization Bits 8 to 15							
8	9	10	11	12	13	14	15
Mux Mode		Temp. Coeff.		Checker	Inv.Checker	$\overline{Col}$	Inv.Row
Initialization Bits 16 to 23							
16	17	18	19	20	21	22	23
M/$\overline{LSB}$	$\overline{Video}$	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
Initialization Bits 24 to 31							
24	25	26	27	28	29	30	31
Icon	Sleep 2	Test 6	Test 5	Test 4	Test 3	Test 2	Test 1

Table 7

Mux ratio (Init. bit 8, 9)		
8	**9**	**mux mode**
0	0	8
0	1	16
1	0	20
1	1	24

Table 8

Init.bit 8-9: Mux mode bits. The multiplex ratio is selected by these two bits. Table 8 shows the corresponding values.
Init.bit 10-11: V_{LCD} temperature coefficient is selected by these two bits. Table 11 shows the corresponding values.
Init.bit 12: Checker bit gives the possibility to force all outputs segments in checked form (see Fig. 10 and Fig. 18.14).
Init.bit 13: Inverse Checker bit gives the possibility to force all outputs segments in inverse checked form (see Fig. 10 and Fig. 18.15).
Init.bit 14: $\overline{Col}$ bit configures the EM6124 on row and column driver or column driver only. In this mode the frame frequency must be external.
Init.bit 15: Row inversion, possibility to inverse the order of the row outputs (see Table 10 and Fig. 18.12).
Init.bit 16: M/$\overline{LSB}$, possibility to inverse the order loading for RAM data (see Fig. 4).
Init.bit 17: $\overline{Video}$ bit, possibility to inverse the content of the RAM. All the 0L pass to 1L and all the 1L pass to 0L (see Fig. 18.11).
Init.bit 18-23: V_{LCD} 64 steps programmation bits. See Fig. 8. Bit 18 (step 1) for MSB and bit 23 (step 6) for LSB.
Init.bit 24: Icon bit adds one line more to the selected mux mode ratio for icon segments outputs.
Init.bit 25: Sleep 2. Set all outputs at V_{SS}.
Init.bit 26-31: Must be setted to 0L.

Reset 1

Power-up: Must be followed by a RESET cycle. After the reset 1 pulse the LCD controller driver is set to the following status:
- All outputs at V_{SS}
- Blank & Set (cmdbits 0,1) = 0L
- Sleep mode (cmdbit 2) = 0L
- RAM address (cmdbits 3 to 7) = 0L
- Multiplex ratio (init.bits 8, 9) = 0L
- Temperature coefficient (init.bits 10,11) = 0L
- Checker & Inv.Checker (init.bits 12, 13) = 0L
- $\overline{Col}$ Mode (init.bit 14) = 1L
- Inv. Row (init.bit 15) = 0L
- M/$\overline{LSB}$ (init.bit 16) = 1L
- $\overline{Video}$ (init.bit 17) = 1L
- V_{LCD} step (init.bits 18 to 23) = 0L
- Icon (init.bit 24) = 0L
- Sleep 2 (init.bit 25) = 1L
- The content of the RAM remains unchanged

An initialization should take place after reset (32 bits sent).

Pin Assignment

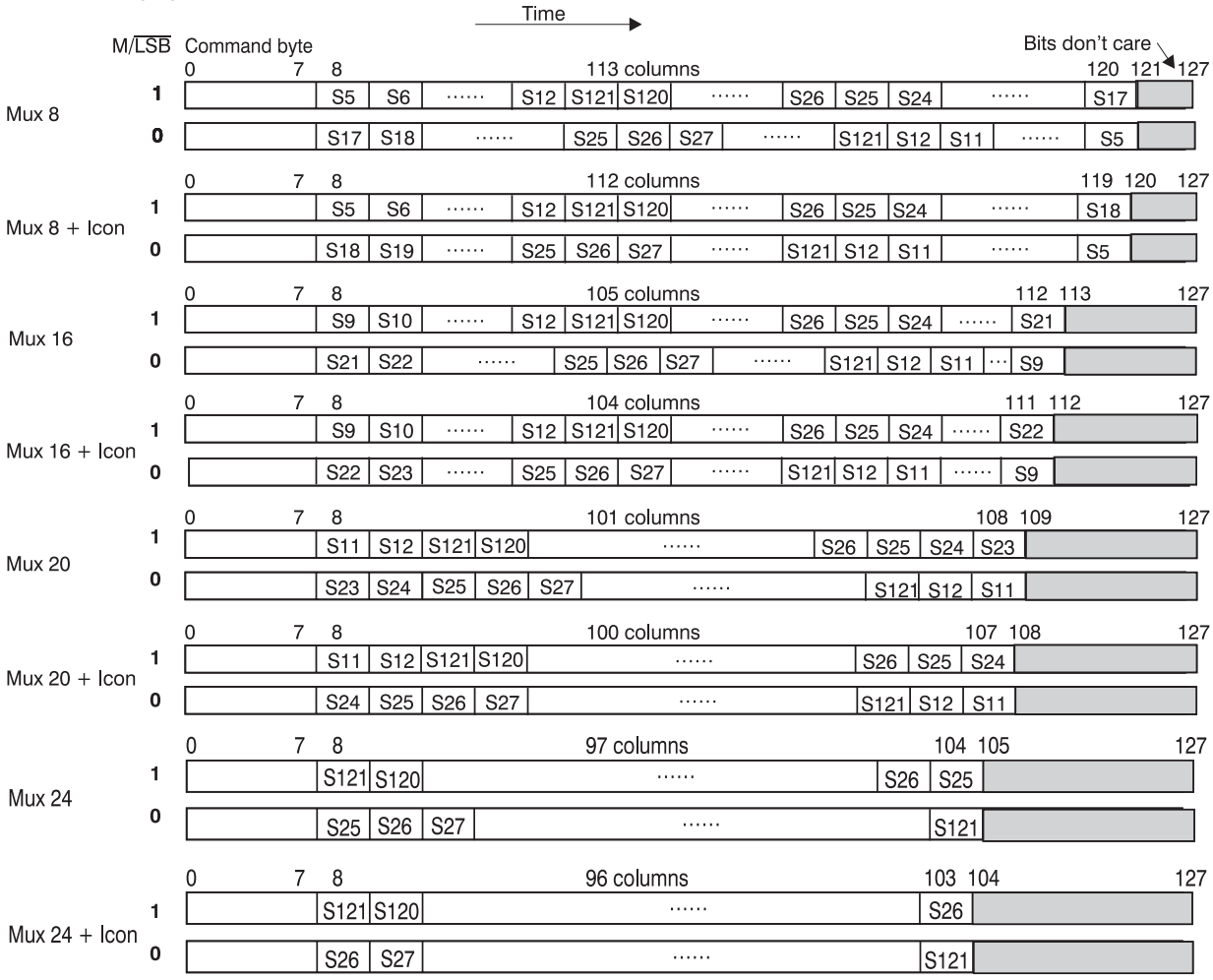
Name	Function
S1...S121	LCD outputs, see Fig.4
FR	AC I/O signal for LCD driver output
DI	Serial data input
DO	Serial data output
$\overline{CLK}$	Data clock input
$\overline{RES1}$	General reset
$\overline{RES2}$	Reset the serial interface counter
V_{LCD}	Internal generated voltage output
V_{DD1}	Power supply for logic
V_{DD2}	Power supply for analogic
V_{HV}	Power supply for high voltage
V_{SS}	Supply GND

Table 9

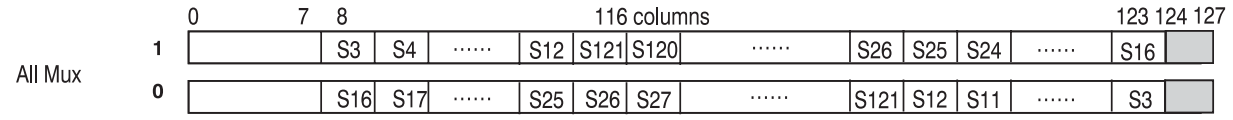
Data Transfer Cycle

1. $\overline{Col}$ inactive (1L)

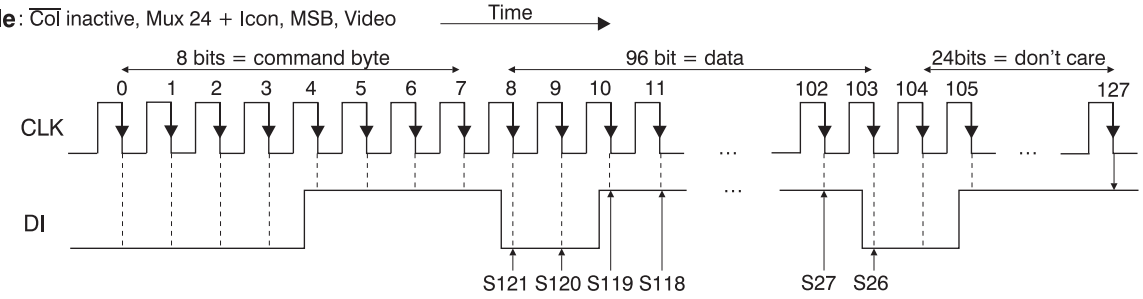
Command byte and display information mode need 128 bit load cycles.



2. $\overline{Col}$ active (0L)



3. Example: $\overline{Col}$ inactive, Mux 24 + Icon, MSB, Video



RAM address = 01111 = S16 (See table 10).
For row connected to pad S16, column connected to pad S119 is "ON", to pad S26 is "OFF".

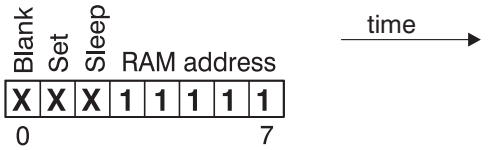
Fig. 4

Output Row Assignments

Row	RAM Address					Mux Mode															
						Mux 8		Mux 8 + Icon		Mux 16		Mux 16 + Icon		Mux 20		Mux 20 + Icon		Mux 24		Mux 24 + Icon	
						Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row	
	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	0	0	0	0	0	S1	S16	S1	S17	S1	S20	S1	S21	S1	S22	S1	S23	S1	S24	S1	S25
2	0	0	0	0	1	S2	S15	S2	S16	S2	S19	S2	S20	S2	S21	S2	S22	S2	S23	S2	S24
3	0	0	0	1	0	S3	S14	S3	S15	S3	S18	S3	S19	S3	S20	S3	S21	S3	S22	S3	S23
4	0	0	0	1	1	S4	S13	S4	S14	S4	S17	S4	S18	S4	S19	S4	S20	S4	S21	S4	S22
5	0	0	1	0	0	S13	S4	S13	S13	S5	S16	S5	S17	S5	S18	S5	S19	S5	S20	S5	S21
6	0	0	1	0	1	S14	S3	S14	S4	S6	S15	S6	S16	S6	S17	S6	S18	S6	S19	S6	S20
7	0	0	1	1	0	S15	S2	S15	S3	S7	S14	S7	S15	S7	S16	S7	S17	S7	S18	S7	S19
8	0	0	1	1	1	S16	S1	S16	S2	S8	S13	S8	S14	S8	S15	S8	S16	S8	S17	S8	S18
9	0	1	0	0	0			S17	S1	S13	S8	S13	S13	S9	S14	S9	S15	S9	S16	S9	S17
10	0	1	0	0	1					S14	S7	S14	S8	S10	S13	S10	S14	S10	S15	S10	S16
11	0	1	0	1	0					S15	S6	S15	S7	S13	S10	S13	S13	S11	S14	S11	S15
12	0	1	0	1	1					S16	S5	S16	S6	S14	S9	S14	S10	S12	S13	S12	S14
13	0	1	1	0	0					S17	S4	S17	S5	S15	S8	S15	S9	S13	S12	S13	S13
14	0	1	1	0	1					S18	S3	S18	S4	S16	S7	S16	S8	S14	S11	S14	S12
15	0	1	1	1	0					S19	S2	S19	S3	S17	S6	S17	S7	S15	S10	S15	S11
16	0	1	1	1	1					S20	S1	S20	S2	S18	S5	S18	S6	S16	S9	S16	S10
17	1	0	0	0	0							S21	S1	S19	S4	S19	S5	S17	S8	S17	S9
18	1	0	0	0	1									S20	S3	S20	S4	S18	S7	S18	S8
19	1	0	0	1	0									S21	S2	S21	S3	S19	S6	S19	S7
20	1	0	0	1	1									S22	S1	S22	S2	S20	S5	S20	S6
21	1	0	1	0	0											S23	S1	S21	S4	S21	S5
22	1	0	1	0	1													S22	S3	S22	S4
23	1	0	1	1	0													S23	S2	S23	S3
24	1	0	1	1	1													S24	S1	S24	S2
25	1	1	0	0	0															S25	S1

Table 10

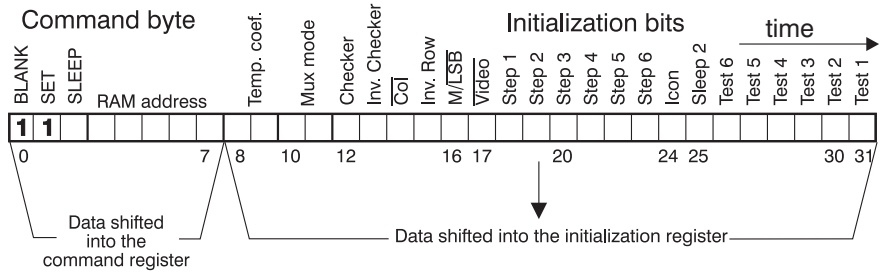
Command Byte Only Mode



In this mode only 8 bits have to be shifted into the EM6124 with address bits to logic 1.

Fig. 5

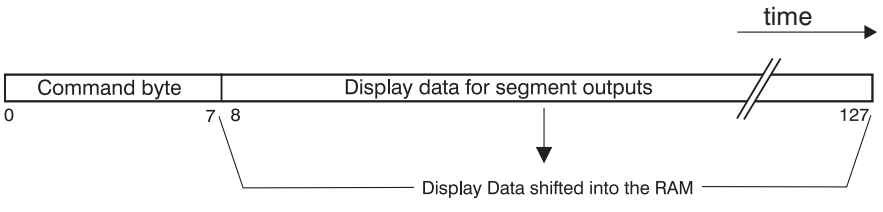
Command Byte and Initialization Mode



In this mode only 32 bits have to be shifted into the EM6124 with bits BLANK and SET to logic 1.

Fig. 6

Command Byte and Display Information Mode



This mode needs 128 bits shifted into the EM6124. Do not introduce one of the two codes which were described above. (All address bits to logic 1 or BLANK and SET bits to 1 simultaneously)

Fig.7

Typical V_{LCD} Programming

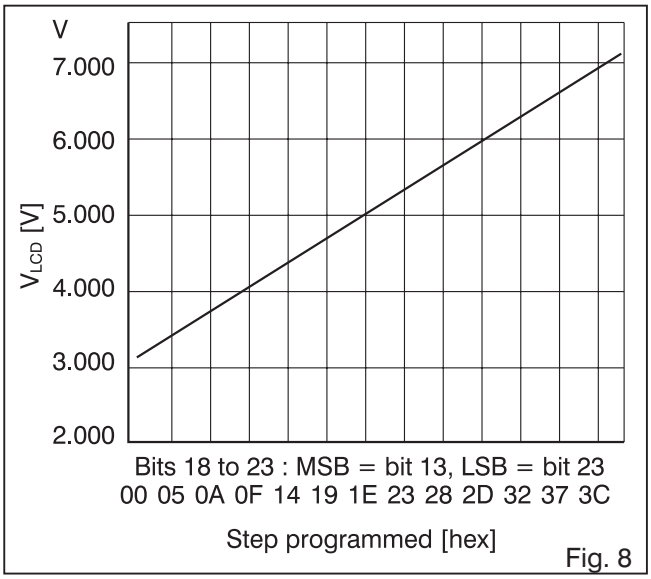


Fig. 8

Temperature Control

Due to the temperature dependency of liquid cristals viscosity the LCD controlling voltage V_{LCD} must be increased for lower temperatures to maintain optimal contrast. The EM6124 is available with 4 different temperature coefficients (see Fig. 9). The coefficient is selected by 2 bits in the initialization code TC bits 10 and 11. Table 11 shows the typical values of the different temperature coefficients. They are proportional to the programmed V_{LCD}.

Typical Values of the Temperature Coefficients

Bit 10, Bit 11	Value	Unit
0 0	- 0.02 x V_{LCD}	mV/°C
0 1	- 0.52 x V_{LCD}	mV/°C
1 0	- 1.16 x V_{LCD}	mV/°C
1 1	- 1.82 x V_{LCD}	mV/°C

Table 11

Temperature Coefficients

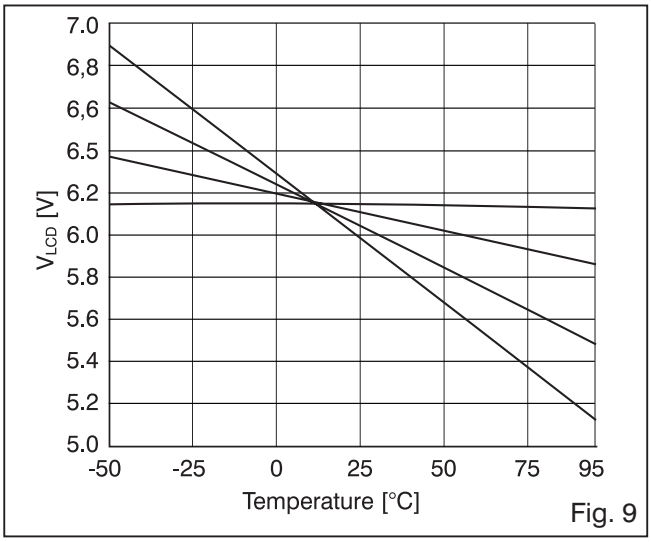


Fig. 9

Checker and Checker Inverse

A fast check display can be easily created setting initialization bits 12 and 13 (called “Checker” and “Inv. Checker”). The display is completely checked with only 2 initialization sequences, one “Checker” and one “Inv. Checker”. For Checker, the pattern fills the display with alternately ON and OFF pixels as shown in Fig. 10. For Inv. Checker, everything is inverted (see Fig.18.14 and 18.15).

Pattern of Checker Mode

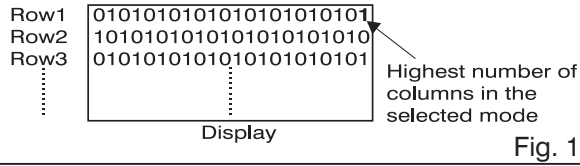
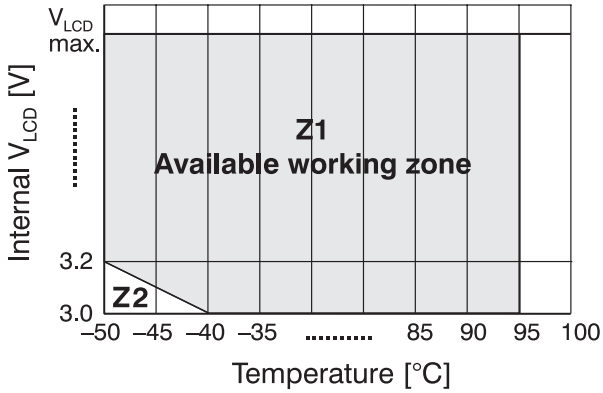


Fig. 10

Internally Generated V_{LCD} versus Temperature



(**Z2** = non available working zone)

Fig. 11

Display Functions

Bit	State	
	Logic 0	**Logic 1**
8 - 9: Mux Mode	See table 8	
10 -11:Temp.Coeff.	See table 11	
12: Checker	Inactive	Chess display
13: Inv. Checker	Inactive	Inverse chess display
14: $\overline{\text{Col}}$	Colum driver only	Row and column driver
15: Inv. Row	Increment rows (example for mux 24: row 1, 2, 3, ... , 24, 1, 2, ...)	Decrement rows (example for mux 24: row 24, 23, 22, ... ,2 ,1, 24, 23, ...)
16: M/$\overline{\text{LSB}}$	Loading in LSB mode	Loading in MSB mode
17: $\overline{\text{Video}}$	Inverse content of RAM	Inactive
18 - 23: V_{LCD} step	See Fig. 8	
24: Icon	Inactive	Add one line more to seledted mux mode
25: Sleep	Inactive	All outputs at V_{SS}
26 - 31:	Must be at 0L	

Table 12

Block Diagram

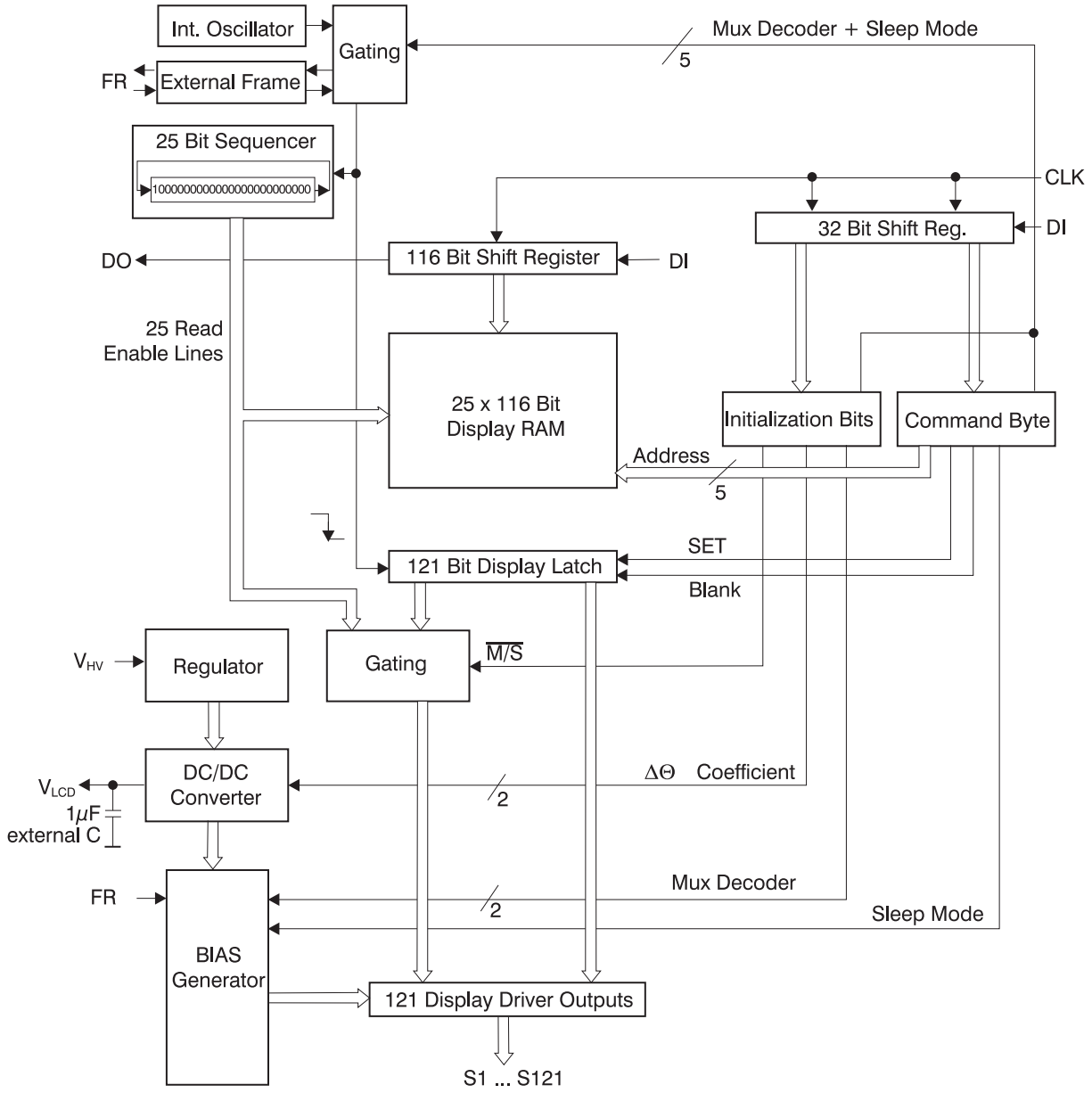


Fig. 12

LCD Voltage Bias Levels

LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}}{V_{OFF}\ (rms)}$	$\frac{V_{ON}\ (rms)}{V_{OFF}\ (rms)}$
EM6124 (24) n=24 1:24 MUX	6 Levels	$\sqrt{\frac{\sqrt{n}\,(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}} = 4.68$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 1.230$
EM6124 (20) n=20 1:20 MUX	6 Levels	$\sqrt{\frac{\sqrt{n}\,(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}} = 4.39$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 1.255$
EM6124 (16) n=16 1:16 MUX	1/5 Bias 6 Levels	$\sqrt{\frac{\sqrt{n}\,(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}} = 4.08$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 1.291$
EM6124 (8) n=8 1:8 MUX	1/4 Bias 5 Levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n-15}{n+3}} = 1.446$

Table 13

Optimum LCD Bias Voltages

Multiplex Rate	V_{LCD}	V1	V2	V3	V4	V_{SS}
1 : 24	1	0.830	0.660	0.340	0.170	0
1 : 20	1	0.817	0.634	0.366	0.183	0
1 : 16	1	0.800	0.600	0.400	0.200	0
1 : 8	1	0.750	0.500	0.250	-	0

V_{LCD} > V1 > V2 > V3 > V4 >V_{SS}

The values in the above table are given in reference to V_{LCD} e.g. 0.5 means 0.5 x V_{LCD}

Table 14

Row and Column Multiplexing Waveform EM6124 (8)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

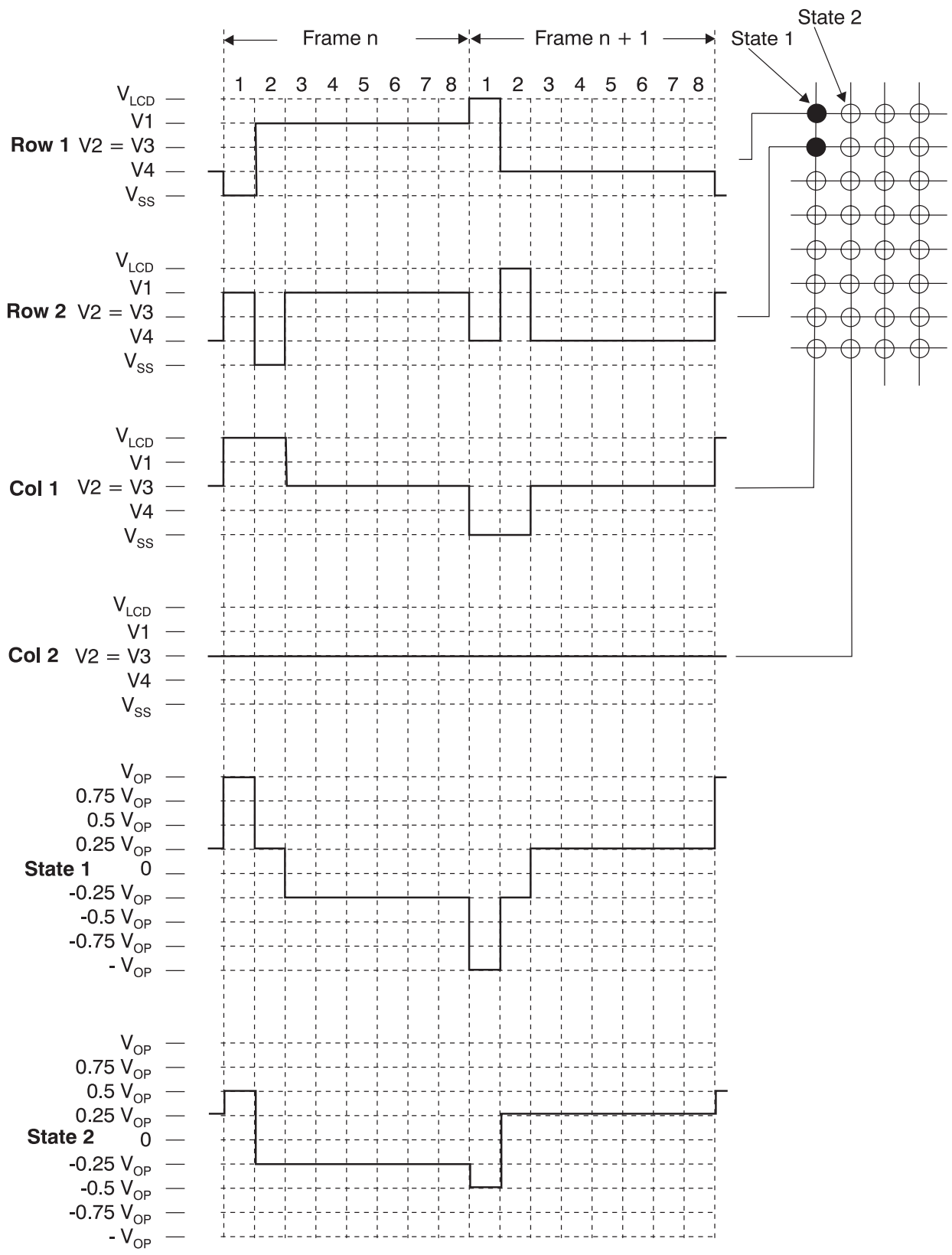


Fig. 13

Row and Column Multiplexing Waveform EM6124 (16)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

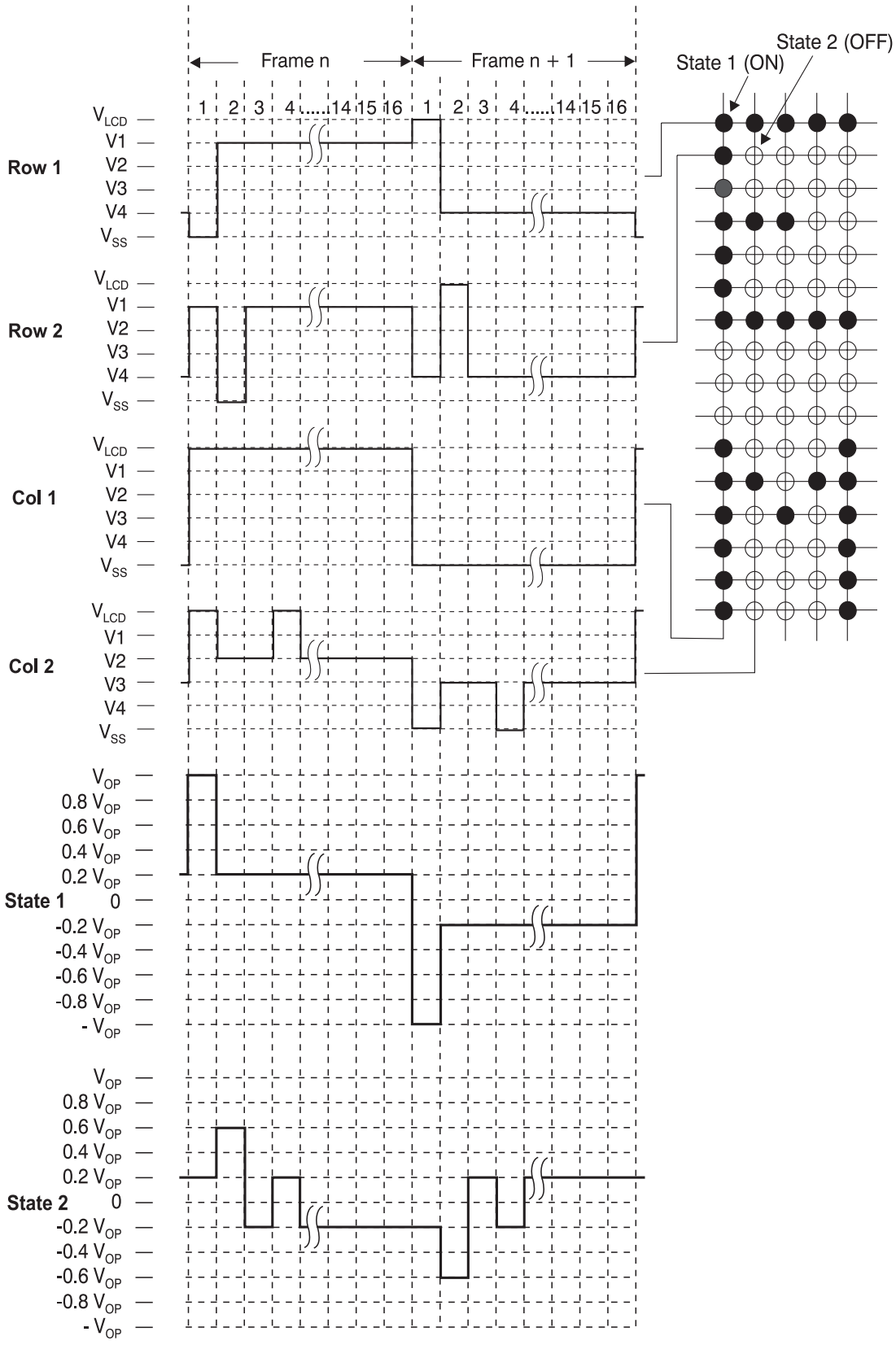


Fig. 14

Row and Column Multiplexing Waveform EM6124 (20)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

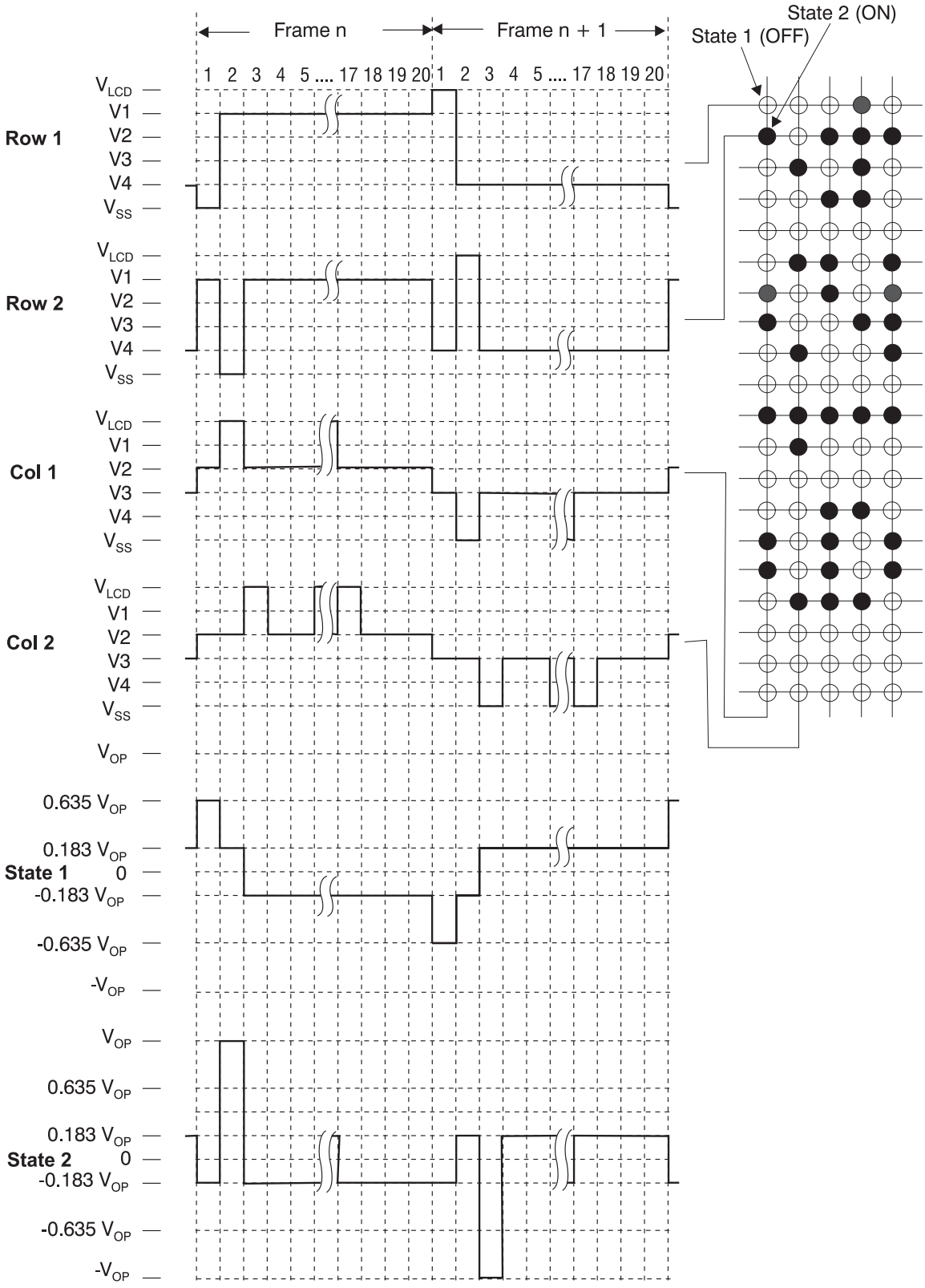


Fig. 15

Row and Column Multiplexing Waveform EM6124 (24)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

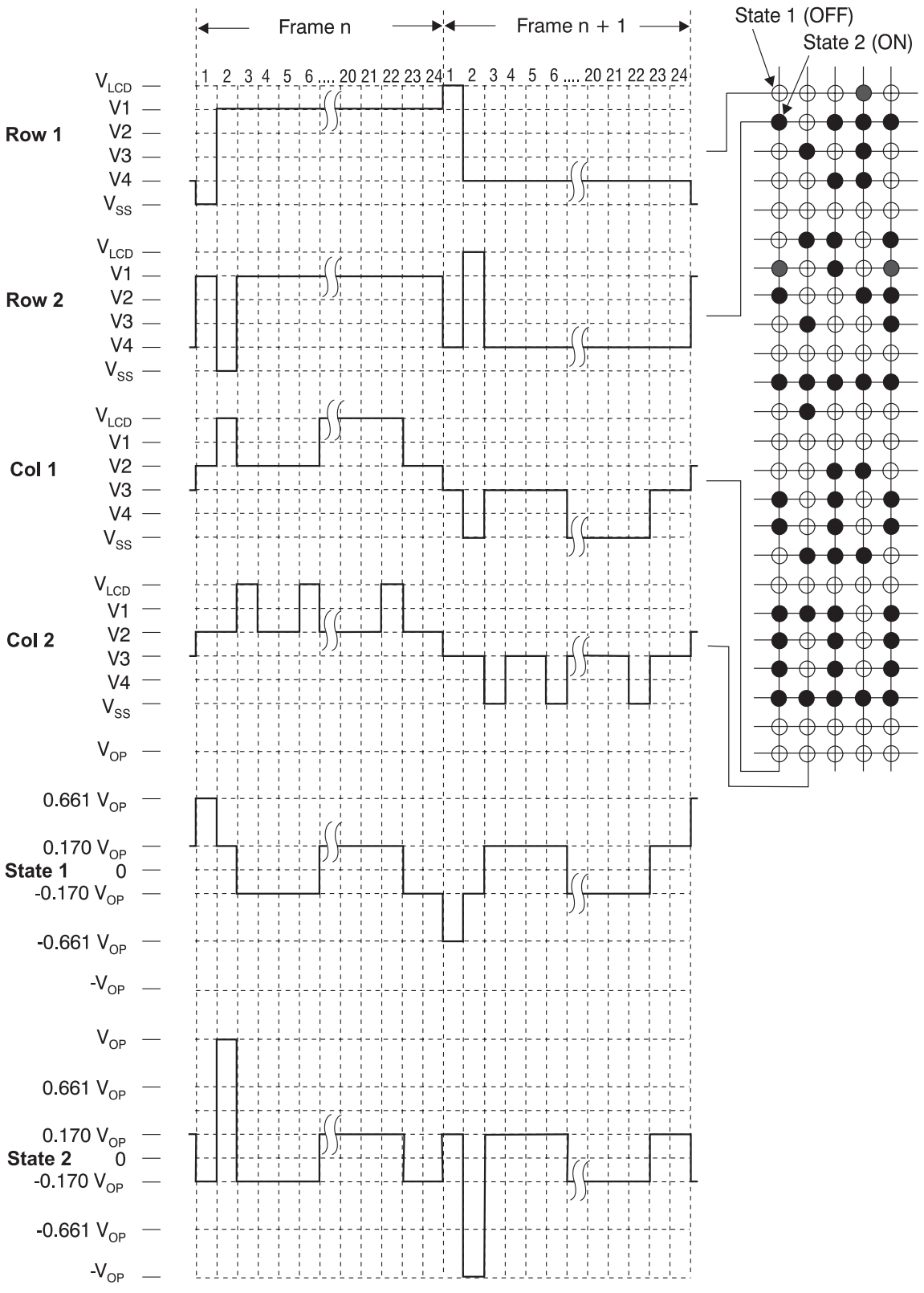


Fig. 16

Functional Description

Supply Voltage V_{DD1}, V_{DD2}, VH_V, V_{LCD}, V_{SS}
The voltage between V_{DD1} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{DD2} and V_{SS} is the supply voltage for the analogic. V_{DD1} and V_{DD2} must be the same voltage and, in order to guarantee the best functioning, V_{DD1} and V_{DD2} have to be separately connected to the PCB (see Fig. 19). The voltage V_{LCD} is internally generated for the supply voltage of the LCD and is used for the generation of the internal LCD bias level. An external capacitor of 1 μF must be connected between V_{LCD} and V_{SS}. Table 15 shows the relationship between V1, V2, V3, V4 for a programmed multiplex rate. Note that $V_{LCD} > V1 > V2 > V3 > V_{SS}$ for the EM6124 8 mux programmed, and for the EM6124 16, 20, 24 mux programmed $V_{LCD} > V1 > V2 > V3 > V4 > V_{SS}$. The voltage between V_{HV} and V_{SS} is the supply voltage for high voltage part of the EM6124. An external V_{LCD} may also be used by connecting a power supply and programming a lower V_{LCD} voltage during initialization.

Data Input
The data input pin, DI, is used to load serial data into the EM6124. The normal serial data word length is128 bits. 32 and 8 bits are also available in a special mode (see 1 Bit Interface Description). The command byte is loaded first and then the segment data bits (see Fig. 4).

$\overline{\text{RES1}}$ Input
Reset is accomplished by applying an external $\overline{\text{RES1}}$ pulse (active low). When reset occurs within the specified time, all internal register are reset however the content of the RAM is still unchanged. The state after reset is described on page 4.

$\overline{\text{RES2}}$ Input
Reset is accomplished by applying an external $\overline{\text{RES2}}$ pulse (active low). When reset occurs within the specified time, the internal counter for serial interface is reset. The counter of the serial interface for data inputs is ready for a new loading of data. This reset 2 does not change the content of the RAM neither the content of the command and the initialization bits. To avoid trouble in case of software interrupt of the MPU during data loading, this function can be used.

Power-Up
On power up the data in the shift registers, the display RAM, the sequencer driving the 8/16/20/24 rows and the 121 bit display latches are undefined.

CLK Input
The clock input is used to clock the DI serial data into the EM6124.

FR Input / Output
The frame frequency is realized by an internal oscillator with a typical value of 75 Hz. The internal row frequency changes with the number of rows (F_{row} = 75 x n, where n = 8, 16, 20, 24). When bit 14 ($\overline{\text{Col}}$) is inactive (active low), the frame frequency is given by the internal oscillator. This frequency can be measured on the I/O FR. When bit 14 ($\overline{\text{Col}}$) is active (active low), the frame frequency is external then the frequency is given directly by the FR input to the row and column driver (see Fig. 16 and 17 for more details concerning the frame frequency).

Driver Outputs S1 to S116
There are 121 LCD driver outputs on the EM6124. The output assignments depend on the chosen mux mode ratio (init. bits 8, 9) and the Col function (init. bit 14).
When init. bit 14 (Col) is active, all 116 outputs function as column drivers. Table “Output Row Assignments” and Fig. 4 describe exactly the correspondent data to the output of the chip. There is one to one relationship between the display RAM and the LCD driver outputs. Each pixel (segment) driven by the EM6124 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the pixel “on” and Clearing it turns “off”.
For chip-on-glass better performances can be obtained by covering the backside of the chip.

Typical Frame Frequency at V_{DD} = 3 V

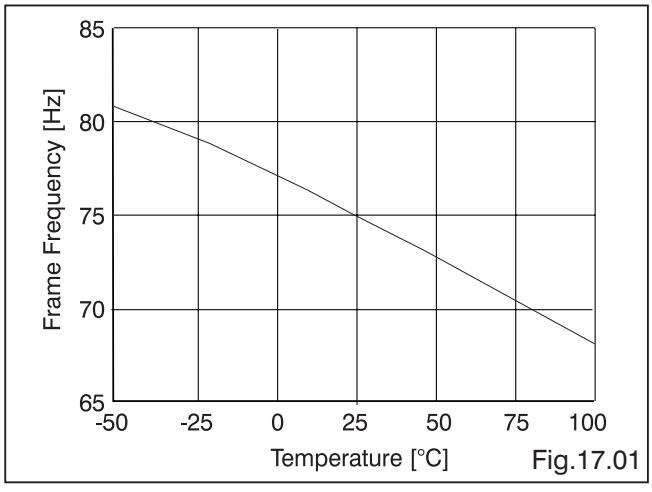


Fig.17.01

Typical Frame Frequency at T_A = 25 °C

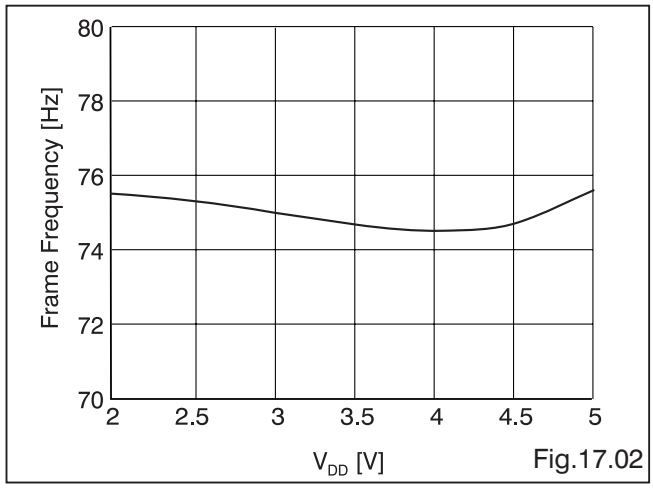


Fig.17.02

Application Example

These tables/figures show how to use the EM6124 with a given initialization. Rows “Data” show the logical value to affect pad DI for each falling edge of pad CLK. A reset cycle pad RES1 at OL is required before sending data.

Command byte	Initialization bits or display data

First Initialization

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0

Description

Bits 0,1=1,1 :
initialization is programmed
Bit 2=0 :
no sleep mode
Bits 3 to 7 :
don't care in this case
(not 11111)

Bits 8,9,24 = 1,1,1 : mux mode 24 + icon ; 25 rows driven.
Bits 10,11 = 0,1 : temperature coefficient = $-(0.52 \bullet V_{LCD})$ mV/°C
Bits 12,13 = 0,0 : no checker or inv. checker functions
Bit 14 = 1 : row and column driver configuration
Bit 15 = 0 : row 1 of the RAM displayed on S1, row 2 on S2, … and row 25 on S25.
Bit 16 = 0 : first data sent displayed on S26, last one on S121
Bit 17 = 1 : 1L in the RAM corresponds to a pixel "ON"
Bits 18 to 23 = 1,1,0,0,0,0 :
programmed $V_{LCD} = 3.15 + (1 \bullet 32 + 1 \bullet 16 + 0 \bullet 8 + 0 \bullet 4 + 0 \bullet 2 + 0 \bullet 1) \bullet 0.0625 =$ 6.150 V
Bit 25 = 0 : no sleep 2
Bits 26 to 31 = 0,0,0,0,0,0 : every test bits must be set to 0.

Result

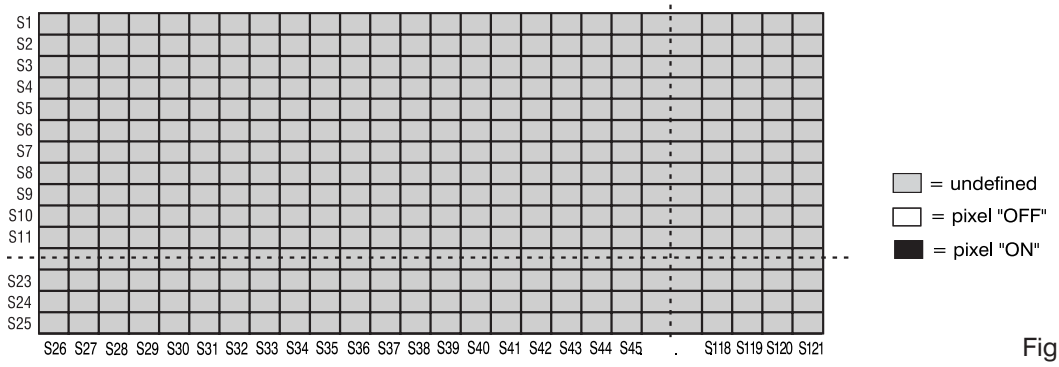


Fig. 18.01

Write Row 1

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	.....	0	0	0

Description

Bits 0,1,2= 0,0,0:
no set, no blank, no sleep
Bits 3 to 7 = 0,0,0,0,0: :
data sent to row 1 of the RAM

Bits 8 to 103 = 0,0,..., 0: first row of the RAM is loaded with 0,0,..., 0
Bits 104 to 127 = don’t care

Result

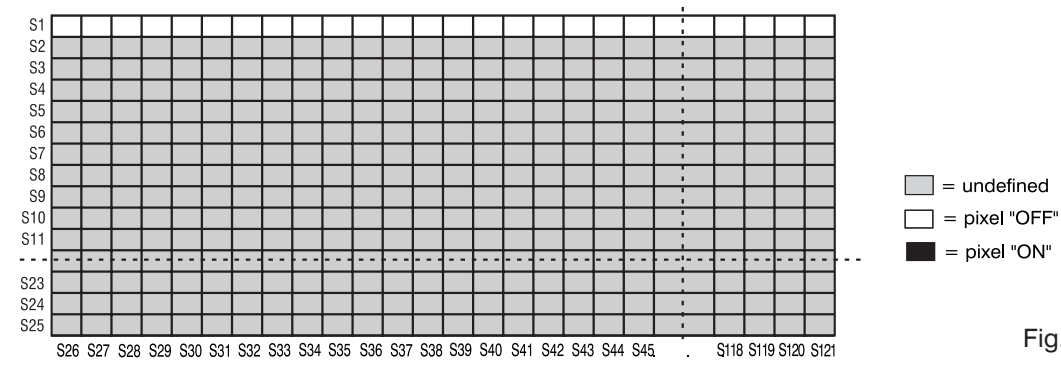


Fig. 18.02

Table 15
(continued on next pages)

Application example continued

	Command byte	Initialization bits or display data

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	0	0	1	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	.....	0	0	0

Description

Bits 0,1,2= 0,0,0: no set, no blank, no sleep
Bits 3 to 7 = 0,0,0,0,1: : data sent to row 2 of the RAM

Second row of the RAM is loaded

Result

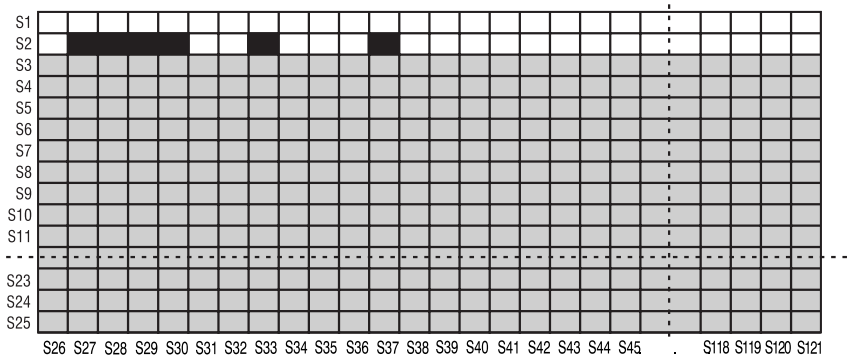


Fig. 18.03

Write Row 2

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	.....	0	0	0

Description

Bits 0,1,2= 0,0,0: no set, no blank, no sleep
Bits 3 to 7 = 0,0,0,1,0: : data sent to row 3 of the RAM

3rd row of the RAM is loaded

Result

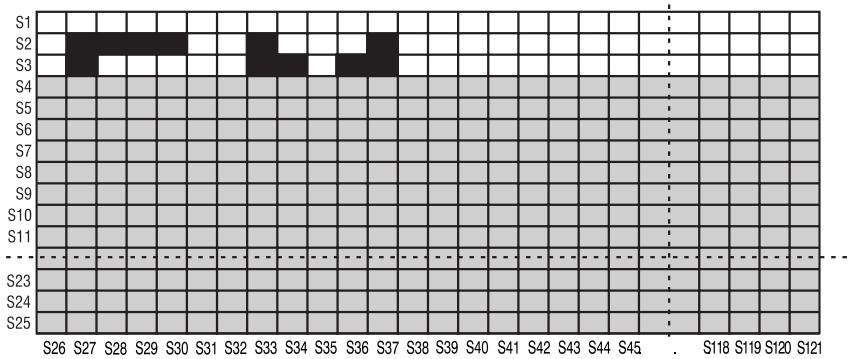


Fig. 18.04

Write Row 3

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	.....	125	126	127
Data	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	.....	0	0	0

Description

Bits 0,1,2= 0,0,0: no set, no blank, no sleep
Bits 3 to 7 = 0,0,0,1,1: : data sent to row 4 of the RAM

4th row of the RAM is loaded

Result

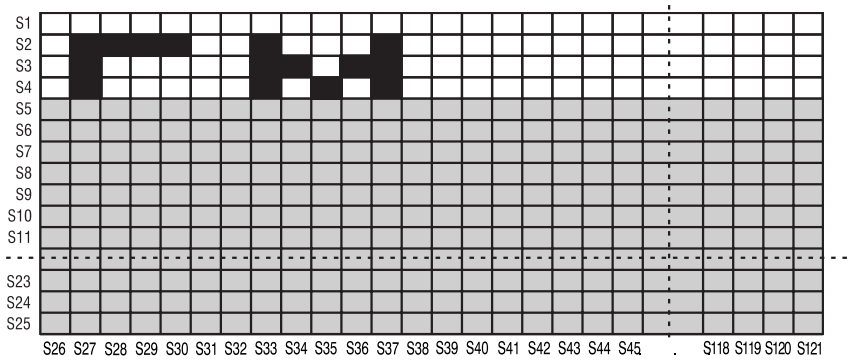


Fig. 18.05

Write Row 4

Application example continued

	Command byte	Initialization bits or display data

Write Row 5

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	.....	0	0	0

Description: **Bits 0,1,2**= 0,0,0: no set, no blank, no sleep **Bits 3 to 7** = 0,0,1,0,0: : data sent to row 5 of the RAM

5th row of the RAM is loaded

Result

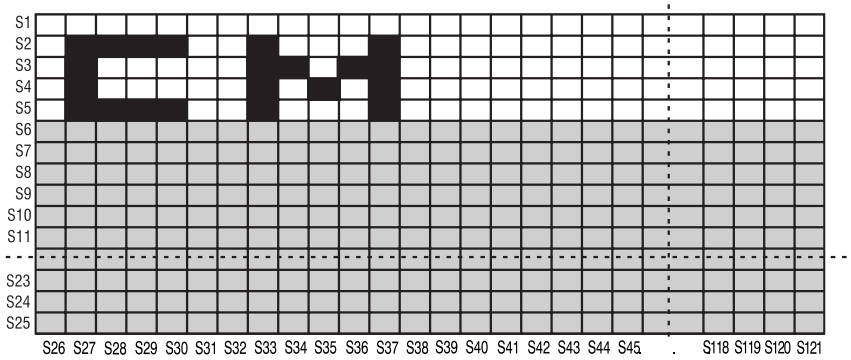


Fig. 18.06

Write Row 6

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	.....	0	0	0

Description: **Bits 0,1,2**= 0,0,0: no set, no blank, no sleep **Bits 3 to 7** = 0,0,1,0,1: : data sent to row 6 of the RAM

6th row of the RAM is loaded

Result

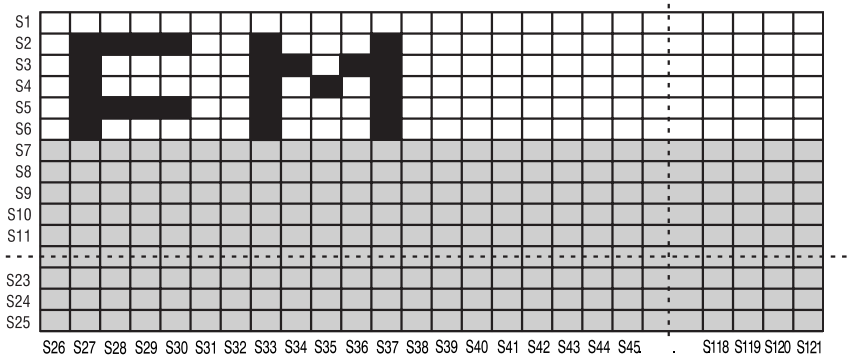


Fig. 18.07

Write Row 7

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	.....	0	0	0

Description: **Bits 0,1,2**= 0,0,0: no set, no blank, no sleep **Bits 3 to 7** = 0,0,1,1,0: : data sent to row 7 of the RAM

7th row of the RAM is loaded

Result

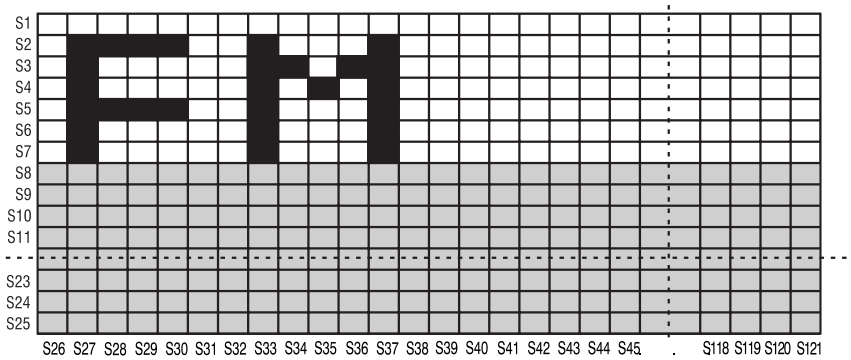


Fig. 18.08

Application example continued

	Command byte	Initialization bits or display data

Write Row 8

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	0	1	1	1	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	.....	0	0	0

Description:
Bits 0,1,2= 0,0,0: no set, no blank, no sleep
Bits 3 to 7 = 0,0,1,1,1: : data sent to row 8 of the RAM

8th row of the RAM is loaded

Result

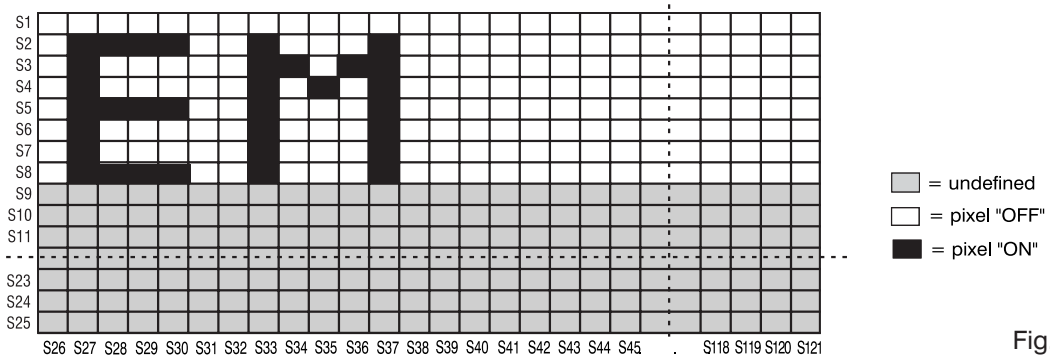


Fig.18.09

Write Row 9

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	.....	125	126	127
Data	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	.....	0	0	0

Description:
Bits 0,1,2= 0,0,0: no set, no blank, no sleep
Bits 3 to 7 = 0,1,0,0,0: : data sent to row 9 of the RAM

9th row of the RAM is loaded

Result

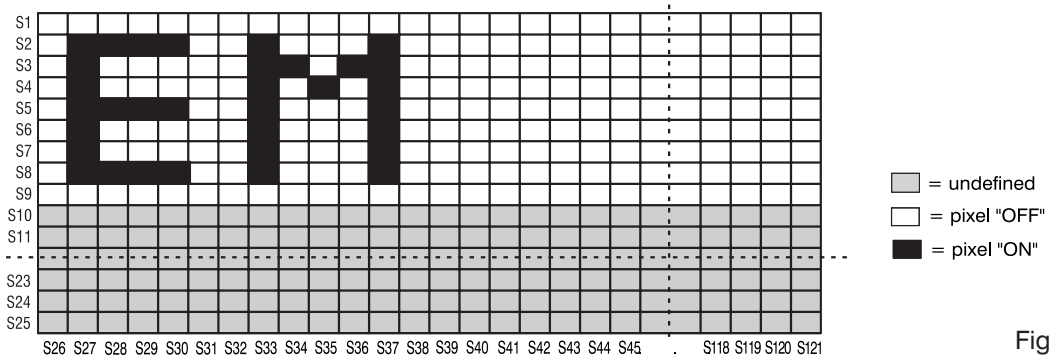


Fig.18.10

Initialization in Video Inverse Mode

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0

Description:
Bits 0,1 = 1,1 : initialization is programmed
Bit 2 = 0
Bits 3 to 7 : don't care in this case (not 1,1,1,1,1)

Bit 17 = 0: 1L in the RAM corresponds to a pixel "OFF"

Result

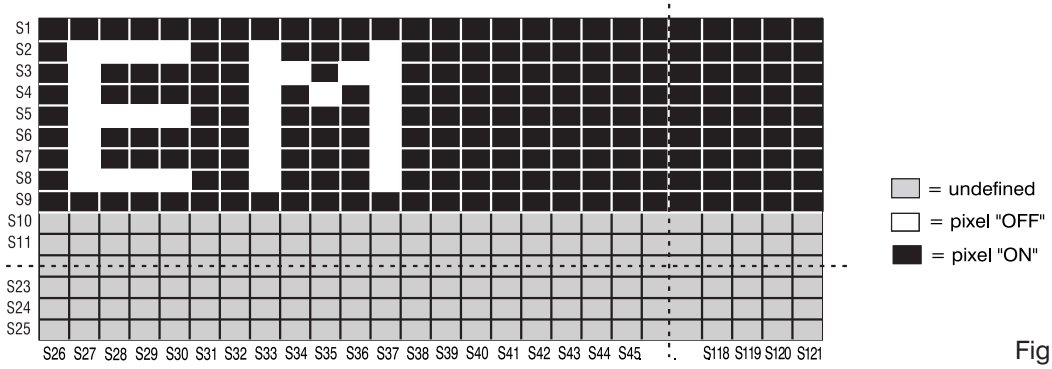


Fig.18.11

Application example continued

	Command byte	Initialization bits or display data

Initialization in Inverse Row Mode

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0

Description

Bits 0,1 = 1,1 :
initialization is programmed
Bit 2 = 0 : no sleep mode
Bits 3 to 7 : don't care in this case (not 11111)

$\overline{\text{Bit}}$ 17 = 1 : 1L in the RAM corresponds to a pixel "ON"
$\overline{\text{Bit}}$ 15 = 1 : row 1 (address '00000') displayed on S25,
row 2 (address '00001') displayed S24,
....., row 25 (address '11000') displayed on S1

Result

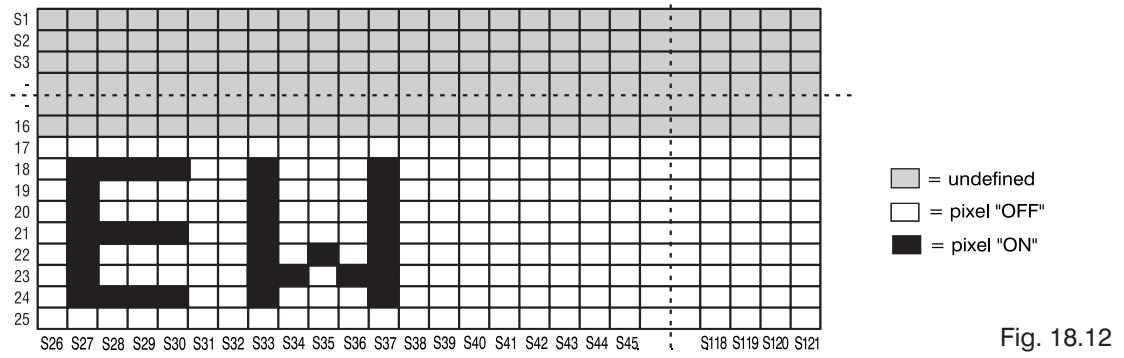


Fig. 18.12

Initialization to Change V_{LCD} (Contrast)

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0

Description

Bits 0,1,= 1,1 :
initialization is programmed
Bit 2 = 0 : no sleep mode
Bits 3 to 7 : don't care in this case (not 11111)

Bit 15 = 1 : row 1 (address '00000') displayed on S25, row 2 (address '00001') displayed S24,
.....,and row 25 (address '11000') displayed on S1
$\overline{\text{Bit}}$ 17 = 1 : 1L in the RAM corresponds to a pixel "ON"
Bits 18 to 23 = 1,0,1,0,0,0 :
programmed V_{LCD} = 3.15 + (1•32+0•16+1•8+0•4+0•2+0•1)•0.0625 = 5.650 V

Result

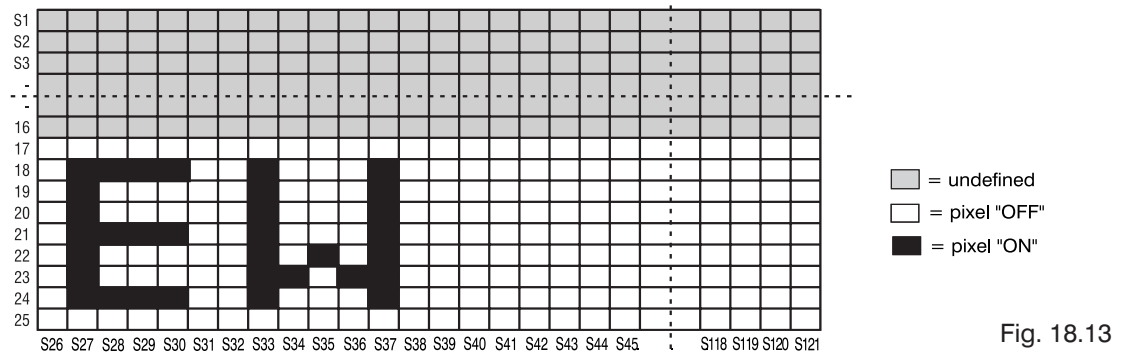


Fig. 18.13

Initialization in Checker Mode

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0

Description

Bits 0,1 = 1,1 :
initialization is programmed
Bit 2 = 0
Bits 3 to 7 : don't care in this case (not 1,1,1,1,1)

Bit 12 = 1 : checker pattern on the LCD, don't care for the RAM
Bit 17 = 1 : 1L in the RAM corresponds to a pixel "ON"

Result

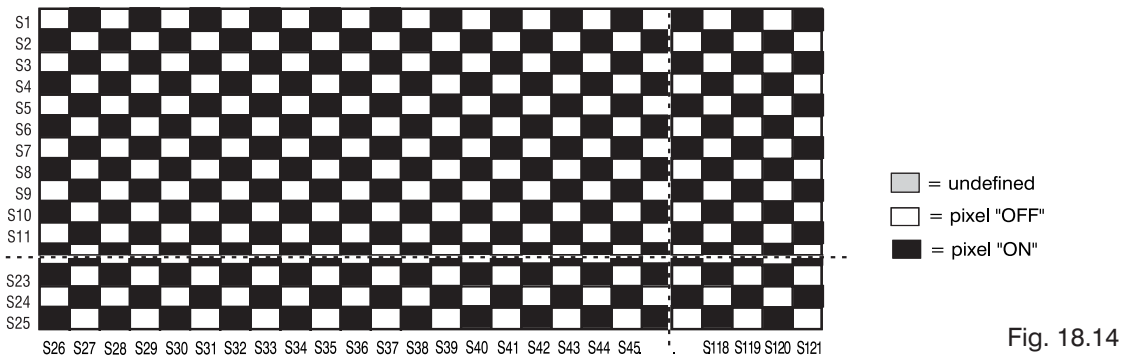


Fig. 18.14

Application example continued

Command byte	Initialization bits or display data

Initialization in Inverse Checker Mode

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	0	1	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0

Description

Bits 0,1 = 1,1 : initialization is programmed
Bit 2 = 0
Bits 3 to 7 : don't care in this case (not 1,1,1,1,1)

Bit 13 = 1 : checker pattern on the LCD, don't care for the RAM
Bit 17 = 1 : 1L in the RAM corresponds to a pixel "ON"

Result

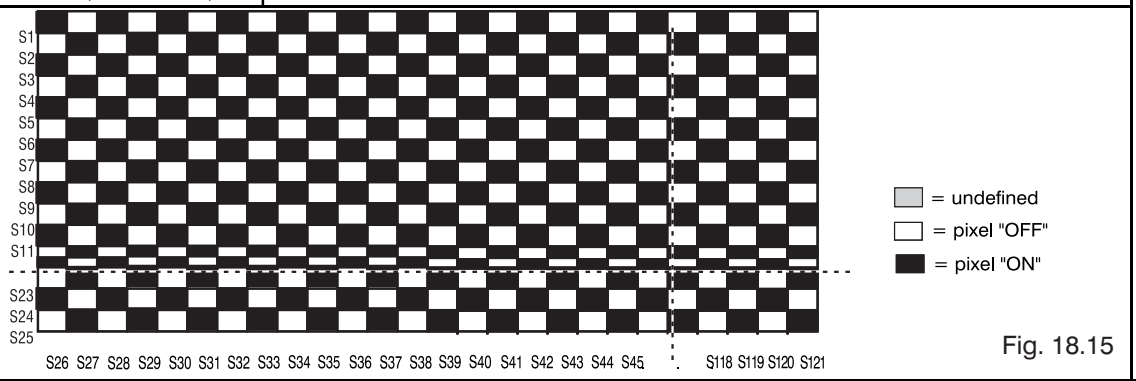


Fig. 18.15

Command Byte only: Set

Bit No	0	1	2	3	4	5	6	7
Data	0	1	0	1	1	1	1	1

Description

Bits 0,1 = 0,1 : blank is programmed
Bit 2 = 0
Bits 3 to 7 = 1,1,1,1,1 : command byte only mode

Result

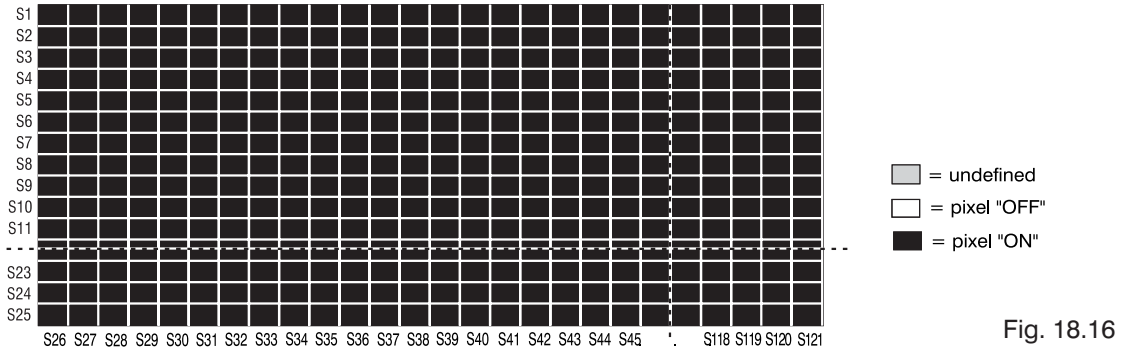


Fig. 18.16

Command Byte only: Blank

Bit No	0	1	2	3	4	5	6	7
Data	1	0	0	1	1	1	1	1

Description

Bits 0,1 = 1,0 : b lank is programmed
Bit 2 = 0
Bits 3 to 7 = 1,1,1,1,1 : command byte only mode

Result

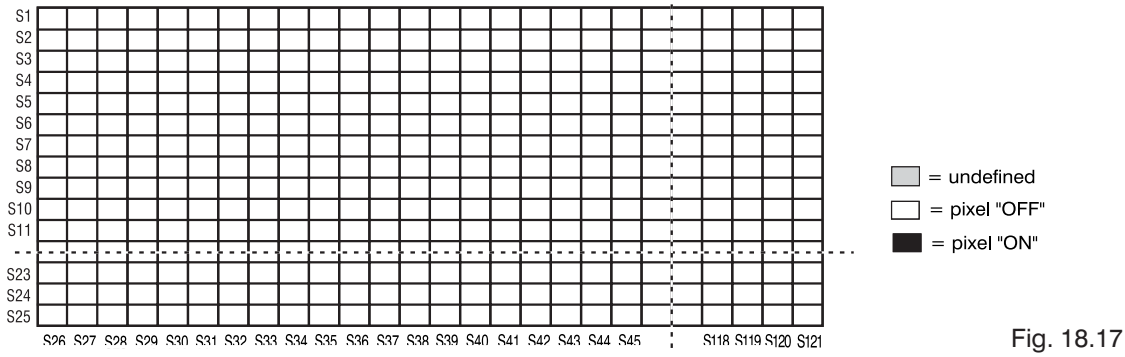
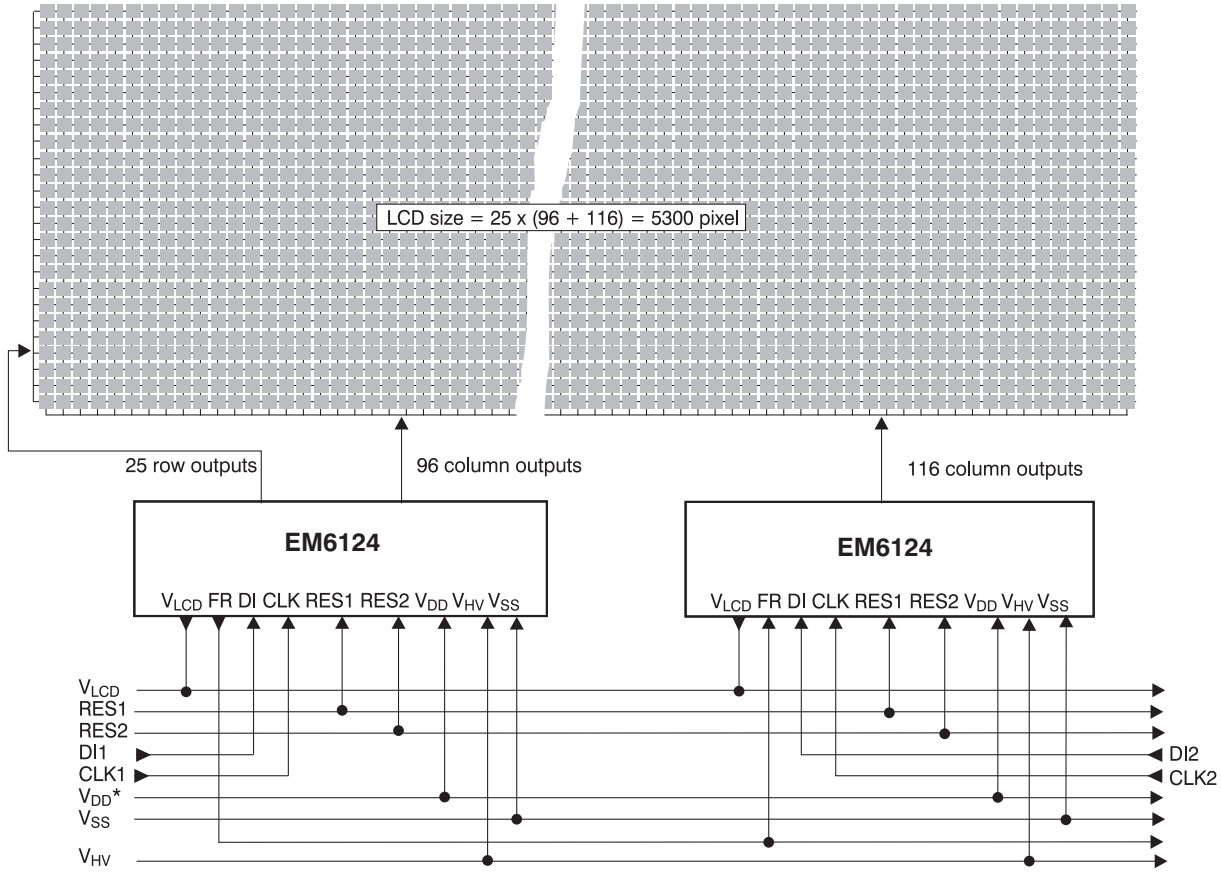


Fig. 18.17

Applications

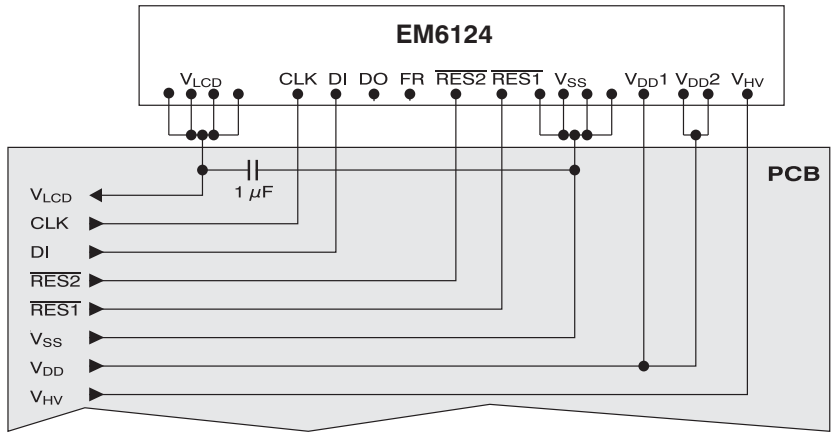
Two EM6124 work in parallel to drive up to 50 rows x 96 columns or 25 rows x 212 columns as below



By connecting the V_{LCD} bias outputs as shown, the pixel load is averaged across all the drivers. The effective bias level source impedance is the parallel combination of the total number of drivers.
* V_{DD1} and V_{DD2} have been connected together.

Fig. 19

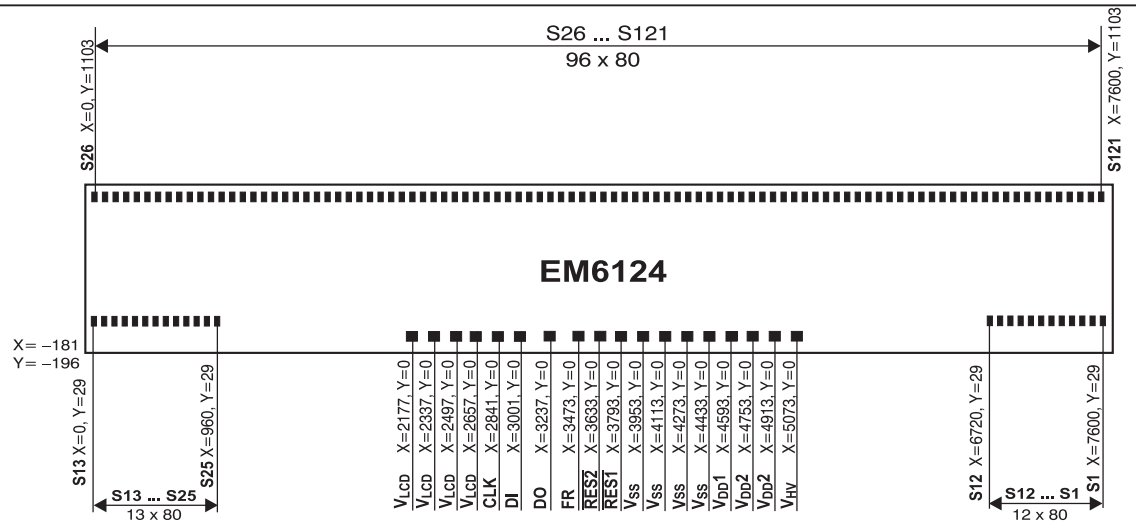
Contacting Power Supply



In order to guarantee the best functioning $V_{DD}1$ and $V_{DD}2$ have to be connected separtely on the PCB, if possible.

Fig. 20

Dimensions of Chip Form and Bumped Die



All dimensions in micron

Thickness: 15 mils
Bump size: LCD output pads = 50 x 100 micron, Input/output pads = 102 x 102 micron
Bump height: 17.5 micron
Bump hardness: 50 Vickers
Chip size: [X x Y] 7930 x 1493 micron or 312 x 59 mils
Note: The origin (0,0) is the lower left coordinate of center pads.
The lower left corner of the chip shows distances to origin.

Fig. 21

Ordering Information

When ordering, please specify the complete Part Number

Part Number	Die Form	Bumping
EM6124WP15E	Die in waffle pack, 15 mils thickness	With gold bumps

For other delivery form in die (with or without bumps), please contact EM Microelectronic-Marin S.A. Minimum order quantity might apply.