Preliminary

GENERAL DESCRIPTION

The EM65160 is a 160-channel output common and segment driver LSI for driving large scale STN dot matrix LCD (liquid crystal display) panel using as PDA, computers and workstation. Since this product can be used as segment or common driver, a LCD panel can be configured only with this product. Through the use of SST (super slim TCP) technology, it is deal for substantially decreasing the size of LCD module frame.

In common driver mode, it can be selected in single mode and dual mode by a mode pin (MD), data input/output pins are bi-directional, four data shift direction are pin selectable.

In segment driver mode, it can be selected 4-bit parallel input mode or 8-bit parallel input mode by a mode pin (MD).

FEATURES

Both common mode and segment mode

- Display duty application: up to 1/480 duty
- Supply voltage for the logic system: +2.5 to +5.5V
- Supply voltage for LCD driver: +15 to +42V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- CMOS silicon process (P-type Silicon substrate)
- 186 pin TCP (tape carrier package) package
- Built-in display-off function: when /DSPOF is “L”, all LCD drive output remain at the V_{SS} level.

Common Mode

- Shift clock frequency: 4.0MHz (Max.)
- Built-in 160 bits bi-directional shift register (divisible into 80bits*2)
- Available in a single mode or in a dual mode
- Data input/output pins are bi-directional, four data shift direction are pin selectable.
- Shift register circuit reset function when /DSPOF active

Segment mode

- Shift clock frequency: 14MHz(Max.) (V_{DD}=+5V ± 10%)
- 8MHz(Max.) (V_{DD}=+2.5V to +4.5V)
- Adopts a data bus system
- 4-bits/8-bits parallel input mode are selected by mode pin (MD)
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select, causes the internal clock to be stopped by automatically counting 160 of input data
- Line latch circuit reset function when /DSPOF active

Preliminary

PIN ARRANGEMENT

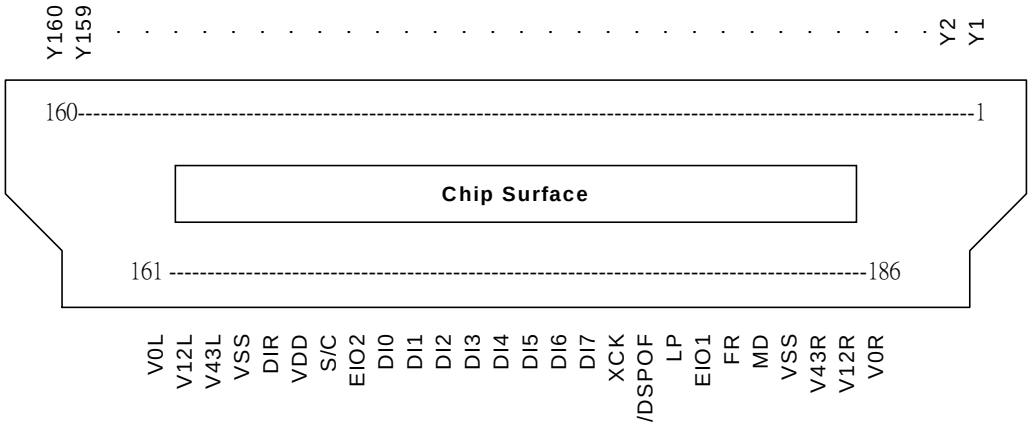


Figure-1 Pin Arrangement

BLOCK DIAGRAM

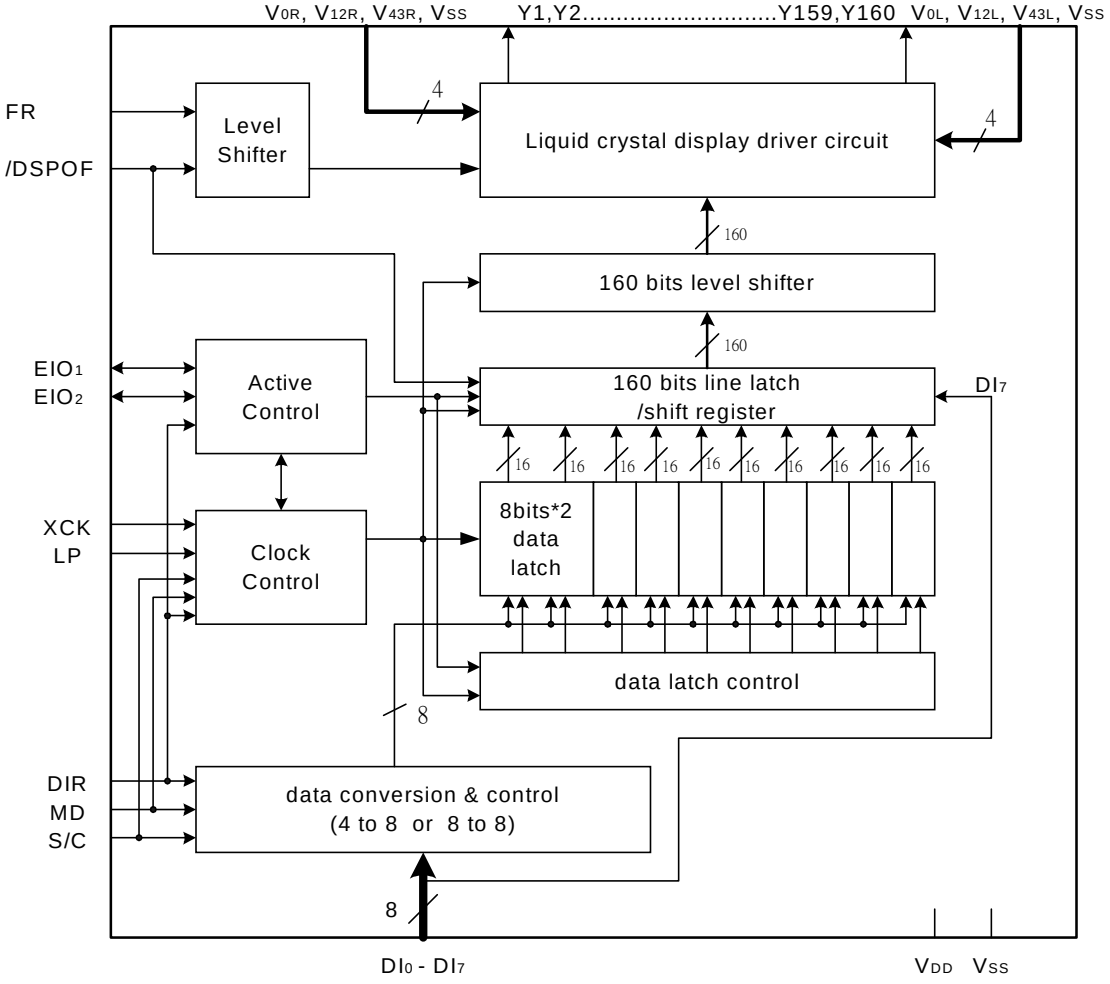


Figure-2 Block Diagram

Preliminary

PIN DESCRIPTION

Table-1 Pin Arrangement

Pin NO.	*Symbol*	*I/O*	*Description*
1 to 160	Y_1 -Y_{160}	O	LCD driver output
161,186	V_{OL}, V_{OR}	-	Power supply for LCD driver
162,185	V_{12L}, V_{12R}	-	Power supply for LCD driver
163,184	V_{43L}, V_{43R}	-	Power supply for LCD driver
165	DIR	I	Display data shift direction selection
166	V_{DD}	-	Power supply for logic system
167	S/C	I	Segment/common mode selection
168 180	EIO_2 EIO_1	I/O	Input /output for chip select or data of shift register
169 to 176	DI_0 – DI_7 DI_7	I	Display data input for segment mode Dual mode data input for common mode
177	XCK	I	Display data shift clock input for segment mode
178	/DSPOF	I	Control input for deselect output level
179	LP	I	Latch pulse input/shift clock input for shift register
181	FR	I	AC-converting signal input for LCD driver waveform
182	MD	I	Mode selection input
164,183	V_{SS}	-	Ground (0 V)

Segment Mode

Table-2 Pin Functions Of Segment Mode

<table>
<tr><th>Symbol</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>V_{DD}</td><td>I</td><td>Power Supply</td><td>Power supply for internal logic connects to +2.5 to +5.5V</td></tr>
<tr><td>V_{SS}</td><td>I</td><td>GND</td><td>Connect to Ground</td></tr>
<tr><td>V_{0R}，V_{0L}
V_{12R}，V_{12L}
V_{43R}，V_{43L}</td><td>I</td><td>Power Supply</td><td>Power supply for LCD driver level
• Normally，the bias voltage used is set by resistor divider
• Ensure that the voltage are set such that $V_{ss} < V_{43} < V_{12} < V_0$
• To further reduce the difference between the output waveforms of LCD driver output pin Y_1 and Y_{160}，externally connect V_{iR} and V_{iL} (i=0,12,43)</td></tr>
<tr><td>DI_0 – DI_7</td><td>I</td><td>Controller</td><td>Input for display data
• In 4-bit parallel input mode，input data into DI_0 – DI_3, connect DI_4 – DI_7 to V_{SS} or V_{DD}
• In 8-bit parallel input mode，input data into DI_0 – DI_7</td></tr>
<tr><td>XCK</td><td>I</td><td>Controller</td><td>Clock signal for taking display data
Data is read on the falling of the clock pulse</td></tr>
<tr><td>LP</td><td>I</td><td>Controller</td><td>Latch signal for display data
• Data is latched on the falling edge of the clock pulse</td></tr>
<tr><td>S/C</td><td>I</td><td>V_{SS}/V_{DD}</td><td>Selection of segment mode/common mode
<table>
<tr><th>S/C</th><th>Mode selection</th></tr>
<tr><td>H</td><td>Segment mode</td></tr>
<tr><td>L</td><td>Common mode</td></tr>
</table></td></tr>
<tr><td>DIR</td><td>I</td><td>V_{SS}/V_{DD}</td><td>Directional selection for reading display data
<table>
<tr><th>DIR</th><th>Data read direction</th></tr>
<tr><td>L</td><td>Y_{160} to Y_1</td></tr>
<tr><td>H</td><td>Y_1 to Y_{160}</td></tr>
</table></td></tr>
</table>

Segment mode (continuous)

Symbol	*I/O*	*Connected to*	*Functions*
/DSPOF	I	Controller	Control signal for output deselect level • The input signal is level-shifted from logic voltage level to LCD driver voltage level ，and controls LCD drive circuit • When the signal is low，the output (Y_1 – Y_{160}) of LCD drive be set to level V_{SS}，the contents of line latch are reset，but read the display data in the data latch regardless of condition of /DSPOF • When this signal is high, the operation returns to the normal status.
FR	I	Controller	AC signal for LCD drive • Input a frame inversion signal • The LCD driver output voltage level can be set by line latch output signal and FR signal
MD	I	V_{SS}/V_{DD}	Mode selection *MD* / *Mode selection*: H = 8-bit parallel input; L = 4-bit parallel input
EIO_1，EIO_2	I		Input/output for chip selection • In output state，after 160-bit of data have been read，set to “L” then set to “H” • In input state ，the chip is selected when EI is set to “L”，then 160-bit of data have been read，the chip is deselected *DIR* / *EIO_1* / *EIO_2*: H = Input / Output; L = Output / Input
Y_1-Y_{160}	O	LCD Panel	LCD driver output. One of four levels is output according to the combination of the FR signal and display data

Common Mode

Table-3 Pin Functions Of Common Mode

Symbol	*I/O*	*Connected to*	*Functions*
V_{DD}	I	Power supply	Power supply for internal logic connects to +2.5 to +5.5V
V_{SS}	I	GND	Connect to Ground
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{34R}, V_{34L}	I	Power supply	Power supply for LCD driver level • Normally，the bias voltage used is set by resistor divider • Ensure that the voltage are set such that $V_{ss} < V_{43} < V_{12} < V_0$ • To further reduce the difference between the output waveforms of LCD driver output pin Y_1 and Y_{160} ,externally connect V_{iR} and V_{iL} (i=0,12,34)
EIO_1，EIO_2	I		Data input/output shift for bi-directional shift register • When EIO_1(EIO_2) is input，it will be pull-down • When EIO_1(EIO_2) is output，it will not be pull-down *DIR* / *EIO_1* / *EIO_2*: H = Input / Output; L = Output / Input
LP	I	Controller	Shift clock for bi-directional shift register • Data is shifted on the falling edge of the clock

Common Mode (Continuous)

<table>
<tr><th>Symbol</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>DIR</td><td>I</td><td>Controller</td><td>Directional selection of bi-directional shift register
<table>
<tr><th>DIR</th><th>Data read direction</th></tr>
<tr><td>L</td><td>Y_{160} to Y_1</td></tr>
<tr><td>H</td><td>Y_1 to Y_{160}</td></tr>
</table></td></tr>
<tr><td>/DSPOF</td><td>I</td><td>Controller</td><td>Control signal for output deselect level
• The input signal is level-shifted from logic voltage level to LCD driver voltage level，and controls LCD drive circuit
• When the signal is low，the output (Y_1 – Y_{160}) of LCD drive be set to level V_{SS}，the contents of shift register are reset not read
• When this signal return to high, the operation returns to the normal status.</td></tr>
<tr><td>FR</td><td>I</td><td>Controller</td><td>AC signal for LCD drive
• Input a frame inversion signal
• The LCD driver output voltage level can be set by line latch output signal and FR signal</td></tr>
<tr><td>MD</td><td>I</td><td>V_{ss}/V_{DD}</td><td>Mode selection
<table>
<tr><th>MD</th><th>Mode selection</th></tr>
<tr><td>H</td><td>Dual mode</td></tr>
<tr><td>L</td><td>Single mode</td></tr>
</table></td></tr>
<tr><td>S/C</td><td>I</td><td>V_{ss}/V_{DD}</td><td>Selection of segment mode/common mode
<table>
<tr><th>S/C</th><th>Mode selection</th></tr>
<tr><td>H</td><td>Segment mode</td></tr>
<tr><td>L</td><td>Common mode</td></tr>
</table></td></tr>
<tr><td>DI_7</td><td>I</td><td>Controller</td><td>Dual mode data input
• In dual mode，data can input from 81_{st} bit</td></tr>
<tr><td>DI_0-DI_6</td><td>I</td><td>V_{SS} or V_{DD}</td><td>Not used, avoiding floating.</td></tr>
<tr><td>XCK</td><td>I</td><td>V_{SS} or open</td><td>Not used</td></tr>
<tr><td>Y_1-Y_{160}</td><td>O</td><td>LCD Panel</td><td>LCD driver output.
• One of four voltage levels is output according to FR signal and the data of shift register</td></tr>
</table>

FUNCTIONAL DESCRIPTIONS

Active Control

In case of segment mode, controls the selection or de-selection of the chip. Following a LP signal, and after the chip select signal is input, a select signal is generated internally until 160bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected. In case of common mode, controls the input/output data of bi-directional pins.

SP Conversion & Data Control

In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bits parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

Data Latch Control

In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.

Data Latch

In case of segment mode, latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control, 160 bits of data are read in 20 sets of 8 bits.

Line Latch / Shift Register

In case of segment mode, all 160 bits, which have been read into the data latch block are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.

Level Shifter

The logic voltage signal is boost to the LCD driver voltage level, and output to the driver block.

4-level Driver

Drive the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_{SS}) based on the S/C, FR and /DSPOF

Clock control Logic

Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block.

Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected. In case of common mode, controls the direction of data shift.

Relation between FR, data input and Liquid crystal display driver output voltage level, Explain as following table 4:

Table-4 Liquid Crystal Display Driver Output Voltage Level (Segment Mode)

(a) Segment Mode

FR	*Latch data*	*/DSPOF*	*Driver output voltage level*
H	H	H	V_0
H	L	H	V_2
L	H	H	V_{SS}
L	L	H	V_3
X	**X**	L	V_{SS}

$V_{SS} < V_{43} < V_{12} < V_0$ H: V_{DD} L: V_{SS} **X: Don't care**

(b) Common Mode

FR	*Latch data*	*/DSPOF*	*Driver output voltage level*
H	H	H	V_{SS}
H	L	H	V_1
L	H	H	V_0
L	L	H	V_4
X	X	L	V_{SS}

$V_{SS} < V_{43} < V_{12} < V_0$ H:V_{DD}, L:V_{SS} , **X: Don't care**

Preliminary

Relationship between the display data and driver output pin

Table-5 Relationship Between The Display Data And Driver Output Pin

(a) Segment Mode (4-bit Parallel Mode)

MD	*DIR*	*EIO_1*	*EIO_2*	*Data Input*	*Figure of clock*						
					1_{st}	*2_{nd}*	*3_{rd}*	…	*38_{th}*	*39_{th}*	*40_{th}*
L	L	Output	Input	DI_0	Y_{157}	Y_{153}	Y_{149}	…	Y_9	Y_5	Y_1
				DI_1	Y_{158}	Y_{154}	Y_{150}	…	Y_{10}	Y_6	Y_2
				DI_2	Y_{159}	Y_{155}	Y_{151}	…	Y_{11}	Y_7	Y_3
				DI_3	Y_{160}	Y_{156}	Y_{152}	…	Y_{12}	Y_8	Y_4
L	H	Input	Output	DI_0	Y_4	Y_8	Y_{12}	…	Y_{152}	Y_{156}	Y_{160}
				DI_1	Y_3	Y_7	Y_{11}	…	Y_{151}	Y_{155}	Y_{159}
				DI_2	Y_2	Y_6	Y_{10}	…	Y_{150}	Y_{154}	Y_{158}
				DI_3	Y_1	Y_5	Y_9	…	Y_{149}	Y_{153}	Y_{157}

(b) Segment Mode (8-bit Parallel Mode)

MD	*DIR*	*EIO_1*	*EIO_2*	*Data Input*	*Figure of clock*						
					1_{st}	*2_{nd}*	*3_{rd}*	…	*18_{th}*	*19_{th}*	*20_{th}*
H	L	Output	Input	DI_0	Y_{153}	Y_{145}	Y_{137}	…	Y_{17}	Y_9	Y_1
				DI_1	Y_{154}	Y_{146}	Y_{138}	…	Y_{18}	Y_{10}	Y_2
				DI_2	Y_{155}	Y_{147}	Y_{139}	…	Y_{19}	Y_{11}	Y_3
				DI_3	Y_{156}	Y_{148}	Y_{140}	…	Y_{20}	Y_{12}	Y_4
				DI_4	Y_{157}	Y_{149}	Y_{141}	…	Y_{21}	Y_{13}	Y_5
				DI_5	Y_{158}	Y_{150}	Y_{142}	…	Y_{22}	Y_{14}	Y_6
				DI_6	Y_{159}	Y_{151}	Y_{143}	…	Y_{23}	Y_{15}	Y_7
				DI_7	Y_{160}	Y_{152}	Y_{144}	…	Y_{24}	Y_{16}	Y_8
H	H	Input	Output	DI_0	Y_8	Y_{16}	Y_{24}	…	Y_{144}	Y_{152}	Y_{160}
				DI_1	Y_7	Y_{15}	Y_{23}	…	Y_{143}	Y_{151}	Y_{159}
				DI_2	Y_6	Y_{14}	Y_{22}	…	Y_{142}	Y_{150}	Y_{158}
				DI_3	Y_5	Y_{13}	Y_{21}	…	Y_{141}	Y_{149}	Y_{157}
				DI_4	Y_4	Y_{12}	Y_{20}	…	Y_{140}	Y_{148}	Y_{156}
				DI_5	Y_3	Y_{11}	Y_{19}	…	Y_{139}	Y_{147}	Y_{155}
				DI_6	Y_2	Y_{10}	Y_{18}	…	Y_{138}	Y_{146}	Y_{154}
				DI_7	Y_1	Y_9	Y_{17}	…	Y_{137}	Y_{145}	Y_{153}

(c) Common Mode

MD	*DIR*	*Data transfer direction*	*EIO_1*	*EIO_2*	*DI_7*
L (Single)	H	$Y_1 \rightarrow Y_{160}$	Input	Output	**X**
	L	$Y_{160} \rightarrow Y_1$	Output	Input	**X**
H (Dual)	H	$Y_1 \rightarrow Y_{80}$	Input	Output	Input
		$Y_{81} \rightarrow Y_{160}$			
	L	$Y_{160} \rightarrow Y_{81}$	Output	Input	Input
		$Y_{80} \rightarrow Y_1$			

H:V_{DD}, L:V_{SS} , **X: Don't care**

Preliminary

Connection example of plural segment driver

Case of DIR=”L”

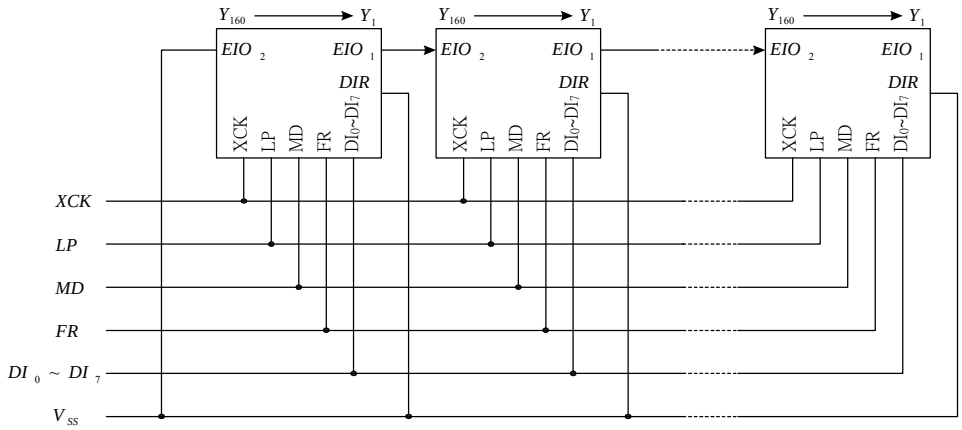


Figure-3. Connection Example Of Plural Segment Driver (DIR=”L”)

Case of DIR=”H”

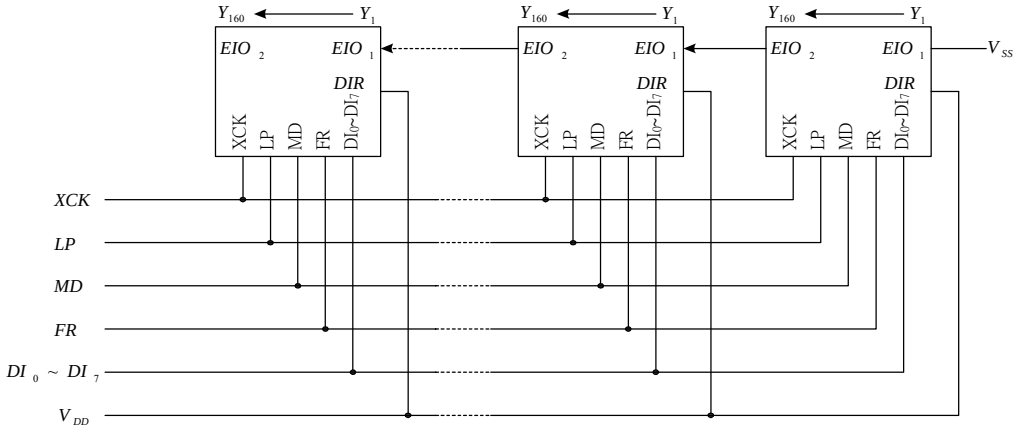


Figure-4. Connection Example Of Plural Segment Driver (DIR=”H”)

Timing chart of 4-Device cascade Connection of Segment Drivers

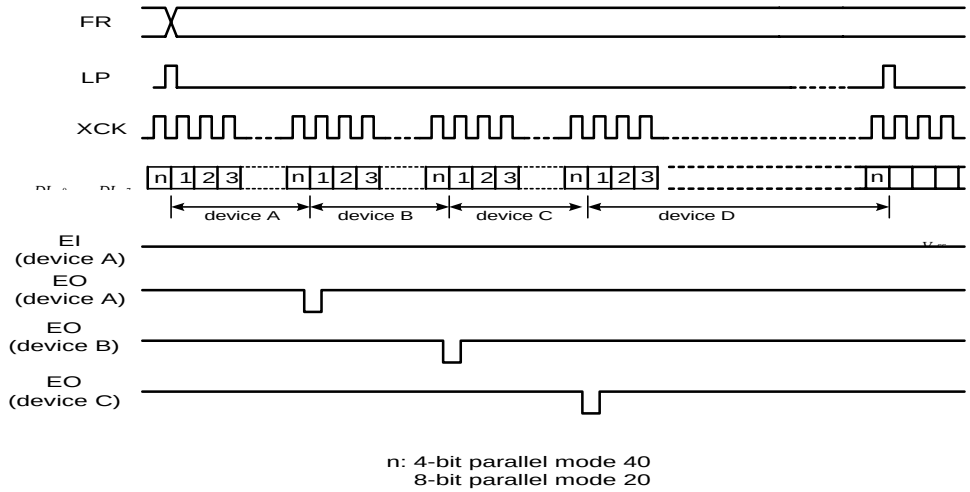


Figure-5. Timing Chart Of 4-Device Cascade Connection Of Segment Drivers

Preliminary

Connection of plural common driver of single mode

Single mode case of DIR="L"

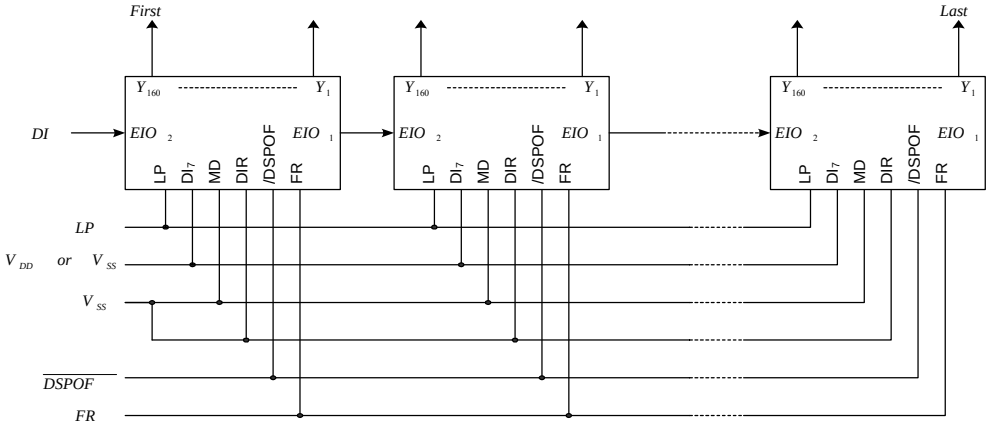


Figure-6. Connection Of Plural Common Driver Of Single Mode (DIR="L")

Single mode case of DIR="H"

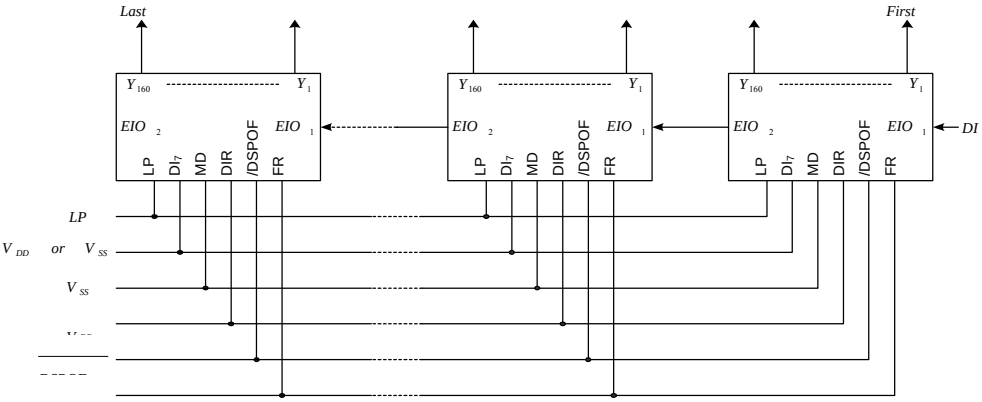


Figure-7. Connection Of Plural Common Driver Of Single Mode (DIR="H")

Connection of plural common driver of dual mode

Dual mode case of DIR="L"

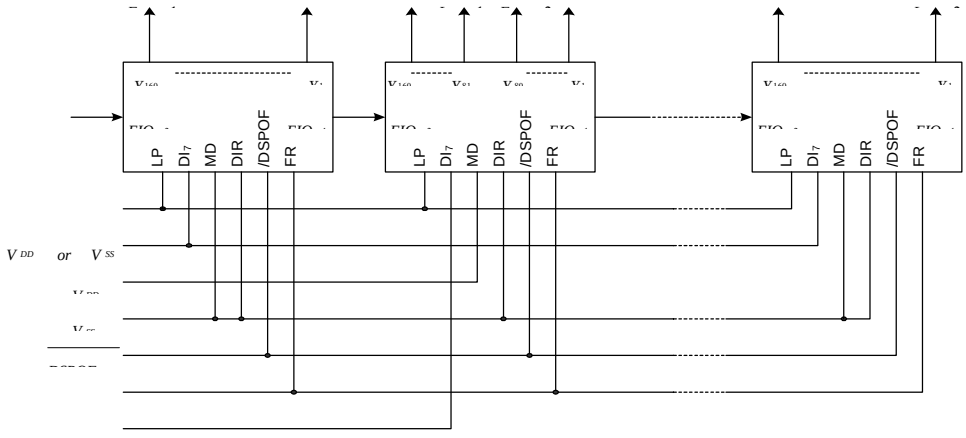


Figure-8. Connection Of Plural Common Driver Of Dual Mode (DIR="L")

Preliminary

Dual mode case of DIR="H"

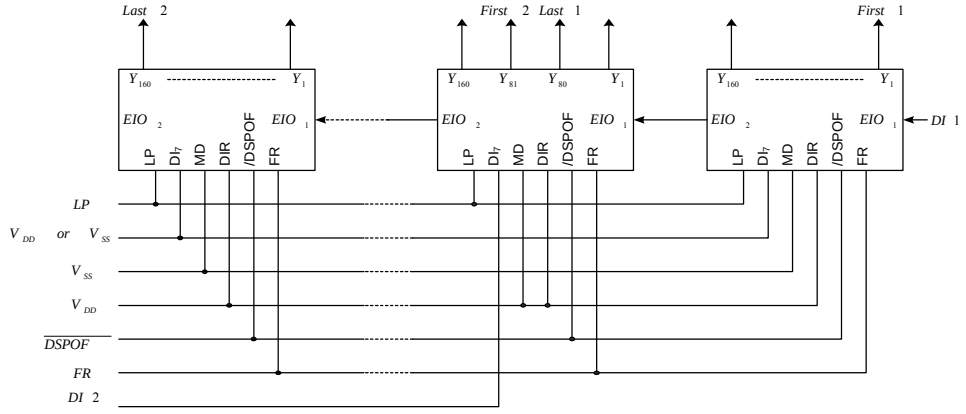


Figure-9. Connection Of Plural Common Driver Of Dual Mode (DIR="H")

Power Supply Circuit for LCD drive

Resistive dividing

Driving bias voltage is generally generated by a resistive divider.(Figure 17)

Precaution when connecting or disconnecting the power.

This LSI has a high voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

We recommend you connecting the serial resistor (50~100Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. And set up the suitable value of the resistor in consideration of LCD display grade.

When connecting or disconnecting the power supply, show the following recommend sequence.

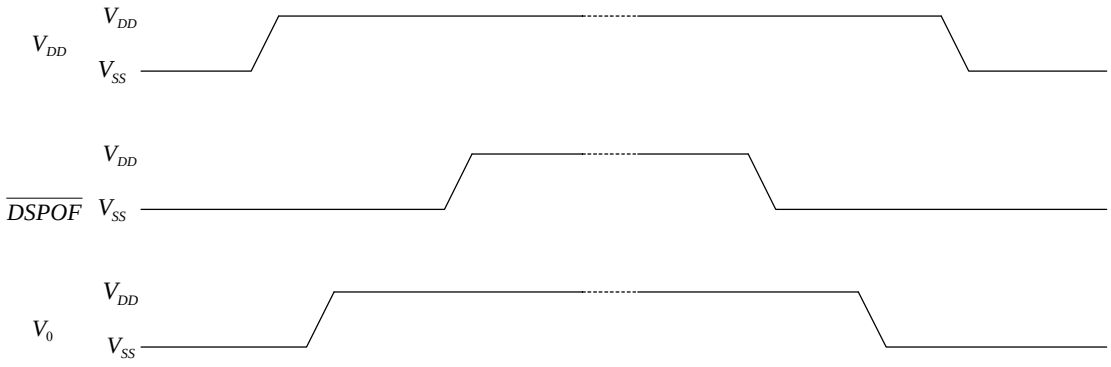


Figure-10. Sequence For Connecting Or Disconnecting The Power Supply

Drive by Operation Amplifier

In graphic display, the size of the LCD becomes larger and the display duty ratio becomes smaller, so the stability of LCD drive voltage level is more important than in small display system.

Since the LCD for graphic display is large and has many picture elements, the load capacitance becomes large. The high impedance of the power supply for LCD drive produces distortion in the drive waveforms, and degrades display quality. For this reason, the LCD drive voltage level impedance should be reduced with operational amplifier. (Figure 17)

Range of Operating Voltage: V0

It is necessary to set the voltage for V0 within the VDD operating voltage range shown in the diagram below.

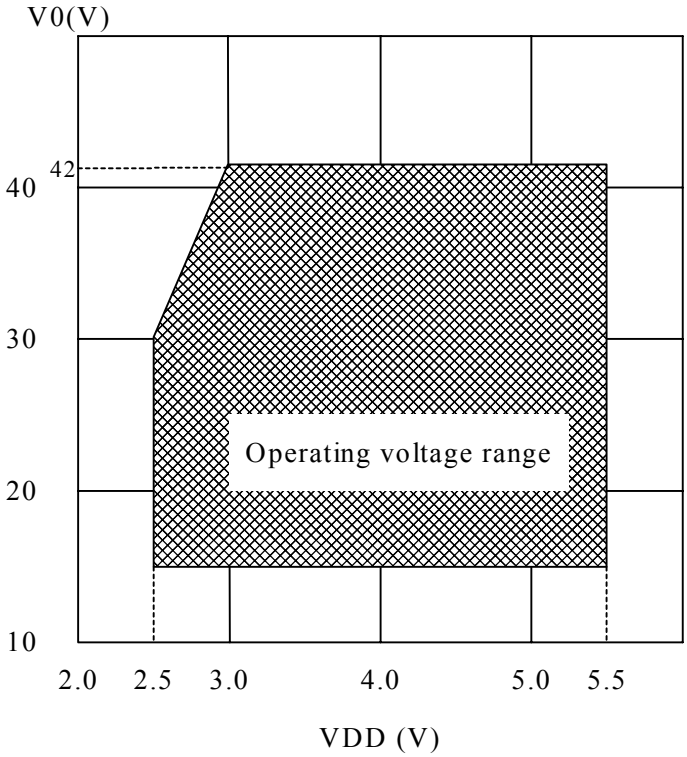


Figure-11 Operating Voltage Range (VDD-VO)

Absolute Maximum ratings

Table-6 Absolute Maximum Ratings

Parameter	*Symbol*	*Conditions*	*Applicable pins*	*Ratings*	*Unit*
Supply voltage (1)	V_{DD}	T_a=25℃ Referenced to V_{SS} (0V)	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_{0-7}, XCK, LP, DIR, FR, MD, S/C, EIO_1, EIO_2, /DSPOF	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

Preliminary

Recommended Operation Conditions

Table-7 Recommended Operation Conditions

Parameter	*Symbol*	*Conditions*	*Applicable pins*	*Min.*	*Type*	*Max.*	*Unit*
Supply voltage (1)	V_{DD}	Referenced to V_{SS} (0V)	V_{DD}	+2.5		+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+15		+42	V
Operating temperature	T_{opr}			-20		+85	℃

Note: Ensure that voltages are set such that $V_{ss} < V_{43} < V_{12} < V_0$

DC Characteristics

Segment Mode

Table-8 DC Characteristics Of Segment Mode

(V_{SS} == 0V, V_{DD} = +2.5 to +5.5V, V_0 = +15 to +42V, T_a = -20~+85°C)

Parameter	*Symbol*	*Conditions*	*Applicable pins*	*Min.*	*Typ.*	*Max.*	*Unit*
Input voltage	V_{IH}		DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C, EIO_1, EIO_2, /DSPOF	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output Voltage	V_{OH}	I_{OH}=-0.4mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C, EIO_1, EIO_2, /DSPOF			+10	μA
	I_{LIL}	V_I=V_{SS}				-10	μA
Output resistance	R_{ON}	$\|\Delta V_{ON}\|$ =0.5V, V_0=+40V	Y_1- Y_{160}		0.7	1.0	kΩ
		$\|\Delta V_{ON}\|$ =0.5V, V_0=+30V			1.0	1.5	
		$\|\Delta V_{ON}\|$ =0.5V, V_0=+20V			1.5	2.0	
Stand-by current	I_{STB}	*1	V_{SS}			50.0	μA
Consumed current (Deselection)	I_{DD1}	*2	V_{DD}			2.0	mA
Consumed current (Selection)	I_{DD2}	*3	V_{DD}			8.0	mA
Consumed current	I_0	*4	V_0			1.0	mA

Note:

1. V_{DD}=+5.0V, V_0=+42.0V, V_I=V_{SS}
2. V_{DD}=+5.0V, V_0=+42.0V, V_I=V_{SS}, f_{XCK}=14MHz, No-load, EI=V_{DD}
3. V_{DD}=+5.0V, V_0=+42.0V, V_I=V_{SS}, f_{XCK}=14MHz, No-load, EI=V_{SS}
4. V_{DD}=+5.0V, V_0=+42.0V, V_I=V_{SS}, f_{XCK}=14MHz, f_{FR}=80Hz, No-load, EI=V_{SS}

(The input data is turned over by data taking clock (4-bit parallel input mode)

Common mode

Table-9 DC Characteristics Of Common Mode

(V_{SS} = 0V, V_{DD} = +2.5 to 5.5V, V_0 = +15 to +42V, Ta = -20~85°C)

Parameter	*Symbol*	*Conditions*	*Applicable pins*	*Min.*	*Typ.*	*Max.*	*Unit*
Input voltage	V_{IH}		DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C, EIO_1, EIO_2, /DSPOF	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}= -0.4mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}= +0.4mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C, EIO_1, EIO_2, /DSPOF			+10	μA
	I_{LIL}	V_I=V_{SS}				-10	μA
Output resistance	R_{ON}	|ΔV_{ON}| =0.5V, V_0=+40V	Y_1- Y_{160}		0.7	1.0	kΩ
		|ΔV_{ON}| =0.5V, V_0=+30V			1.0	1.5	
		|ΔV_{ON}| =0.5V, V_0=+20V			1.5	2.0	
Input pull-down current	I_{PD}	V_I=V_{DD}	XCK, EIO_1, EIO_2			100.0	μA
Stand-by current	I_{STB}	*1	V_{SS}			50.0	μA
Consumed current (1)	I_{DD}	*2	V_{DD}			80.0	μA
Consumed current (2)	I_0	*2	V_0			160.0	μA

NOTE:

1. V_{DD} = +5V, V_0 = +42V, V_I = V_{SS}

2. V_{DD} = +5V, V_0 = +42V, f_{LP} = 41.6kHz, f_{FR} = 80Hz, case of 1/480 duty operation, No-load

AC Electrical characteristic

Segment mode 1

Table-10 AC Electrical Characteristics Of Segment Mode 1

(V_{SS} = 0V, V_{DD} = +4.5 to +5.5V, V_0 = +15 to +42V, T_a = -20~85°C)

Parameter	*Symbol*	*Condition*	*Min.*	*Type*	*Max.*	*Unit*
Shift clock period *1	T_{WCK}	T_R,T_F≦10ns	71			ns
Shift clock "H" pulse width	T_{WCKH}		23			ns
Shift clock "L" pulse width	T_{WCKL}		23			ns
Data setup time	T_{DS}		10			ns
Data hold time	T_{DH}		20			ns
Latch pulse "H" pulse width	T_{WLPH}		23			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		25			ns
Latch pulse rise to shift clock rise time	T_{LS}		25			ns
Latch pulse fall to shift clock fall time	T_{LH}		25			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		21			ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			μs
Output delay time (1)	T_D	C_L=15pF			40	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L=15pF			1.2	μs
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	μs

NOTES:

1. Take the cascade connection into consideration.

2. (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high-speed operation.

Segment mode 2

Table-11 AC Electrical Characteristics Of Segment Mode 2

(V_{SS} = 0V, V_{DD} = +2.5 to +4.5V, V_0 = +15 to +42V, T_a = -20~85°C)

Parameter	*Symbol*	*Condition*	*Min.*	*Type*	*Max.*	*Unit*
Shift clock period *1	T_{WCK}	T_R,T_F≦10ns	125			ns
Shift clock "H" pulse width	T_{WCKH}		51			ns
Shift clock "L" pulse width	T_{WCKL}		51			ns
Data setup time	T_{DS}		30			ns
Data hold time	T_{DH}		40			ns
Latch pulse "H" pulse width	T_{WLPH}		51			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		51			ns
Latch pulse rise to shift clock rise time	T_{LS}		51			ns
Latch pulse fall to shift clock fall time	T_{LH}		51			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		36			ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			μs
Output delay time (1)	T_D	C_L=15pF			78	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L=15pF			1.2	μs
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	μs

NOTES:

1. Take the cascade connection into consideration.

2. (T_{WCK} − T_{WCKH} − T_{WCKL}) / 2 is maximum in the case of high-speed operation.

Common mode

Table-12 AC Electrical Characteristics Of Common Mode

(V_{SS} = 0V, V_{DD} = +2.5 to +5.5V, V_0 = +15 to +42V, T_a = -20~85°C)

Parameter	*Symbol*	*Condition*	*Min.*	*Type*	*Max.*	*Unit*
Shift clock period	T_{WLP}	T_R,T_F≦20ns	250			ns
Shift clock "H" pulse width	T_{WLPH}	V_{DD}=+5.0V±10%	15			ns
		V_{DD}=+2.5V~+4.5V	30			ns
Data setup time	T_{SU}		30			ns
Data hold time	T_H		30			ns
Input signal rise time	T_R				50	ns
Input signal fall time	T_F				50	ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			μs
Output delay time (1)	T_{DL}	C_L=15pF			200	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L=15pF			1.2	μs
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	μs

Timing diagram

Timing characteristics of segment mode

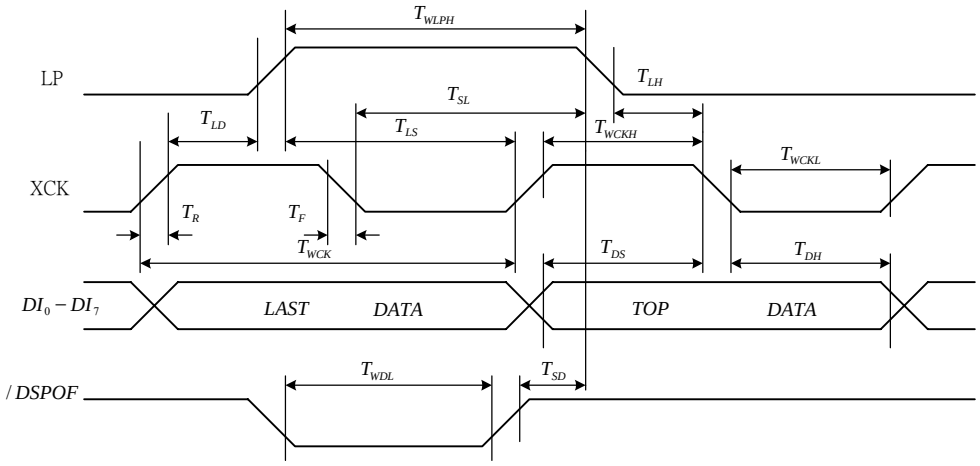


Figure-12 Timing Characteristics Of Segment Mode (1)

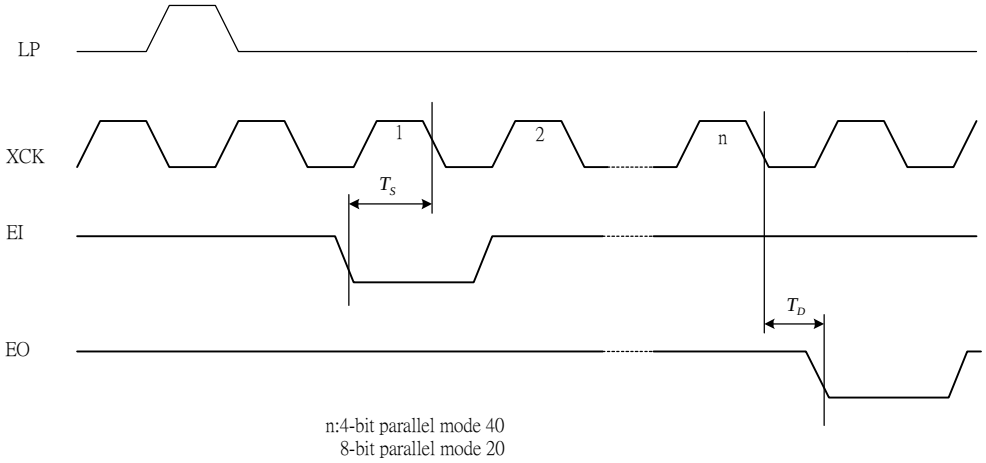


Figure-13. Timing Characteristics Of Segment Mode (2)

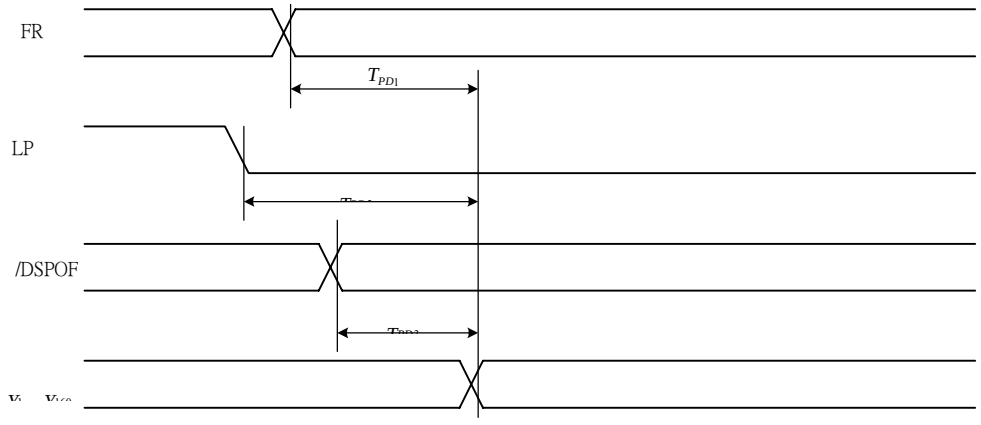


Figure-14. Timing Characteristics Of Segment Mode (3)

Preliminary

Timing characteristics of common mode

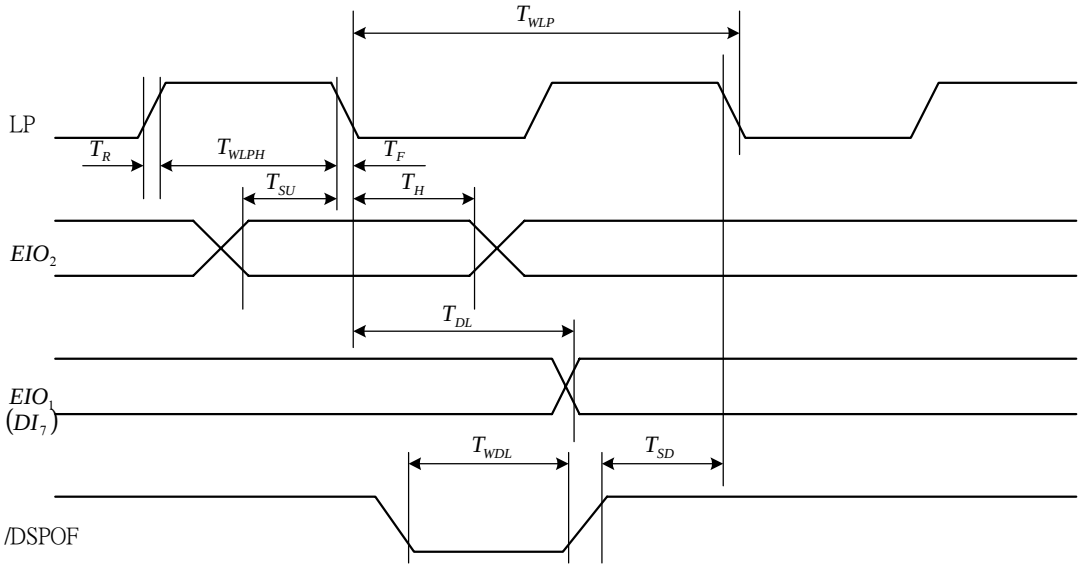
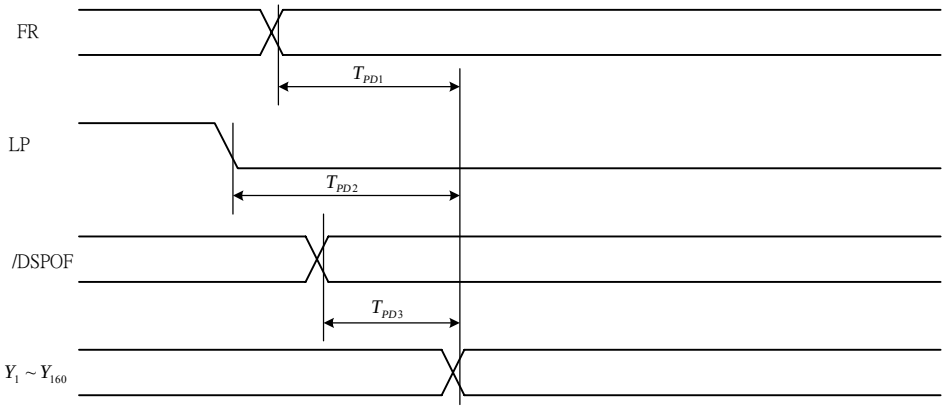


Figure-15 Timing Characteristics Of Common Mode (1)



DIR="L"

Figure-16. Timing Characteristics Of Common Mode (2)

Preliminary

Application circuit

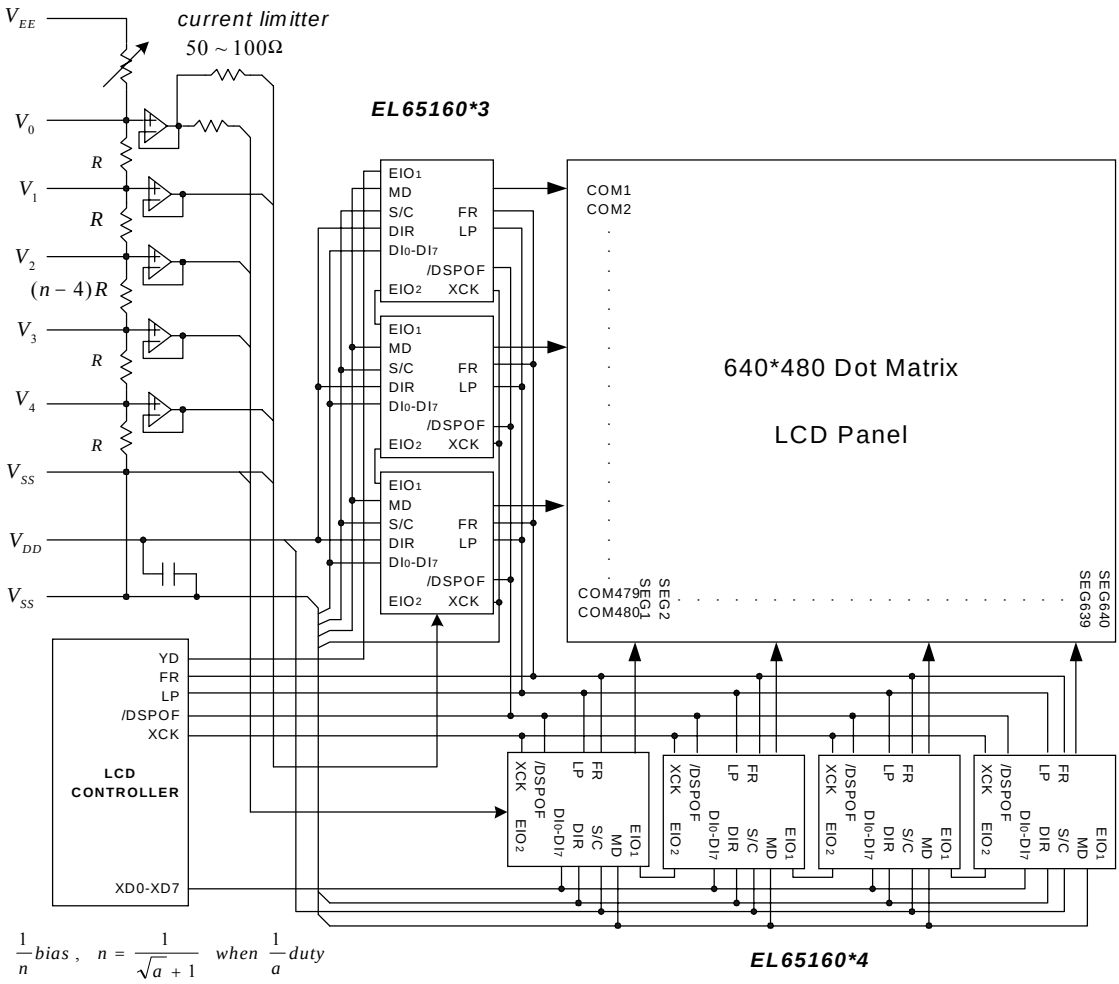
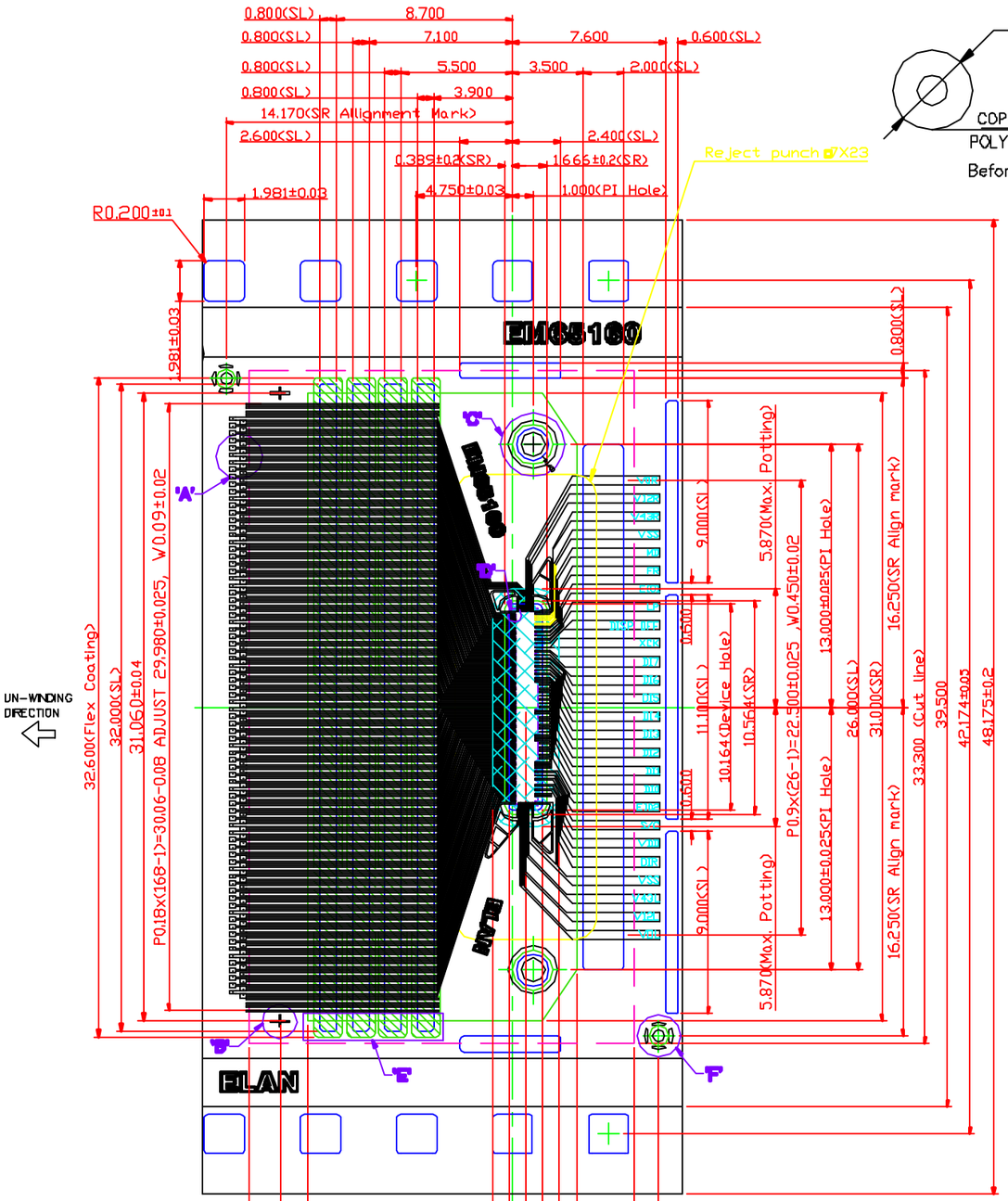
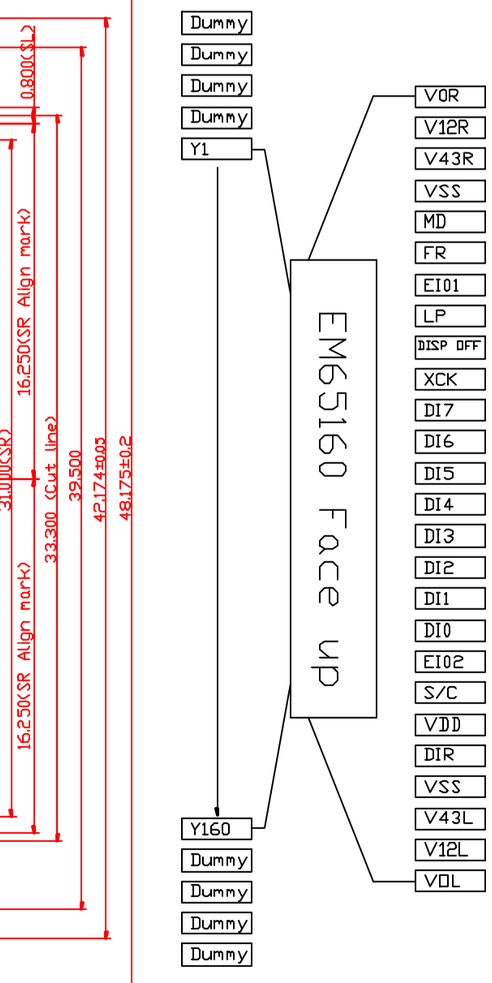
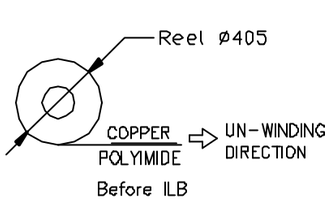
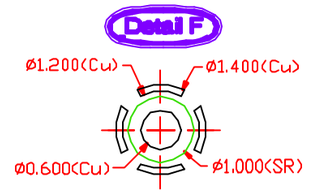


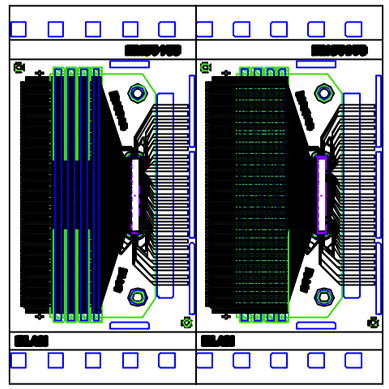
*Figure-17. Application Circuit Of 640*480 LCD Panel*

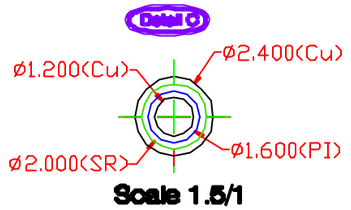


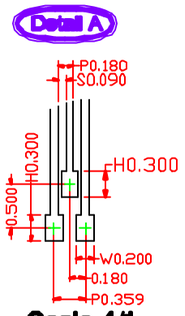


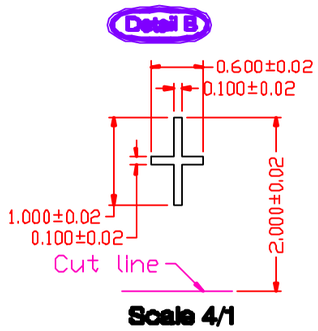


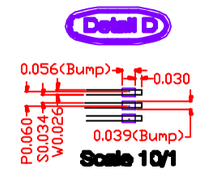


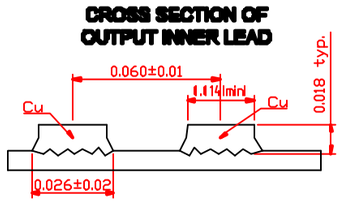


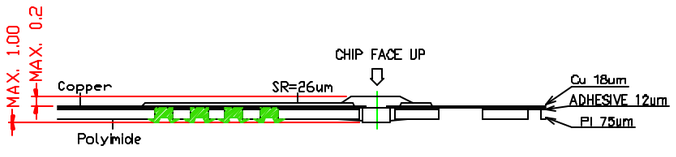


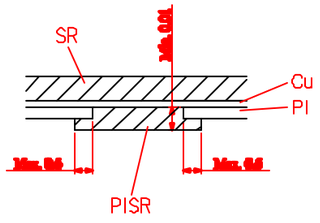


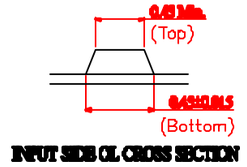


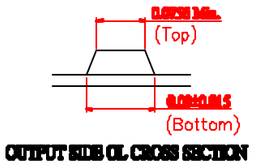












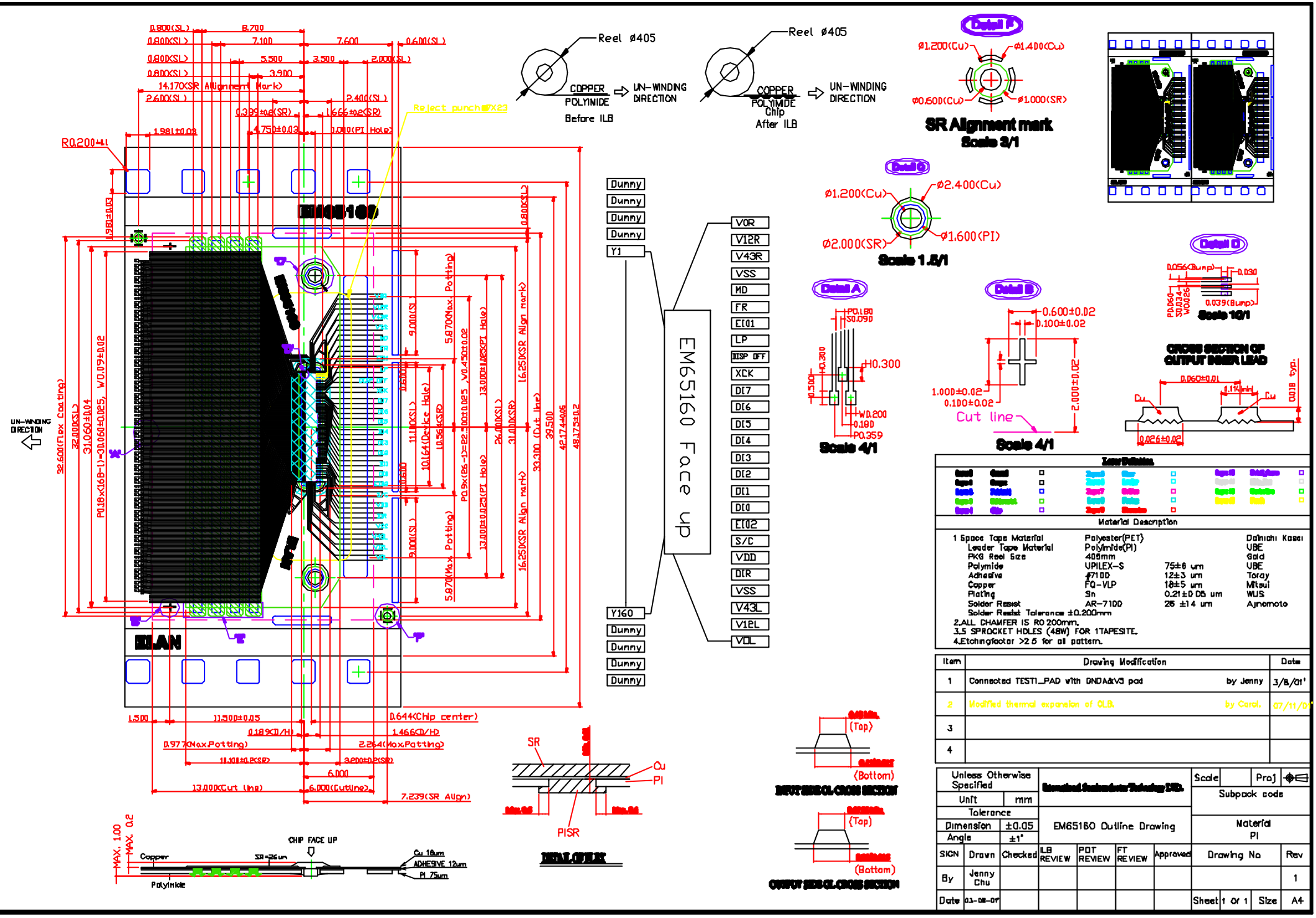
Material Description

1.Space Tape Material	Polyester(PET)		Dainichi Kasei
Leader Tape Material	Polyimide(PI)		UBE
PKG Reel Size	405mm		Gold
Polyimide	UPILEX-S	75±6 um	UBE
Adhesive	#7100	12±3 um	Toray
Copper	FQ-VLP	18±5 um	Mitsui
Plating	Sn	0.21±0.05 um	WUS
Solder Resist	AR-710D	26 ±14 um	Ajinomoto
Solder Resist Tolerance. ±0.200mm			

2.ALL CHAMFER IS R0.200mm.
3.5 SPROCKET HOLES (48W) FOR 1TAPESITE
4.Etchingfactor >2.5 for all pattern.

Item	Drawing Modification	Date
1	Connected TEST1_PAD with GNDA&V5 pad by Jenny.	3/8/01'
2		
3		
4		

Unless Otherwise Specified			International Semiconductor Technology LTD.				Scale		Proj
Unit	mm						Subpack code		
Tolerance									
Dimension	±0.05		EM65160 Outline Drawing				Material PI		
Angle	±1°								
SIGN	Drawn	Checked	ILB REVIEW	POT REVIEW	FT REVIEW	Approved	Drawing No		Rev
By	Jenny Chu								1
Date	03-08-01'						Sheet	1 Of 1	Size A4



Material Description

1 Space Tape Material	Polyester(PET)			Dainichi Kasei
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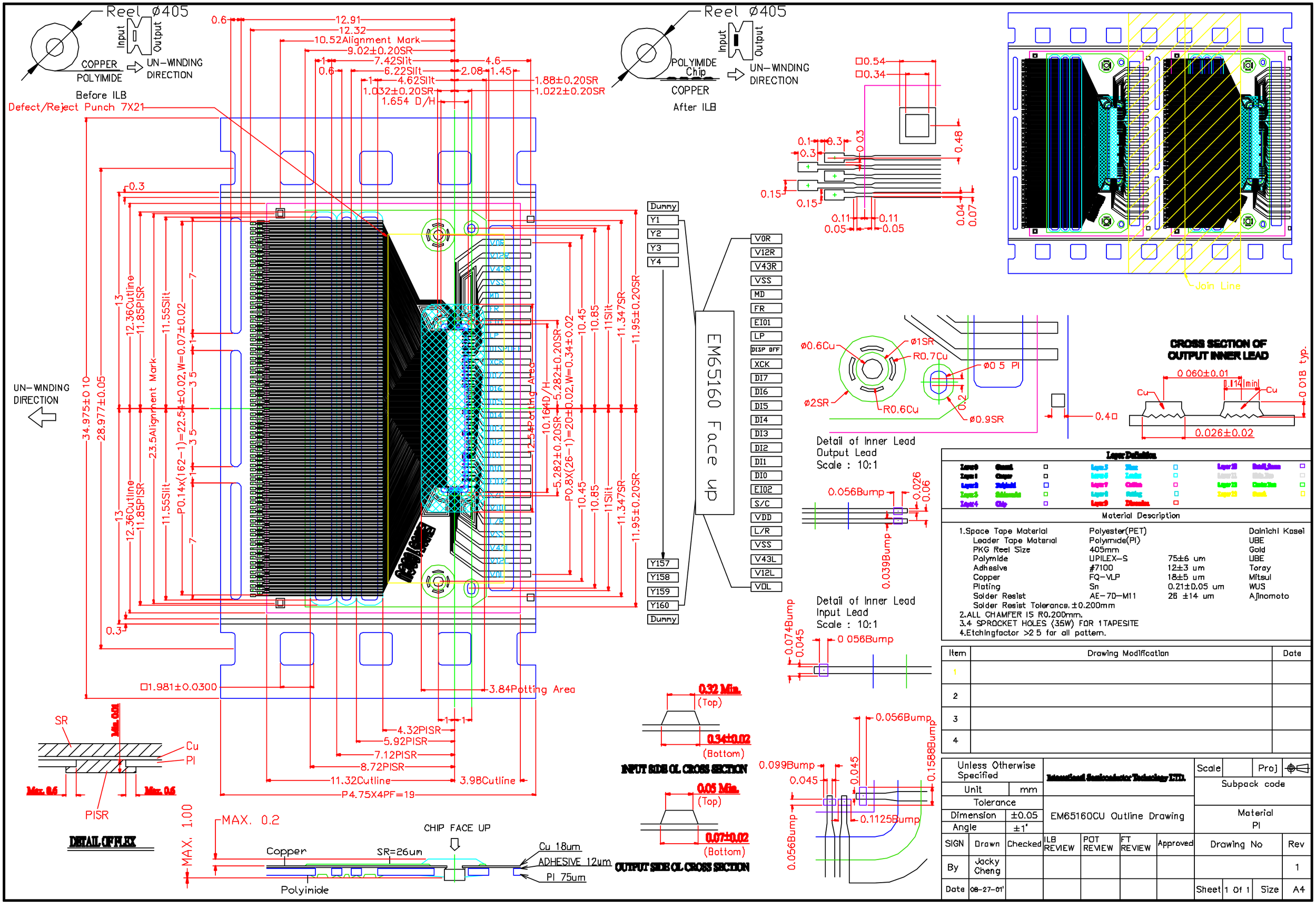
PKG Reel Size	405mm			Gold
Polymide	UPILEX-S	75±6 um		UBE
Adhesive	#7100	12±3 um		Toray
Copper	FQ-VLP	18±5 um		Mitsui
Plating	Sn	0.21±0.05 um		WUS
Solder Resist	AR-7100	25 ±14 um		Ajinomoto
Solder Resist Tolerance ±0.200mm				

2.ALL CHAMFER IS R0.200mm.
3.5 SPROCKET HOLES (48W) FOR 1TAPESITE.
4.Etchingfactor >2.5 for all pattern.

Item	Drawing Modification		Date
1	Connected TEST1_PAD with GNDA&VSS pad	by Jenny	3/8/01'
2	Modified thermal expansion of OLB.	by Carol.	07/11/01'
3			
4			

Unless Otherwise Specified							Scale		Proj
Unit	mm						Subpack code		
Tolerance									
Dimension	±0.05		EM65160 Outline Drawing				Material		
Angle	±1°						PI		
SIGN	Drawn	Checked	ILB REVIEW	POT REVIEW	FT REVIEW	Approved	Drawing No		Rev
By	Jenny Chu								1
Date	03-08-01'						Sheet	1 Of 1	Size A4



Layer Definition

Layer0	Gound	□	Layer5	Blue	□	Layer10	Gold_Bump	□
Layer1	Copper	□	Layer6	Yellow	□	Layer11	White_Bump	□
Layer2	Polyimid	□	Layer7	Outline	□	Layer12	Outline_Bump	□
Layer3	Silkscreen	□	Layer8	Marking	□	Layer13	Mark	□
Layer4	Chip	□	Layer9	Dimension	□			

Material Description

1.Space Tape Material	Polyester(PET)		Dainichi Kasei
Leader Tape Material	Polymide(PI)		UBE
PKG Reel Size	405mm		Gold
Polymide	UPILEX-S	75±6 um	UBE
Adhesive	#7100	12±3 um	Toray
Copper	FQ-VLP	18±5 um	Mitsui
Plating	Sn	0.21±0.05 um	WUS
Solder Resist	AE-70-M11	26 ±14 um	Ajinomoto
Solder Resist Tolerance. ±0.200mm			

2.ALL CHAMFER IS R0.200mm.
3.4 SPROCKET HOLES (35W) FOR 1TAPESITE
4.Etchingfactor >2.5 for all pattern.

Item	Drawing Modification	Date
1		
2		
3		
4		

Unless Otherwise Specified			International Semiconductor Technology LTD.				Scale		Proj
Unit	mm						Subpack code		
Tolerance			EM65160CU Outline Drawing				Material PI		
Dimension	±0.05								
Angle	±1°								
SIGN	Drawn	Checked	ILB REVIEW	POT REVIEW	FT REVIEW	Approved	Drawing No		Rev
By	Jacky Cheng								1
Date	08-27-01'						Sheet	1 Of 1	Size A4