GENERAL DESCRIPTION

The EM65565A is a 65 Common 132 Segment dot matrix *liquid crystal display* (***LCD***) driver LSI, it can be connected directly to a microprocessor bus, be selected 8-bit parallel or serial data input interface. The chip of EM65565A contains 65x132 bits of *display data RAM* (***DDRAM***) and there is a one-to-one correspondence between the *LCD* panel pixels and the internal RAM bits.

The EM65565A chip can drive a 65×132 dot display. Moreover, the capacity of the display can be extended by master/slave structures between chips. The chips are able to minimize power consumption because no external operating clock is necessary for the *DDRAM* read/write operation. Furthermore, because each chip is equipped internally with a low-power *LCD* driver power supply, resistors for *LCD* driver power voltage adjustment and a display clock CR oscillator circuit, the EM65565A chip can be used to create the lowest power display system with the fewest components for high-performance portable devices.

FEATURES

- Direct display of RAM data through the *DDRAM*.RAM bit data: “0” Illuminated, “1” Non-illuminated
- RAM capacity 65 × 132 = 8580 bits
- Display driver circuits: 65 common output and 132 segment outputs
- High-speed 8-bit MPU interface (80-series and 68-series) / Serial interfaces are supported.
- Abundant command functions: display data Read/Write, display ON/OFF, status read, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, *LCD* bias set, electronic volume, read-modify-write, segment driver direction select, power saver, static indicator, common output status select, V_0 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators
- Low-power *LCD* power supply circuit equipped internally. Booster circuit (with Boost ratios of Two/Three/Four/Five times, where the step-up voltage reference power supply can be input externally) High-accuracy voltage adjustment circuit (external input) V_0 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- Internal CR oscillator circuit (external clock can also be input)
- Extremely low power consumption,
- Power supply, Operable on the low 1.8 voltage, Logic power supply $V_{DD} – V_{SS}$ = 2.4 to 3.3 V, Boost reference voltage: V_{CI}= 2.4 to 3.3 V, *LCD* drive power supply: $V_{LCD}=V_0 – V_{SS}$ =4.5 to 12.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- Package: COG and TCP.
- These chips not designed for resistance to light or resistance to radiation.

Series specifications

Name	Duty	Bias	Common output	Segment output	V_{REG} temperature gradient	Package Forms
EM65565AAC	1/65	1/7,1/9	65	132	-0.05%/°C	COG
EM65565AAT						TCP
EM65565ABC					-0.2%/°C	COG
EM65565ABT						TCP
EM65565ACC					External input	COG
EM65565ACT						TCP

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PIN DESCRIPTION

Table 1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>V_{DD}</td><td>Power Supply</td><td>Shared with the MPU power supply terminal V_{CC}</td><td>14</td></tr>
<tr><td>V_{SS}</td><td>Power Supply</td><td>This is a 0 V terminal connected to the system GND.</td><td>20</td></tr>
<tr><td>V_{CI}</td><td>I</td><td>This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.</td><td>3</td></tr>
<tr><td>V_{RS}</td><td>I</td><td>This is the externally input V_{REG} power supply for the LCD power supply voltage regulator. These are only enabled for the models with the V_{REG} external input option.</td><td>3</td></tr>
<tr><td>V_0
V_1
V_2
V_3
V_4</td><td>I/O</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an Op. Amp. Voltage levels are determined based on V_0, and must maintain the relative magnitudes shown below.
$V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$
Master operation: When the power supply turns ON, the internal power supply circuits produce the V_1 to V_4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><td></td><td>1/9 bias</td><td>1/7 bias</td></tr>
<tr><td>V_1</td><td>$8/9 \bullet V_0$</td><td>$6/7 \bullet V_0$</td></tr>
<tr><td>V_2</td><td>$7/9 \bullet V_0$</td><td>$5/7 \bullet V_0$</td></tr>
<tr><td>V_3</td><td>$2/9 \bullet V_0$</td><td>$2/7 \bullet V_0$</td></tr>
<tr><td>V_4</td><td>$1/9 \bullet V_0$</td><td>$1/7 \bullet V_0$</td></tr>
</table></td><td>15</td></tr>
<tr><td>CAP1+</td><td>O</td><td>Capacitor 1 positive connection pin for voltage converter</td><td>3</td></tr>
<tr><td>CAP1-</td><td>O</td><td>Capacitor 1 negative connection pin for voltage converter</td><td>3</td></tr>
<tr><td>CAP2+</td><td>O</td><td>Capacitor 2 positive connection pin for voltage converter</td><td>3</td></tr>
<tr><td>CAP2-</td><td>O</td><td>Capacitor 2 negative connection pin for voltage converter</td><td>3</td></tr>
<tr><td>CAP3+</td><td>O</td><td>Capacitor 3 positive connection pin for voltage converter</td><td>3</td></tr>
<tr><td>CAP4+</td><td>O</td><td>Capacitor 4 positive connection pin for voltage converter</td><td>3</td></tr>
<tr><td>V_{OUT}</td><td>I/O</td><td>DC/DC voltage converter input/output pin, connect a capacitor between this terminal and V_{SS}</td><td>2</td></tr>
<tr><td>V_R</td><td>I</td><td>Output voltage regulator terminal.
These are only enabled when the V_0 voltage regulator internal resistors are not used (IRS = “L”).
These cannot be used when the V_0 voltage regulator internal resistors are used (IRS = “H”).</td><td>3</td></tr>
</table>

(Continuous)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>D7 to D0</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the chip select is inactive, D0 to D7 are set to high impedance.
When the serial interface is selected (P/S = “L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.</td><td>8</td></tr>
<tr><td>D/I</td><td>I</td><td>Determines whether the data bits are data or the instruction (command).
<table>
<tr><td>D/I</td><td>D0 to D7</td></tr>
<tr><td>H</td><td>Display data</td></tr>
<tr><td>L</td><td>Instruction (Command)</td></tr>
</table></td><td>1</td></tr>
<tr><td>/RST</td><td>I</td><td>When /RST is set to “L,” the settings are initialized.</td><td>1</td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>This is the chip select signal. When /CS1 = “L” and CS2 = “H,” then the chip select CS2 becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>Enable clock signal input for the 68-series MPU, active high.
Active low input pin for the 80-series MPU /RD signal</td><td>1</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>Read/Write control signal with 68-series MPU
R/W=”H”: Read, R/W=”L”: Write
Active low input pin for the 80-series MPU /WR signal</td><td>1</td></tr>
<tr><td>MPUS</td><td>I</td><td>This is the MPU interface switch terminal.
MPUS =”H”: 68-series MPU interface.
MPUS =”L”: 80-series MPU interface.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Selects the Parallel or Serial data input interface
P/S = “H”: Parallel data input interface
P/S = “L”: Serial data input interface
The following applies depending on the P/S status:
<table>
<tr><td>P/S</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial Clock</td></tr>
<tr><td>H</td><td>D/I</td><td>D0 to D7</td><td>/RD, /WR</td><td></td></tr>
<tr><td>L</td><td>D/I</td><td>D7 (SI)</td><td>Write only</td><td>D6 (SCL)</td></tr>
</table>
When P/S = “L”, D0 to D5 are HZ. D0 to D5 may be “H”, “L” or Open.
RD (E) and WR (P/W) are fixed to either “H” or “L”.
With serial data input, RAM display data reading is not supported.</td><td>1</td></tr>
<tr><td>DCLKS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
DCLKS = “H”: Internal oscillator circuit is enabled
DCLKS = “L”: Internal oscillator circuit is disabled (requires external input)
When DCLKS = “L”, input the display clock through the DCLK terminal.</td><td>1</td></tr>
</table>

(Continuous)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>M/S = “H”: Master operation
M/S = “L”: Slave operation
The following is true depending on the M/S and DCLKS status:
<table>
<tr><th>M/S</th><th>DCLKS</th><th>Oscillator circuit</th><th>Power Supply Circuit</th><th>DCLK</th><th>FR</th><th>FRS</th><th>/BCT</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>I</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Disable</td><td>Disable</td><td>I</td><td>I</td><td>O</td><td>I</td></tr>
<tr><td>L</td><td>Disable</td><td>Disable</td><td>I</td><td>I</td><td>O</td><td>I</td></tr>
</table>
O: Output, I: Input</td><td>1</td></tr>
<tr><td>DCLK</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and DCLKS status.
<table>
<tr><th>M/S</th><th>DCLKS</th><th>DCLK</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td></tr>
<tr><td>L</td><td>Input</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td></tr>
<tr><td>L</td><td>Input</td></tr>
</table>
When the EM65565A chips are used in master/slave mode, the various DCLK terminals must be connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal.
M/S = “H”: Output
M/S = “L”: Input
When the EM65565A Series chip is used in master/slave mode, the various FR terminals must be connected.</td><td>2</td></tr>
<tr><td>/BCT</td><td>I/O</td><td>This is the LCD blanking control terminal.
M/S = “H”: Output
M/S = “L”: Input
When the EM65565A chip is used in master/slave mode, the various /BCT terminals must be connected.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V_0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V_0 voltage level is regulated by an external resistive voltage divider attached to the V_R terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
<tr><td>/PCT</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/PCT = “H”: Normal mode
/PCT = “L”: High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
</table>

(Continuous)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>SEG0
To
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_0, V_2, V_3, and V_{SS}.
<table>
<tr><td>RAM DATA</td><td>FR</td><td colspan="2">Output Voltage</td></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power Save</td><td>--</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM 0
To
COM 63</td><td>O</td><td>These are the LCD common drive outputs. COM0 to COM63
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_0, V_1, V_4, and V_{SS}.
<table>
<tr><td>Scan Data</td><td>FR</td><td>Output Voltage</td></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V_0</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>--</td><td>V_{SS}</td></tr>
</table></td><td>64</td></tr>
<tr><td>COMS</td><td>O</td><td>These are the common output terminals for the indicator. Both terminals output the same signal. Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
<tr><td>TEST0~4
TEST7~9</td><td>I/O</td><td>These are terminals for IC chip testing.
They are set to OPEN.</td><td>8</td></tr>
</table>

BLOCK DIAGRAM

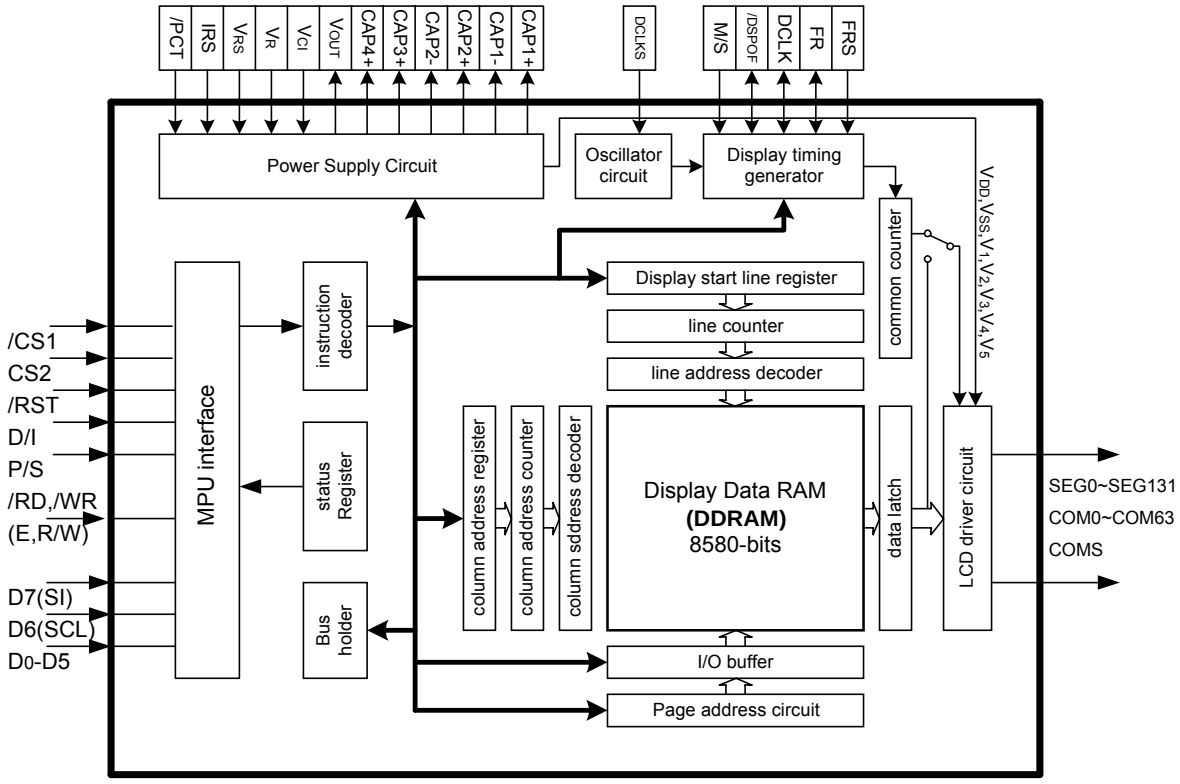


Fig. 1 Block diagram of System

FUNCTIONAL DESCRIPTIONS

The MPU Interface

Selecting the interface Type

The EM65565A chip can be selected either parallel interface or serial interface by the P/S terminal polarity to the “H” or “L”, as shown in Table 2

Table 2

P/S	/CS1	CS2	D/I	/RD	/WR	MPUS	D7	D6	D5~D0
H: Parallel Input	↑	↑	↑	↑	↑	↑	↑	↑	↑
L: Serial Input	↑	↑	↑	--	--	--	SI	SCL	(HZ)

“--“Indicates fixed to either “H” or to “L”

The Parallel Interface:

When the parallel interface has been selected (P/S=”H”), then it is possible to connect directly to either an 80-series MPU or a 68-series MPU by selecting the MPUS terminal to either “H” or to “L”.

Table 3

MPUS	/CS1	CS2	D/I	/RD	/WR	D7~D0
L: 80-series MPU	↑	↑	↑	↑	↑	↑
H: 68-series MPU	↑	↑	↑	E	R/W	↑

Identification of data bus signals by a combination of D/I, /RD (E), /WR (R/W) signals as shown in Table 4.

Table 4

	68-Series	80-Series		Function
D/I	R/W	/RD	/WR	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Read status
0	0	1	0	Write control data (command)

The Serial Interface:

When the chip is active state (/CS1=”L” and CS2=”H”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the SI pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the 8th serial clock for the processing.

The D/I input is used to determine whether or the serial data input is display data (D/I=”H”) or command data (D/I=”L”). The D/I input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 2 is a serial interface signal chart.

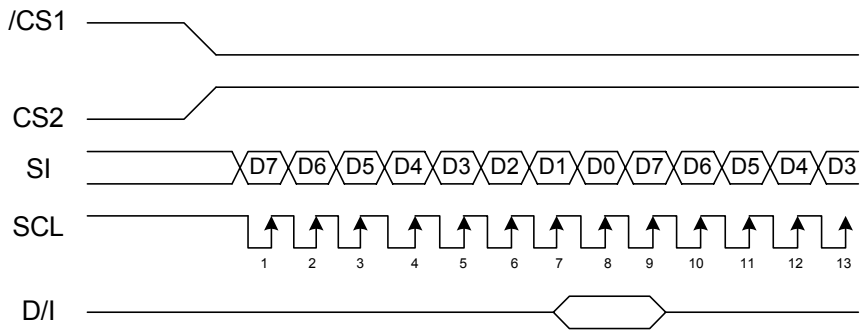


Fig. 2

Notes:

1. When the chip is not active, the shift registers and counter are reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The EM65565A chip have two chip select terminals: /CS1 and CS2. The MPU interface or the serial interface is enabled only when /CS1=”L” and CS2=”H”.

When the chip select is inactive. D0 to D7 enter a high impedance state, and the D/I, /RD, and /WR inputs are inactive. When the serial interface is selected. The shift register and the counter are reset.

Accessing the *DDRAM* and the Internal Registers

In order to make matching of operation frequencies between the MPU and *DDRAM* or internal register, the EM65565A performs a sort of LSI-LSI pipelining via the bus holder attached to the internal data bus.

When the MPU writes data to the *DDRAM*, once the data is stored in the bus holder, then it is written to the *DDRAM* before the next data write cycle. Moreover, when the MPU reads the *DDRAM*, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the *DDRAM*. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or the write cycle operation is conducted. This relationship is shown in Figure 3.

The Busy Flag

The busy flag is output to pin D7 by a read status command. When the busy flag is “1” it indicates that the EM65565A chip is executing its internal operations, any command other than status read is rejected during this time. If the cycle time (t_{CYC}) is maintained, this flag needs not be check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

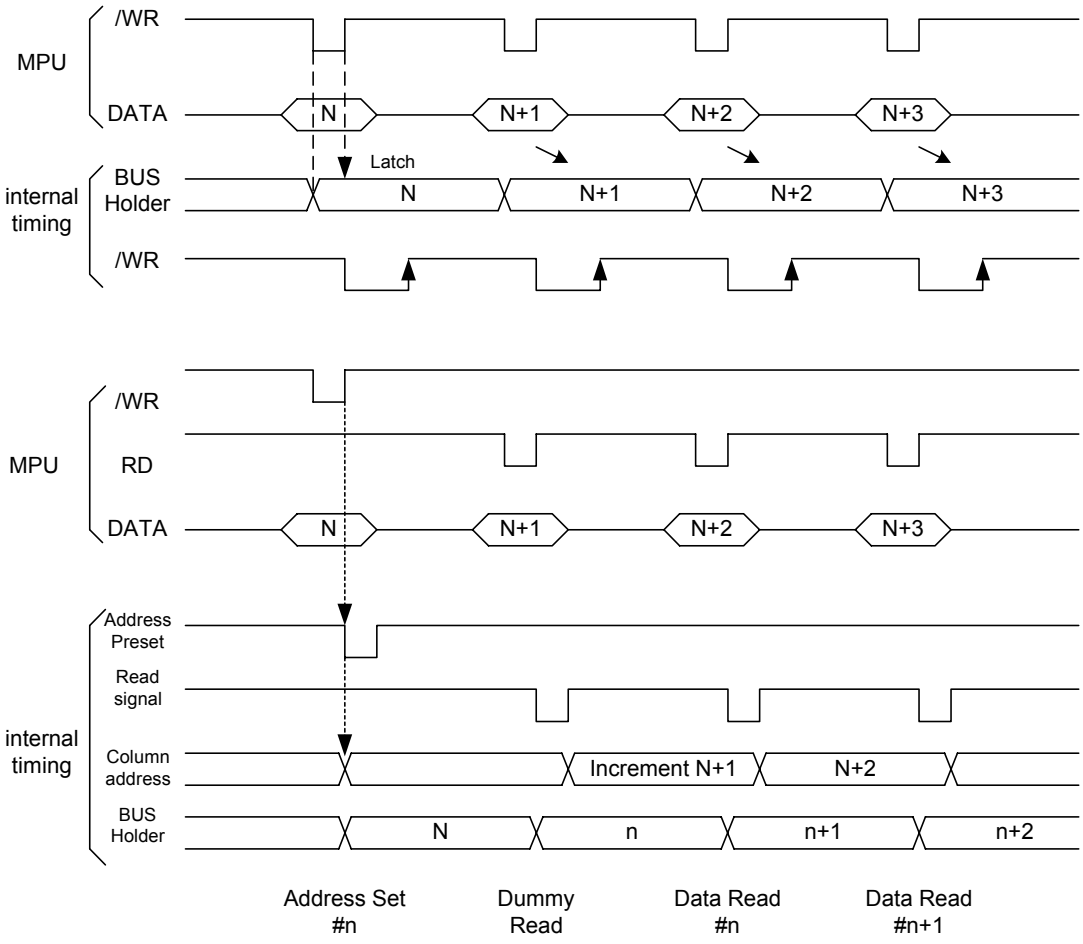


Fig. 3

The Page Address Circuit

The page address of the *DDRAM* is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address 8 is the page for the RAM region used only by the static indicators, and only display data D0 is used.

The Line Address Circuit

The line address circuit specifies the line address relating to the common output when the contents of the *DDRAM* are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for EM65565A when the common output mode is reversed. The display area is a 65 lines area for the EM65565A from the display start line address.

If the line address is changed dynamically using the display start line address set command, screen scrolling. Page swapping, etc. can be performed.

The Column Addresses circuit

The *DDRAM* column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column address stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, the ADC command can be used to reverse the relationship between the *DDRAM* column address and the segment output. Because of this, the constraints on the IC layout when the *LCD* module is assembled can be minimized.

Display Data RAM (*DDRAM*)

The *DDRAM* is a RAM that stores the dot data for the display. It has a 65×132 bits. It is possible to access the desired bit by specifying the page address and the column address. The D7 to D0 display data from the MPU corresponds to the *LCD* common direction. There are few constraints at the time of display data transfer when multiple EM65565A chip is used. Thus and display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the *DDRAM* is accessed asynchronously during *LCD*, it will not cause adverse effects on the display (such as flickering).

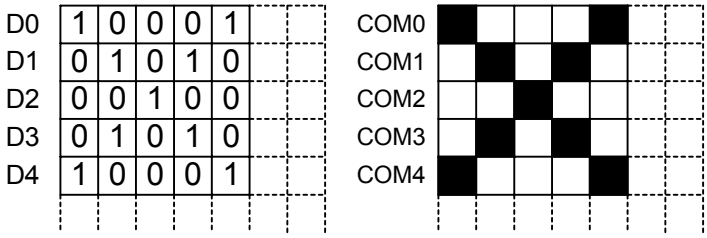


Fig. 4

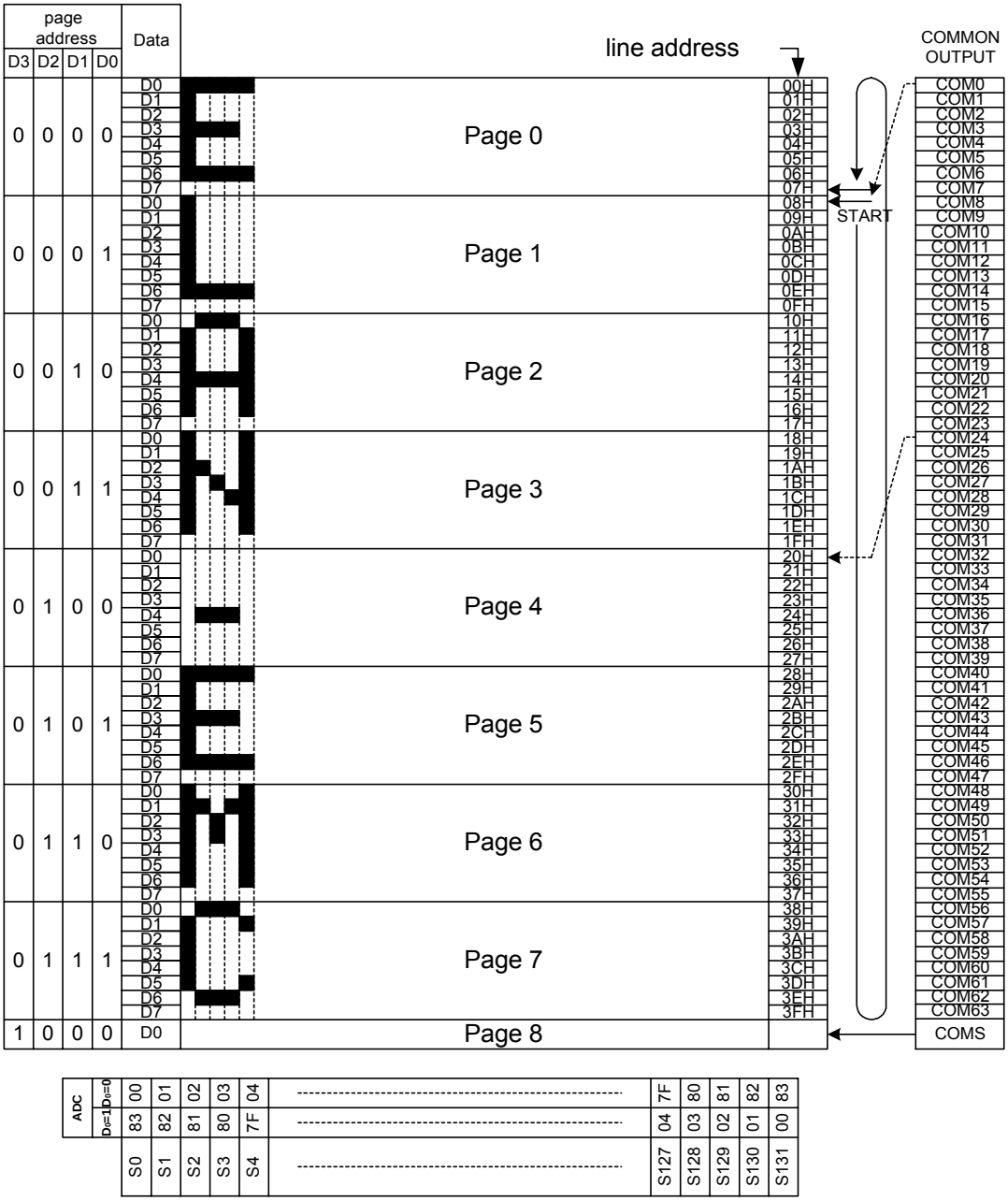

page address
D3 D2 D1 D0
Data
line address
COMMON OUTPUT
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
START
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47 COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63
COMS
ADC
S0 S1 S2 S3 S4 ---------- S127 S128 S129 S130 S131

Fig. 5 *DDRAM*

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver from the *DDRAM*.

Because the display normal/reverse status. Display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the *DDRAM* itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S="H" and DCLKS="H". When DCLKS="L" the oscillation stops, and the display clock is input through the DCLK terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the *DDRAM* by the MPU. Consequently, even if the *DDRAM* is accessed asynchronously during *LCD*, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave from using a two-frames alternating current drive method, as is shown in Figure 6, for the liquid crystal drive circuit.

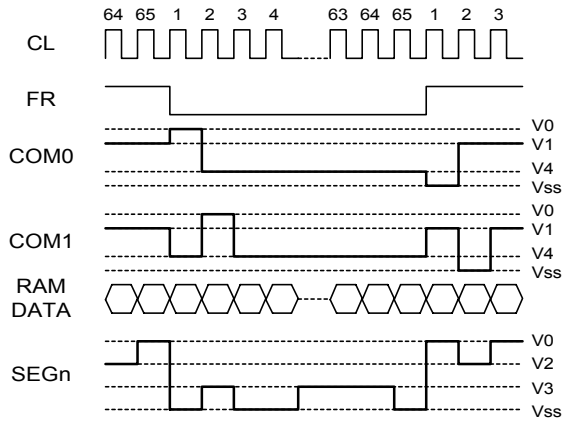


Fig. 6

When plural EM65565A chip are used. The slave chips must be supplied the display timing signals (FR, DCLK, /BCT) from the master chip(s). Explain as following Table 5.

Table 5

Operating Mode		FR	DCLK	/BCT
Master (M/S = “H”)	The internal oscillator circuit is enabled (DCLKS=”H”)	O	O	O
	The internal oscillator circuit is disabled (DCLKS=”L”)	O	I	O
Slave (M/S = “L”)	The internal oscillator circuit is enabled (DCLKS=”H”)	I	I	I
	The internal oscillator circuit is disabled (DCLKS=”L”)	I	I	I

O: Output, I: Input

Note: When the EM65565A is used for the master/slave configuration, each of the DCLKS pins is set to the same level together.

The Common Output Status Select Circuit

In the EM65565A chip, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constrains in IC layout at the time of *LCD* module assembly can be minimized.

Table 6

Status	COM Scan Direction
Normal	COM0→ COM63
Reverse	COM63 → COM0

The *LCD* Driver Circuits

These are a 197-channel that generates four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output. Figure 7 shows examples of the SEG and COM output waveform.

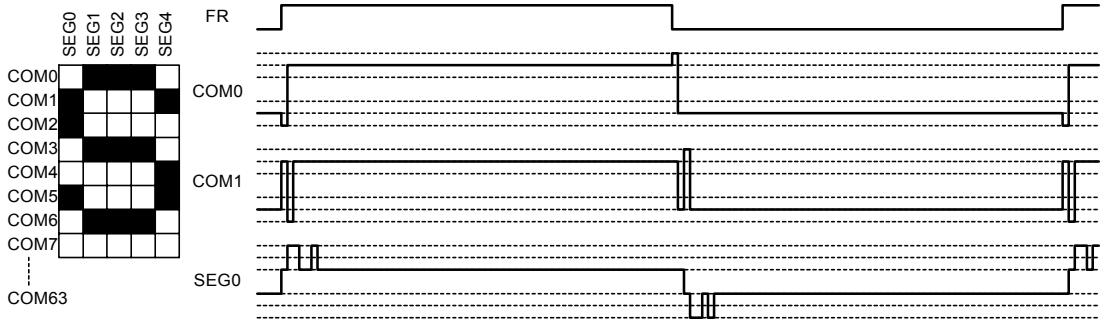


Fig. 7

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for liquid crystal drivers. They comprise Booster (step-up voltage) circuits, Voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuit can turn the Booster circuits, the voltage regulator circuits and the voltage follower circuit ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel.

The Step-up Voltage Circuit:

Using the step-up voltage circuit equipped within the EM65565A chip it is possible to product a five times step-up, a four times step-up, and a three times, and a two times step-up of the V_{CI} voltage levels. The step-up voltage relationships are shown in Figure 8.

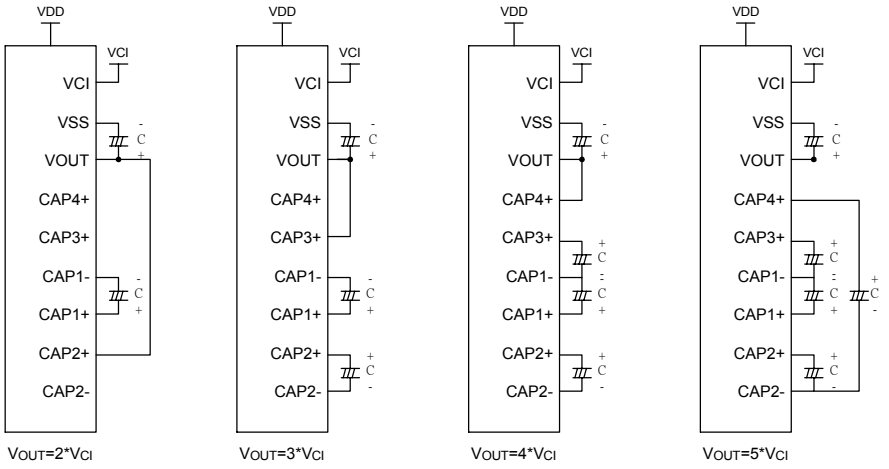


Fig. 8

The Voltage Regulator Circuit

The step-up voltage generated at V_{OUT} output the *LCD* driver voltage V_0 through the voltage regulator circuit.

Because the EM65565A chip has an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. Moreover, in the EM65565A, types of thermal gradients have been prepared as V_{REG} options: Approximately –0.05%/°C, -0.2%/°C and external input (from V_{RS} pin)

(a) When the V_0 voltage regulator internal resistors are used

Through the use of the V_0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the *LCD* brightness. The V_0 voltage can be calculated using equation A over the range where $V_0<V_{OUT}$.

$$V_0 = (1+\frac{R_b}{R_a})V_{EV} = (1+\frac{R_b}{R_a})(1-\frac{\alpha}{162})V_{REG} \quad \text{----------(A)}$$

$$\because V_{EV} = (1-\alpha/162)V_{REG}$$

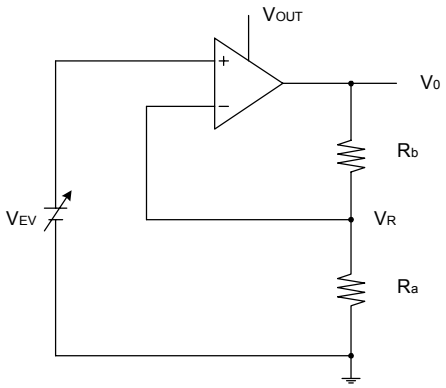


Fig. 9

V_{REG} is the IC-internal fixed voltage supply, and its voltage at Ta=25°C is shown as following:

Type of thermal gradient	V_{REG}
-0.05%/°C	2.1V
-0.2%/°C	2.1V
External input	V_{RS}

The α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 7 shows the value for α depending on the electronic volume register settings.

Table 7

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

R_b/Ra is the V_0 voltage regulator internal resistor ratio and can be set to 8 different levels through the V_0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in Table 8 depending on the 3-bit data settings in the V_0 voltage regulator internal resistor ratio register.

Table 8

Register			Type of thermal gradients		
			-0.05%/°C	-0.2%/°C	External input
D2	D1	D0	1+(Rb/Ra) ratio		
0	0	0	3.0	3.0	1.5
0	0	1	3.5	3.5	2.0
0	1	0	4.0	4.0	2.5
0	1	1	4.5	4.5	3.0
1	0	0	5.0	5.0	3.5
1	0	1	5.5	5.5	4.0
1	1	0	6.0	6.0	4.5
1	1	1	6.4	6.4	5.0

Fig.9 show, V_0 voltage measured by values of the internal resistance ratio resistor for V_0 voltage adjustment and electric volume resister for each temperature grade model. When Ta=25°C. The V_0 voltage as a function of the V_0 voltage regulator, internal resistor ratio register and the electronic volume register.

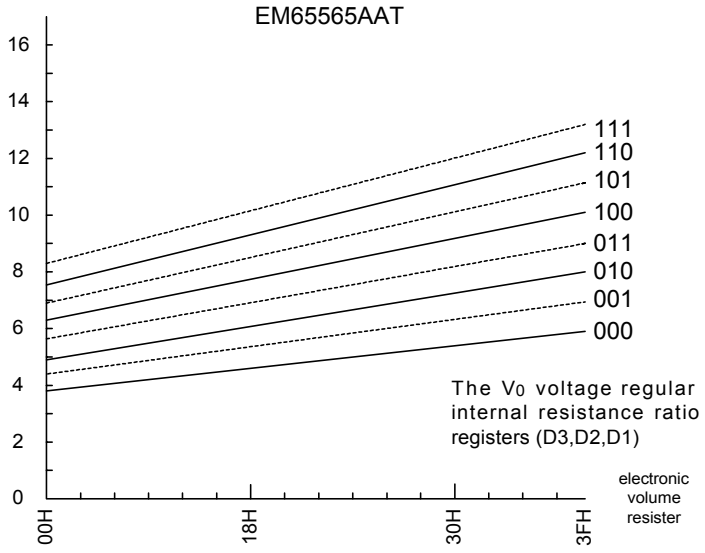


Fig. 10 Where the Thermal Gradient= -0.05%/°C and -0.2%/°C

(b) When an External Resistance is Used

The liquid crystal power supply voltage V_0 can also be set without using the V_0 voltage regulator internal resistors by adding resistors Ra' and Rb'. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the *LCD* by controlling the *LCD* power supply voltage V_0 through commands. In the range where $V_0<V_{OUT}$, the V_0 voltage can be calculated using equation B based on the external resistances Ra' and Rb'.

$$V_5 = (1+\frac{R_b'}{R_a'})V_{EV} = (1+\frac{R_b'}{R_a'})(1-\frac{\alpha}{162})V_{REG} \quad \text{----------(B)}$$

$$\because V_{EV} = (1-\alpha/162)V_{REG}$$

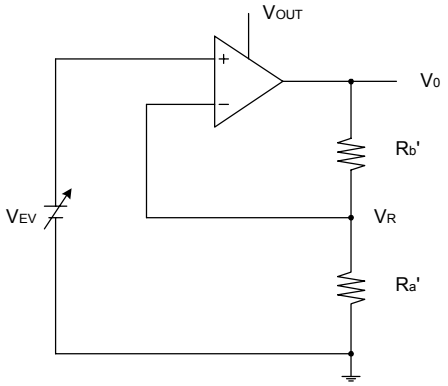


Fig. 11

The Liquid Crystal Voltage Generator Circuit

The V_0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3 and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3, and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for EM65565A can be selected.

The Power Supply Control Circuit

The power supply circuit equipped in the EM65565A Series chip has very power consumption (normal mode: /PCT = "H"). However, for *LCD*s or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the /PCT terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Step1: display OFF.

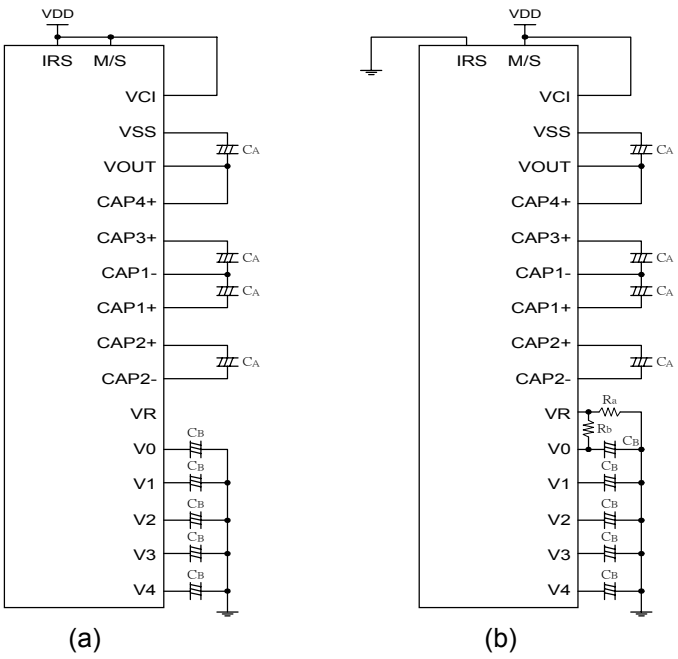
Step2: display all point ON.

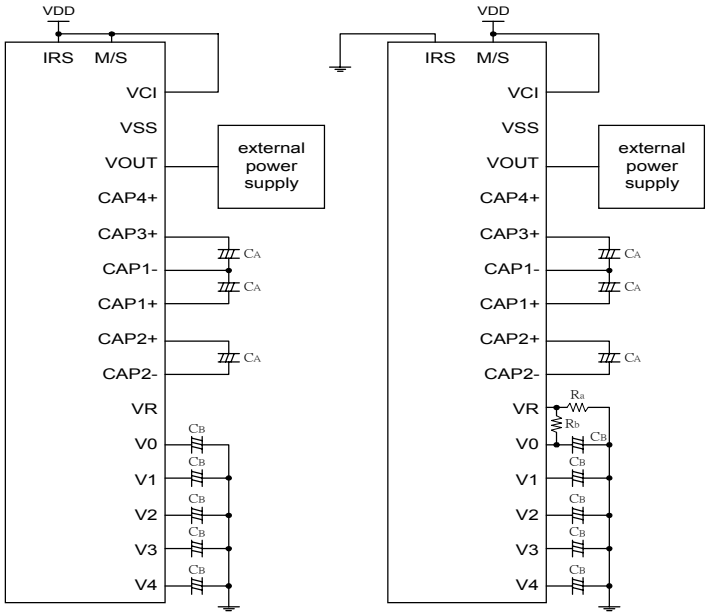
Step3: internal power supply OFF.

Reference Circuit Example

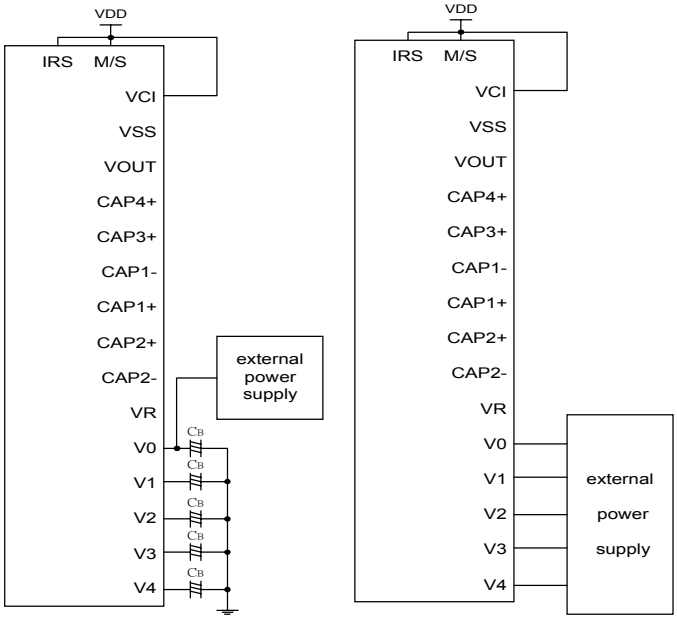
Figure 21 shows reference circuit examples.

1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit, and the voltage regulator internal resistor is used. Fig 12-(a)
2. When used all of the step-up circuit, voltage regulating circuit and V/F circuit, and the voltage regulator internal resistor is not used. Fig 12-(b).
3. When the voltage regulator circuit, V/F circuit and the V_0 voltage regulator internal resistor are used. Fig 12-(c).
4. When the voltage regulator circuit and V/F circuit are used, and the V_0 voltage regulator internal resistor is not used. Fig 12-(d).
5. When the V/F circuit is used. Fig 12-(e)
6. When not using any internal LCD power supply circuit. Fig 12-(f)




VDD
IRS
M/S
VCI
VSS
VOUT
CAP4+
CAP3+
CAP1-
CAP1+
CAP2+
CAP2-
VR
V0
V1
V2
V3
V4
external power supply
CA
CB
Ra
Rb

(c) (d)


VDD
IRS
M/S
VCI
VSS
VOUT
CAP4+
CAP3+
CAP1-
CAP1+
CAP2+
CAP2-
VR
V0
V1
V2
V3
V4
external power supply
CB

(e) (f)

Fig. 12

Examples of shared reference settings. When V_0 can very between 8 and 12V

Item	Set value
C_A	1.0 – 4.7 μF
C_B	0.47 - 1.0 μF

Notes:

1. Because the V_R terminal input impedance is high, use short leads and shielded lines.
2. C_A and C_B are determined by the size of the *LCD* being driven. Select a value that will stabilize the liquid crystal drive voltage.

The Reset Circuit

When the /RST input falls to “L”, these LSI reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: normal (ADC command D0 = 0)
4. Power control resister: (D2, D1, D0) = (0,0,0)
5. Serial interface internal register data clear
6. *LCD* power supply bias ratio: 1/9 bias
7. Read-modify-write OFF
8. Static indicator OFF: Static indicator register: (D1, D2) = (0,0)
9. Display start line set to first line
10. Column address set to address 0
11. Page address set to page 0
12. Common output status normal
13. V_0 voltage regulator internal power supply ratio set mode clear
    V_0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1,0,0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0)
15. Test mode clear

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect. The /RST terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RST terminal.

In the EM65565A, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the /RST terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the /RST terminal is “L” the display timing generator circuit is stopped, and the DCLK, FR, FRS, and /BCT terminals are fixed to “H”. There is no influence on the D0 to D7 terminals.

COMMANDS

Table 9

Command	Command Code											Functions
	D/I	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	**D**	LCD display ON/OFF D=0:OFF, D=1:ON
Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
Column address set upper bit	0	1	0	0	0	0	1	Most column address				Sets the most 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least column address				Sets the least 4 bits of the display RAM column address.
Status read	0	0	1	Status				0	0	0	0	Reads the status data
Display data write	1	1	0	Write data								Writes to the display RAM
Display data read	1	0	1	Read data								Reads from the display RAM
ADC select	0	1	0	1	0	1	0	0	0	0	**D**	Sets the display RAM address SEG output correspondence D=0:normal, 1:reverse
Display normal/reverse	0	1	0	1	0	1	0	0	1	1	**D**	Sets the LCD display normal/reverse D=0:normal, 1:reverse
Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	**D**	Display all points D=0: normal display D=1: all points ON
LCD bias set	0	1	0	1	0	1	0	0	0	1	**D**	Sets the LCD drive voltage bias ratio D=0: 1/9, D=1:1/7
Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address only increment at write: +1
End	0	1	0	1	1	1	0	1	1	1	0	Stop read-modify-write
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Common output mode select	0	1	0	1	1	0	0	**D**	.	.	.	Select COM output scan direction D=0:normal direction D=1:reverse direction
Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power Supply operating mode
V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio mode
Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V_0 output voltage electronic volume register
Electronic volume Register set	0	1	0	.	.	Electronic volume value						
Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	**D**	D=0:OFF, D=1:ON
Static indicator register set	1	0	1	.	.	.	.	.	.	Mode		Set the flashing mode

(Continuous)

Command	Command Code										Functions
	D/I	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Power saver	0	1	0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Display OFF and display all points ON compound command
NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
Test	0	1	0	1	1	1	1	.	.	.	.	Command for IC test. Don't use this command

. Display ON/OFF

This command turns the display on and off. When the display OFF command is executed when in display all point ON mode, power saver mode is entered.

(AEH, AFH)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	0	1	0	1	1	1	**D**

D=0:Display turn OFF

D=1:Display turn ON

. Set Display start line

This command specifies a line address thus marking the display line that corresponds to C0.

(40H to 7FH)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

. Set Column address

This command specifies a *DDRAM* column address. The column address is split into two parts (the upper 4-bits and the lower 4-bits) when it set. The column address is automatically incremented by 1 each time the MPU accesses from the set address to the *DDRAM*. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 131 (83H), and the page address is not changed continuously.

Upper bits (10H to 18H), Lower bits (00H to 0FH)

D/I	/RD	/WR(R/W)		D7----------D0							
0	1	0	Upper bits	0	0	0	1	A7	A6	A5	A4
			Lower bits	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
↓	↓	↓	↓	↓	↓	↓	↓	↓
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

. Set Page address

This command is used to specify a page address equivalent to a row address for MPU access to the *DDRAM*.

(B0H to B8H)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page number
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	1	1	1	7
1	0	0	0	8

. Select ADC

This command specifies a segment driver direction. The column address is automatically incremented by 1 each time when the read or write the display data.

(A0H, A1H)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	0	1	0	0	0	0	**D**

D=0 clockwise output (forward) **S0**(00H)→**S131**(83H)

D=1 counterclockwise output (reverse) **S0**(83H)→**S131**(00H)

. Write display data

Write data from data bus into *DDRAM*. Since the column address is automatically incremented by "1" after write.

D/I	/RD	/WR(R/W)	D7----------D0
1	1	0	Write data

. Read display data

Read data from *DDRAM* onto data bus. Since the column address is automatically incremented by "1" after read. When the serial interface is used, reading of the display data becomes invalid.

D/I	/RD	/WR(R/W)	D7----------D0
1	0	1	Read data

. Read status

D/I	/RD	/WR(R/W)	D7----------D0							
0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0

Busy: the busy bit indicated whether the driver accept instruction or not.

Busy=0: the driver will be accepted new instruction

Busy=1: no new instruction will be accepted.

ADC:

ADC=0: reverse (column address 131-n ↔ segment driver n)

ADC=1: Normal (column address n ↔ segment driver n)

ON/OFF: indicated the current status of the display

ON/OFF=0: display ON

ON/OFF=1: display OFF

Reset: indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

Reset=0: Normal operation

Reset=1: currently executing reset instruction

. Read-modify-write

This instruction defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an "End" instruction is received.

When the "End" instruction is entered, the column address returned to the one used during input of Read-modify-Write instruction. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

Any instruction can be used in this instruction. However, the column address set instruction cannot be used.

(E0H)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	1	1	0	0	0	0	0

. End

This instruction cancels the read modify write instruction, returning the column address to the initial mode address.

(EEH)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	1	1	0	1	1	1	0

. Reset

This instruction initialization the display data line register, the column address, the page address counter, the V_0 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and read-modify-write mode and test mode are released. It does not affect the contents of the *DDRAM*. When the power supply is turned on, a reset signal is entered in the /RST pin. The reset instruction cannot be used instead of this reset signal.

(E2H)

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	1	1	0	0	0	1	0

. Display all point ON

This command makes it possible to force all display points ON regardless of the content of the *DDRAM*. The contents of the *DDRAM* are maintained when this is done.

(A4H, A5H)

D/I	/RD	/WR(R/W)	D7----------D0								Setting
0	1	0	1	0	1	0	0	1	0	**D**	D=0: Normal display D=1: Display all point ON

. Display Normal /Reverse

This command can reverse the lit and unlit display without overwriting the contents of the *DDRAM*. When this is done the *DDRAM* contents are maintained.

(A6H, A7H)

D/I	/RD	/WR(R/W)	D7----------D0								Setting
0	1	0	1	0	1	0	0	1	1	**D**	D=0: Normal (RAM data “H” LCD ON) D=1: Reverse (RAM data “L” LCD ON)

. LCD Bias Set

This command specifies the voltage Bias ratio for *LCD*

(A2H, A3H)

D/I	/RD	/WR(R/W)	D7----------D0								Setting
0	1	0	1	0	1	0	0	0	1	**D**	D=0: 1/9 Bias D=1: 1/7 Bias

. Common Output Mode Select

This command can select the scan direction of the common output terminal

D/I	/RD	/WR(R/W)	D7----------D0								Setting
0	1	0	1	1	0	0	**D**	.	.	.	D=0: Normal COM0→COM63 D=1: Reverse COM63→COM0

. Power Controller Set

This command set the function of power supply circuit

D/I	/RD	/WR(R/W)	D7----------D0								Setting
0	1	0	0	0	1	0	1	**D2**	**D1**	**D0**	Voltage Follower Circuit D0=0: OFF, D0=1: ON Voltage Regular Circuit D1=0: OFF, D1=1: ON Booster Circuit D2=0: OFF, D2=1: ON

. V_0 Voltage Regulator Internal Resistor Ratio Set

This command set the V_0 voltage regulator internal resistor ratio

(20H, 27H)

D/I	/RD	/WR(R/W)	D7----------D0								Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								↓	↓	↓	↓
								1	1	1	Large

. The Electronic Volume

This command is used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other

The Electronic Volume Mode Set:

When this command is input, the electronic volume register set command enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used.

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set:

This command specifies *LCD* drive voltage V_0 assumes one of the 64 Voltage level. When the electronic volume function is not used, set this to (1,0,0,0,0,0).

D/I	/RD	/WR(R/W)	D7----------D0								V_0
0	1	0	.	.	0	0	0	0	0	1	Small
			.	.	↓	↓	↓	↓	↓	↓	↓
			.	.	1	1	1	1	1	1	Large

. Static Indicator

This command controls the static drive system indicator display. This is used when one of the static indicator *LCD* drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal.

Static Indicator ON/OFF:

When the static indicator ON command is entered. The static indicator register set command is enabled.

D/I	/RD	/WR(R/W)	D7----------D0								Static Indicator
0	1	0	1	0	1	0	1	1	0	**D**	D=0: OFF D=1: ON

Static Indicator Register Set:

D/I	/RD	/WR(R/W)	D7----------D0								Indicator display state
0	1	0	.	.	.	.	.	.	0	0	OFF
			.	.	.	.	.	.	0	1	Blinking at approximately 0.5 second interval
			.	.	.	.	.	.	1	0	Blinking at approximately one second interval
			.	.	.	.	.	.	1	1	Constantly on

. Power Save

The power save mode is entered when the display all point ON is performed while display OFF mode. The power save mode has the sleep mode and the standby mode. The sleep mode is entered when the static indicator is OFF, and the standby mode is entered when the static indicator is ON. This mode is cleared by the display all point OFF.

The sleep mode operation stops all operations in the *LCD* display system, and as long as there are no accesses from the MPU. In sleep mode operation, the oscillator circuit, the *LCD* power supply circuit, and all *LCD* driver circuits are halted.

The standby mode operation, the duty *LCD* display system operations are halted and only the static driver system for the indicator continues to operate, providing the minimum required consumption current for the static driver. In sleep mode operation, the *LCD* power supply circuit and the duty system *LCD* drive circuits are halted. The static drive system does not operate and the oscillator circuit continues to operate.

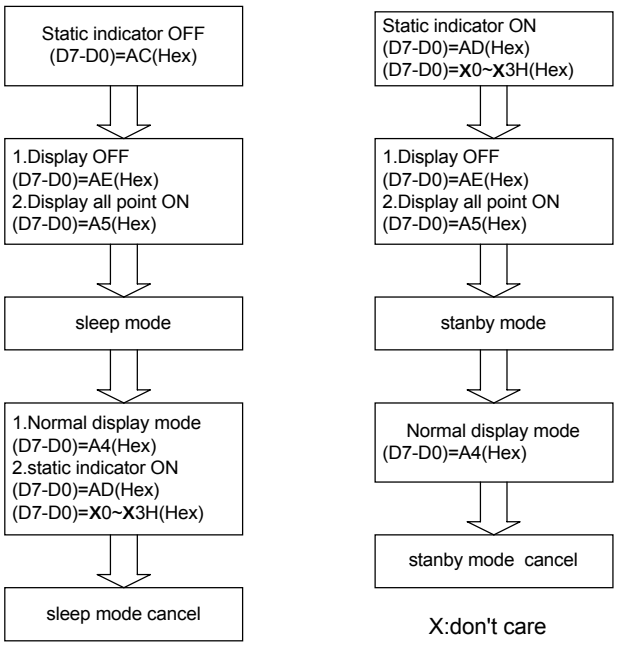


Fig. 13

. NOP

Non-operation command

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	1	1	0	0	0	1	1

. Test

This command is for IC chip testing. It can be cleared by applying a “L” signal to /RST input by the reset command or by using a NOP

D/I	/RD	/WR(R/W)	D7----------D0							
0	1	0	1	1	1	1	.	.	.	.

Initialization:

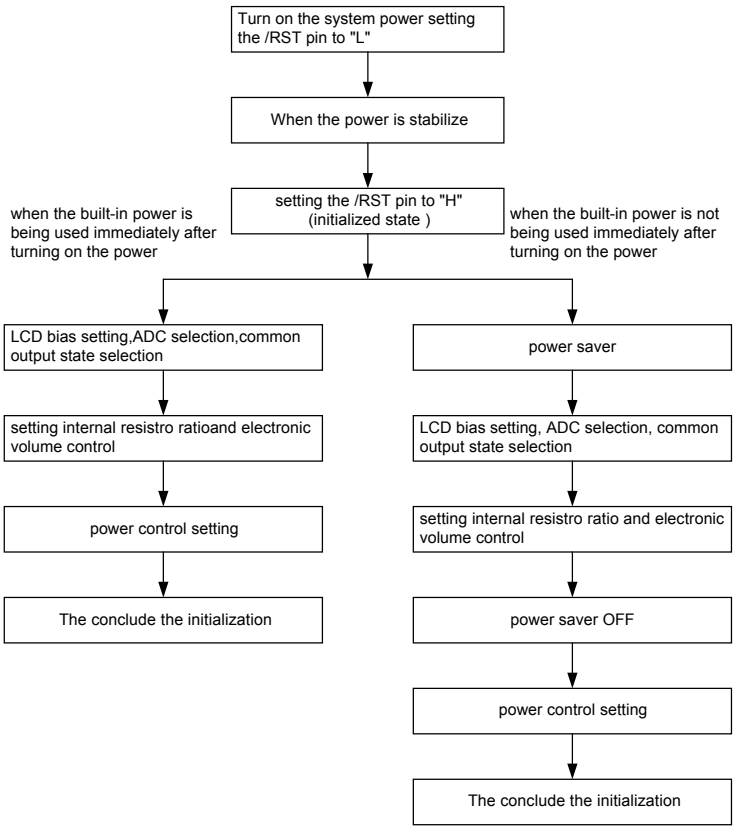


Fig. 14

The Relationship between oscillator frequency f_{OSC}, display clock frequency f_{CL} and the LCD frame rate frequency f_{FR}

Table 10

	f_{CL}	f_{FR}
When the internal oscillator circuit is used (DCLKS="H")	$F_{OSC}/4$	$f_{CL}/65=f_{OSC}/260$
When the internal oscillator circuit is not used (DCLKS="L")	External input	$f_{CL}/260$

ABSOLUTE MAXIMUM RATINGS

Table 11 Absolute Maximum Ratings

Unless otherwise noted, V_{SS} = 0 V

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +4.0	V
Power supply voltage		V_{OUT}, V_0	-0.3 to 12	V
Power supply voltage		V_1, V_2, V_3, V_4	-0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP COG	T_{STR}	–55 to +100 –55 to +125	°C

Notes and Cautions

1. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.
2. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

DC CHARACTERISTICS

Table 12 DC characteristics

Item		Symbol	Condition & Application Pin		Rating			Units
					Min.	Typ.	Max.	
Operating voltage (1)	Recommended voltage	V_{DD}	Pin V_{DD}		2.7		3.3	V
	Possible operating voltage		Pin V_{DD}		2.4		3.3	
Operating voltage (2)	Possible operating voltage	V_0			4.5		12	
		V_1, V_2			$0.6V_0$		V_0	
		V_3, V_4			V_{SS}		$0.4V_0$	
High-level input voltage		V_{IHC}	Pin D/I, D0-D7, /RD, /WR, /CS1, CS2, DCLKS, DCLK, FR, M/S, MPUS, P/S, /BCT, /RST, IRS, /PCT		$0.8V_{DD}$		V_{DD}	
Low-level input voltage		V_{ILC}			V_{SS}		$0.2V_{DD}$	
High-level output voltage		V_{OHC}	I_{OH}=-0.5mA	Pin D0-D7, FR, FRS, /BCT, DCLK	$0.8V_{DD}$		V_{DD}	
Low-level output voltage		V_{OLC}	I_{OL}=0.5mA		V_{SS}		$0.2V_{DD}$	
Input leakage current		I_{LI}	V_{IN}=V_{DD} or V_{SS} Pin D/I, /RD, /WR, /CS1, CS2, DCLKS, M/S, MPUS, P/S, /RST, IRS, /PCT		-1.0		1.0	μA
Output leakage current		I_{LO}	Pin D0-D7, FR, FRS, /BCT, DCLK		-3.0		3.0	
LCD driver ON resistor		R_{ON}	Ta=25°C Pin COM n & SEG n	V_0=8V |ΔV|=0.1V		3.2	5.4	kΩ
Static consumption current		I_{SSO}	Pin V_{SS}, V_{SS2}			0.01	5	μA
Output leakage current		I_{0Q}	V_0=16V, Pin V_0			0.01	15	
Sleep mode consumption current		I_{DDS1}				0.01	5	
Standby mode consumption current		I_{DDS2}				4	8	
Input terminal capacitance		C_{IN}	Ta=25°C, f=1MHz			5.0	8.0	pF
Oscillator Frequency	Internal oscillator	f_{OSC}	Ta=25°C Pin DCLK		18	22	26	kHz
	External input	f_{DCLK}			18	22	26	
Input voltage		V_{CI}	With double		2.4		3.5	V
			With triple		2.4		3.5	
			With quad		2.4		3	
			With five times				2.4	
Supply step-up output voltage		V_{OUT}	Pin V_{OUT}				12	
Voltage follower circuit operating voltage		V_{OUT}	Pin V_{OUT}		6		12	
Voltage follower circuit operating voltage		V_0	Pin V_0		4.5		12	
Base voltage		V_{REG}	Ta=25°C, -0.2%/°C			2.1		

Notes:

1. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.
2. Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C
3. Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF
   Current consumed by total ICs when an external power supply is used.

Display Pattern OFF

Item	Symbol	Condition	Rating			Units
			Min.	Typ.	Max.	
Dynamic Consumption Current	I_{DD} (1)	V_{DD} = 3.0 V, V_0 = 11.0 V	--	16	27	µA

Display Pattern Checker

Item	Symbol	Condition	Rating			Units
			Min.	Typ.	Max.	
Dynamic Consumption Current	I_{DD} (1)	V_{DD} = 3.0 V, V_0 = 11.0 V	--	21	35	µA

• Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Display Pattern ON

Item	Symbol	Condition		Rating			Units
				Min.	Typ.	Max.	
Dynamic Consumption Current	I_{DD} (2)	V_{DD} = 3.0 V, Quad step-up voltage. V_0 = 11.0 V	Normal Mode	--	81	135	µA
			High-Power Mode	--	138	230	

TIMING DIAGRAM

System Bus Read/Write timing I (80-Series MPU)

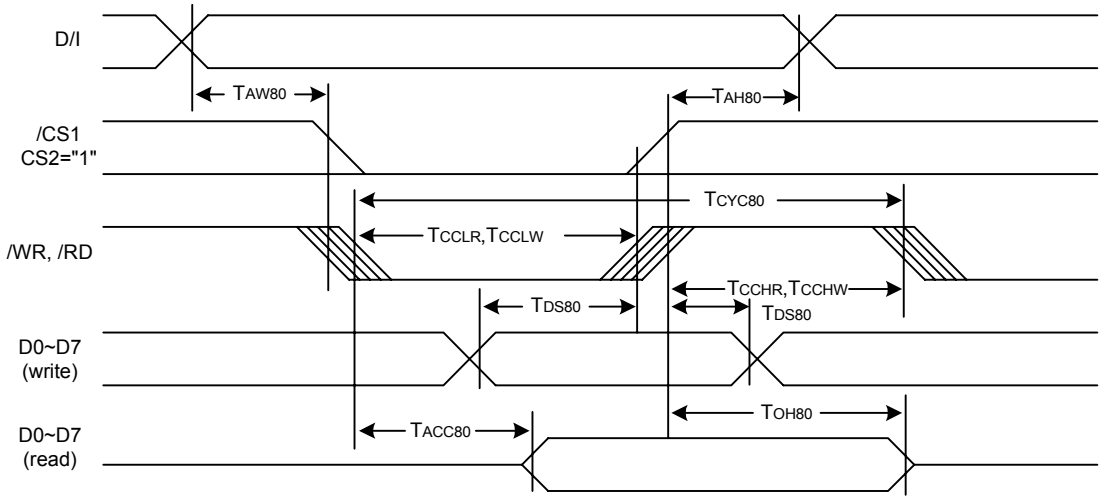


Fig. 15

Table 13 (V_{DD}=2.4V to 3.3V,Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	D/I	T_{AH80}		0	--	ns
Address setup time		T_{AW80}		0	--	ns
System cycle time	D/I	T_{CYC80}		300	--	ns
Control L pulse width (/WR)	/WR	T_{CCLW}		60	--	ns
Control L pulse width (/RD)	/RD	T_{CCLR}		120	--	ns
Control H pulse width (/WR)	/WR	T_{CCHW}		60	--	ns
Control H pulse width (/RD)	/RD	T_{CCHR}		60	--	ns
Data setup time	D0 to D7	T_{DS80}		40	--	ns
Address hold time		T_{DH80}		15	--	ns
/RD access time		T_{ACC80}	C_L=100pF	--	140	ns
Output disable time		T_{OH80}		10	100	ns

Notes:

1. The input signal rise time and fall time (T_R, T_F) is specified at 15 ns or less. When the system cycle time is extremely fast, $(T_R+T_F) \leqq (T_{CYC80}-T_{CCLW}-T_{CCHW})$ for $(T_R+T_F) \leqq (T_{CYC80}-T_{CCLR}-T_{CCHR})$ are specified.
2. All timing is specified using 20% and 80% of V_{DD} as the reference.
3. T_{CCLW} and T_{CCLR} are specified as the overlap between /CS1 being “L” (CS2=”H”) and /WR and /RD being at the “L” level.

System Bus Read/Write Characteristics 2 (68-Series MPU)

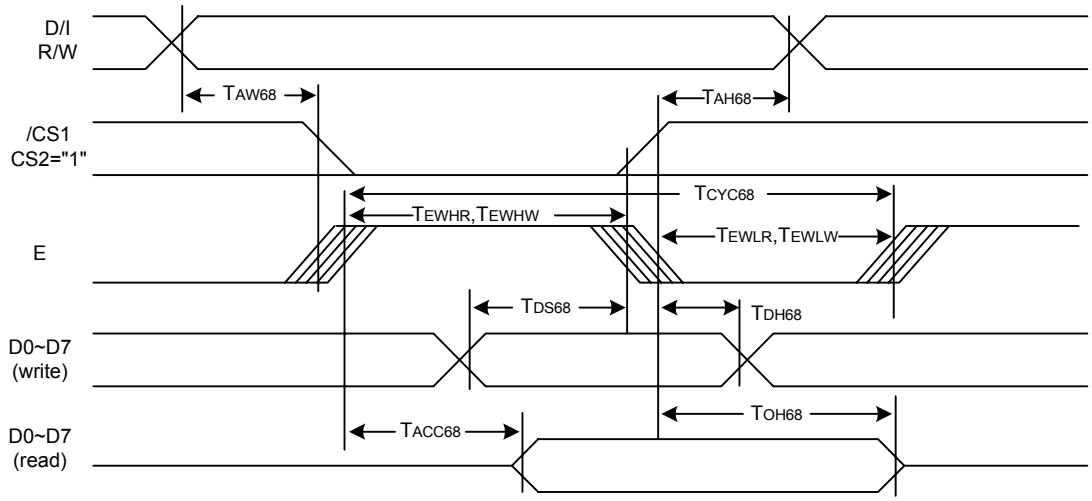


Fig. 16

Table 14 (V_{DD}=2.4V to 3.3V,Ta=-40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		D/I	T_{AH68} T_{AW68}		0 0	-- --	ns ns
System cycle time		D/I	T_{CYC68}		300	--	ns
Data setup time Data hold time		D0 to D7	T_{DS68} T_{DH68}		40 15	-- --	ns ns
Access time Output disable time			T_{ACC68} T_{OH68}	C_L=100pF	-- 10	140 100	ns ns
Enable H pulse time	Read Write	E	T_{EWHR} T_{EWHW}		120 60	-- --	ns ns
Enable L pulse time	Read Write	E	T_{EWLR} T_{EWLW}		60 60	-- --	ns ns

Notes:

1. The input signal rise time and fall time (T_R, T_F) is specified at 15 ns or less. When the system cycle time is extremely fast, $(T_R+T_F) \leqq (T_{CYC68}-T_{EWLW}-T_{EWHW})$ for $(T_R+T_F) \leqq (T_{CYC6}-T_{EWLR}-T_{EWHR})$ are specified.
2. All timing is specified using 20% and 80% of V_{DD} as the reference.
3. T_{EWLW} and T_{EWLR} are specified as the overlap between /CS1 being “L” (CS2=”H”) and E.

The Serial Interface

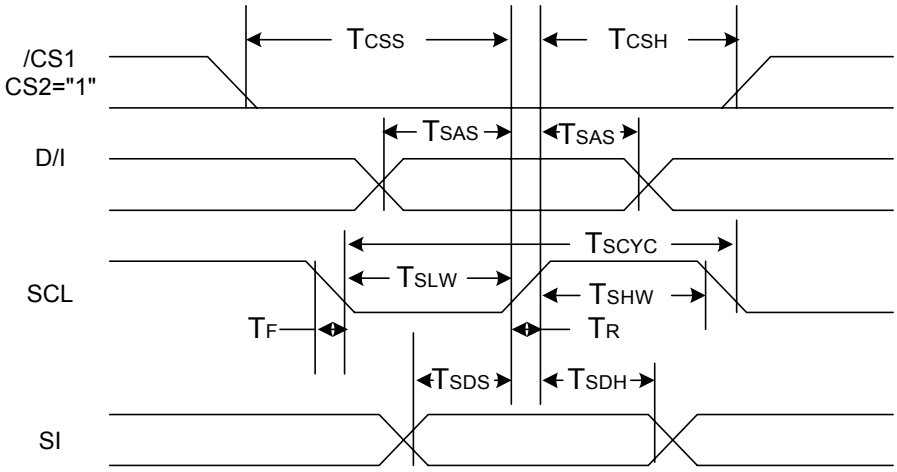


Fig. 17

Table 15 (V_{DD}=2.4V to 3.3V,Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	T_{SCYC}		250	--	ns
SDCLK “H” pulse width		T_{SHW}		100	--	ns
SDCLK “L” pulse width		T_{SLW}		100		ns
Address setup time	D/I	T_{SAS}		150	--	ns
Address hold time		T_{SHA}		150	--	ns
Data setup time	SI	T_{SDS}		100	--	ns
Data hold time		T_{SDH}		100	--	ns
CS-SDCLK time	CS	T_{CSS}		150	--	ns
		T_{CSH}		150	--	ns

1. The input signal rise and fall time (T_R, T_F) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of V_{DD} as the standard.

Display Control Output Timing

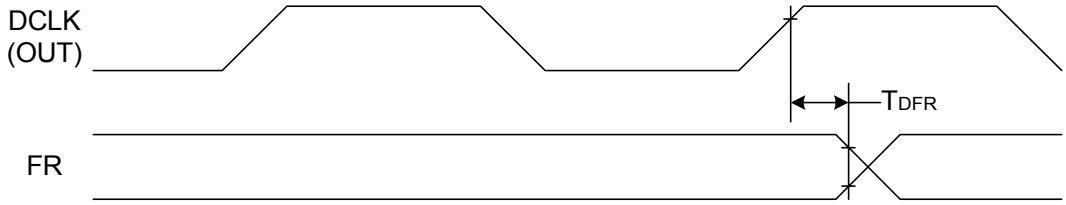


Fig. 18

Table 16 (V_{DD}=2.4V to 3.3V, Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	T_{DFR}	C_L=50pF	--	20	80	ns

● Reset Timing

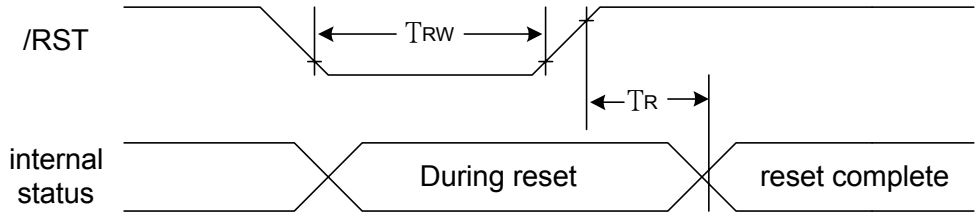


Fig. 19

Table 17 (V_{DD}=2.4V to 3.3V, Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		T_R		--	--	1	μs
Reset “L” pulse width	/RST	T_{RW}		1	--	--	μs

*All timing is specified with 20% and 80% of V_{DD} as the standard.

The MPU Interface (Reference example)

The EM65565A can be connected to either 80-Series MPU or 68-Series MPU. Moreover, using the serial interface it is possible to operate the EM65565A series chips with fewer signal lines. The display area can be enlarged by use plural EM65565A Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 80-Series MPU

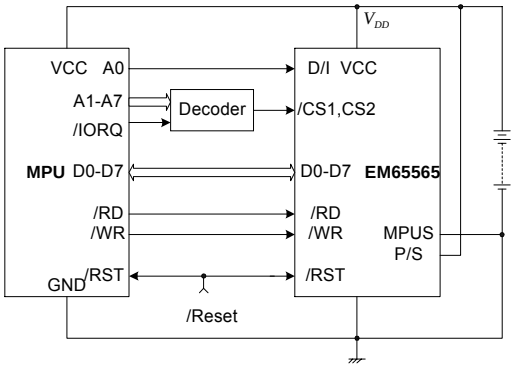


Fig. 20

(2) 68-Series MPU

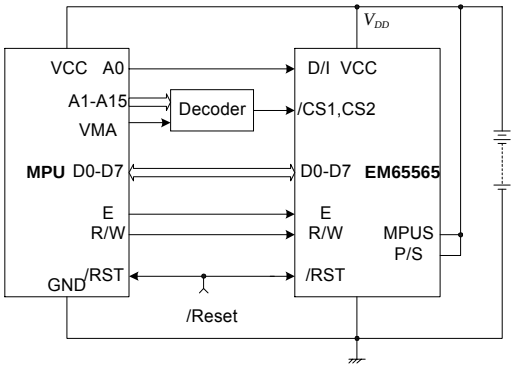


Fig. 21

(3) Using the Serial Interface

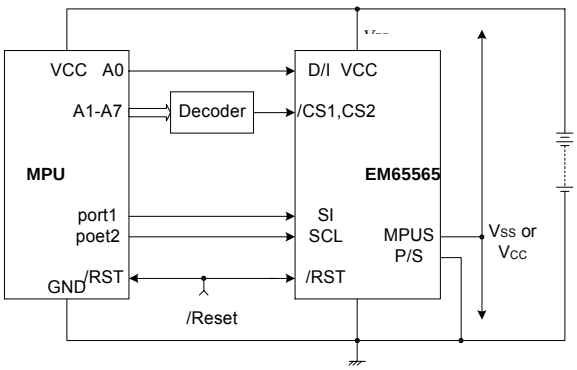


Fig. 22

● **CONNECTIONS BETWEEN *LCD* DRIVERS (REFERENCE EXAMPLE)**

The *LCD* area can be enlarged with ease through the use of multiple EM65565A chips. Use a same equipment type.

EM65565A (master) → EM65565A(slave)

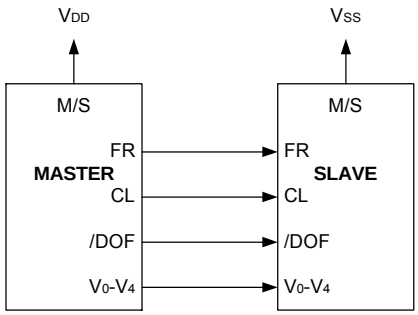


Fig 23

APPLICATION CIRCUIT

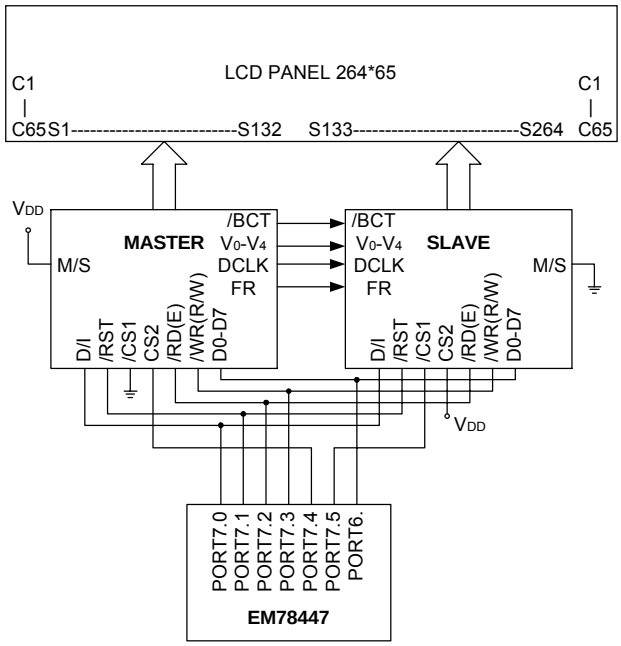


Fig. 24