1. GENERAL DESCRIPTION

The EM78450 is an 8-bit microprocessor developed with low-power, high speed CMOS technology. Integrated into a single chip, are on-chip watchdog timer (WDT), RAM, ROM, real time clock/counter, power down mode, and bi-directional tri-state I/O ports. It is most suited for keyboard encoder development and other related applications.

2. FEATURE

- Operating voltage range: 2.3V~4V, 4V ~ 5.5V option by code.
- Operating temperature range: 0°C ~ 70°C.
- Operating frequency range (base on 2 clocks):
  * Crystal Type : DC ~ 20MHz at 5V, DC ~ 8MHz at 3V and DC ~ 4MHz at 2.3V.
  * RC Type : DC ~ 4MHz at 5V, DC ~ 4MHz at 3V and DC ~ 4MHz at 2.3V.
- Low power consumption:
  * Less then 3 mA at 5V/4MHz
  * Typically 10 μA during sleep mode
- 4K x 13 on chip ROM.
- 11 special function registers.
- 146 × 8 on chip general purpose registers.
- 5 bi-directional I/O ports (35 I/O pins).
- 3 LED direct sink pins with internal serial resistor, option by code.
- One interrupt pin available.
- Built-in RC oscillator with external serial resistor, ±10% variation.
- Built-in power on reset.
- 5 level stacks for subroutine nesting.
- 8-bit real time clock/counter (TCC) with overflow interrupt.
- Options for two oscillator cycle or four oscillator cycle per instruction.
- Power down mode.
- Programmable wake up from sleep circuit on I/O ports.
- Programmable free running on-chip watchdog timer.
- 12 wake-up pins.
- 2 open-drain pins.
- 2 R-option pins.
- Two types of interrupts:
  * External interrupt (/INT).
  * TCC overflow interrupt.
- Package:
  * 40 pins DIP 600mil: EM78450P

3. PIN ASSIGNMENT

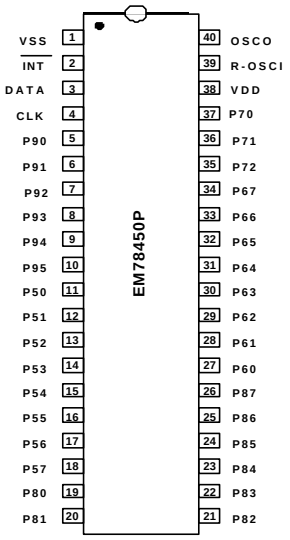


Fig. 1 Pin Assignment

Table 1 Pin Description – EM78450

Symbol	Type	Function Description
R-OSCI	I	XTAL Type: Crystal input; In internal C, external R mode: 56K ohm±5% pull high for 1.8432MHz.
OSCO	O	XTAL Type: Crystal output; In RC mode: Instruction clock output.
P90~P95	I/O	General bi-directional I/O port. All of its pins can be pulled-high by software. P90 and P91 are pin-change wake up pins.
P80~P87	I/O	General bi-directional I/O port. All of its pins can be pulled-high by software. P80 and P81 are also used as the R-option pins.
P70~P72	I/O	3 LED direct-driving pins with internal serial resistor used as output and is software defined.
CLK	I/O	By connecting P74 and P76 together. P74 can be pulled-high by software and it is also a pin-change wake up pin. P76 can be defined as an open-drain output.
DATA	I/O	By connecting P75 and P77 together. P75 can be pulled-high by software and it is also a pin-change wake up pin. P77 can be defined as an open-drain output.
P60~P67	I/O	General bi-directional port. All of its pins can be pulled-high in software, and pin-change wake up pins.
P50~P57	I/O	General bi-directional I/O port. All of its pins can be pulled-high by software.
VDD	-	Power supply pin.

VSS	-	Ground pin.
/INT	I	An interrupt schmitt-triggered pin. The function of interrupts triggers at the falling edge. Users can enable it by software. The internal pull-up resistor is around 50K ohms.

4. FUNCTION DESCRIPTION

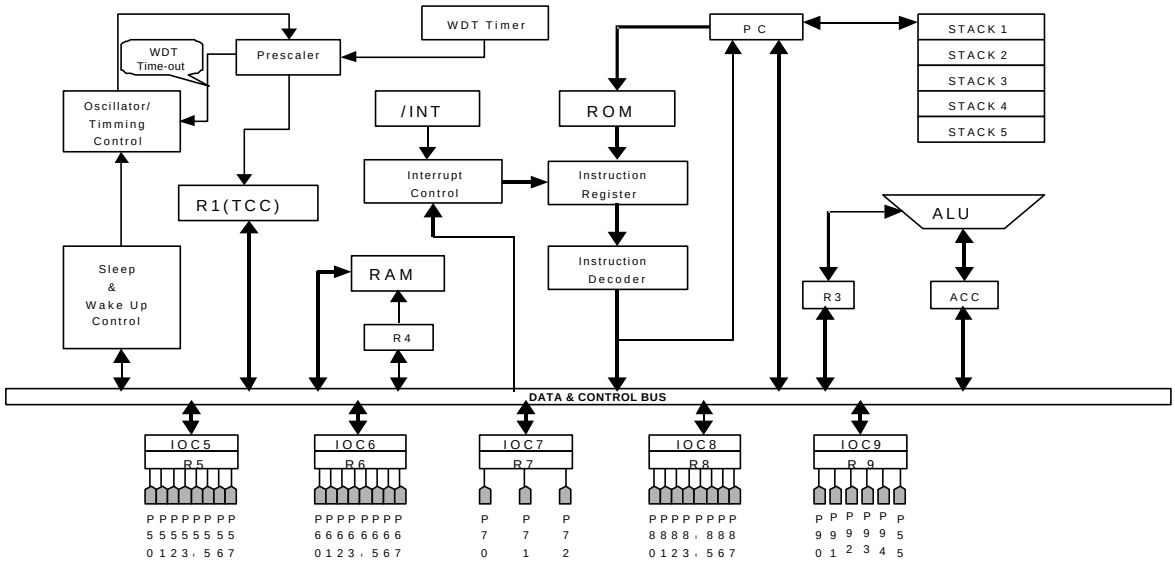


Fig. 2 Functional Block Diagram

4.1 Operational Registers

1. R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

2. R1 (TCC)

- Increased by the instruction cycle clock.
- Written and read by the program as any other register.

3. R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 12 bits wide. The structure is depicted in Fig. 3.
- Generates 4K×13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1K words long.
- R2 is set as all "1"s when under RESET condition.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, JMP" allows jump to any location on one page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- "MOV R2,A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.
- "ADD R2,A" allows a relative address be added to the current PC, and the ninth and tenth bits of PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",....) (except "TBL") will cause the ninth and tenth bits (A8~A9) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address be added to the current PC (R2+A→R2), and contents of the ninth and tenth bits (A8~A9) of PC are not changed. Thus, the computed jump can be on the second (or third, 4th) 256 locations on one program page.
- In case of EM78450, the most significant bits (A10~A11) will be loaded with the contents of bits PS0~PS1 in the status register (R3) upon the execution of a "JMP", "CALL", or any instructions which writes to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents R2. Such instruction will need one more instruction cycle.

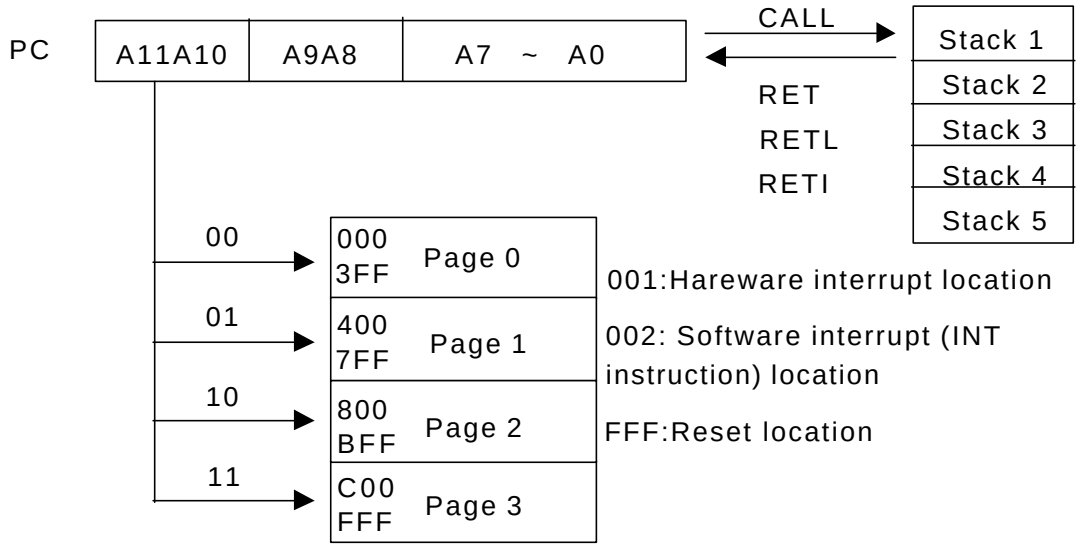


Fig. 3 Program Counter Organization

4. R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

- Bit 0 (C) Carry flag
- Bit 1 (DC) Auxiliary carry flag
- Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- Bit 4 (T) Time-out bit. Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 with WDT timeout.
- Bit 5 (PS0)~6 (PS1) Page select bits. PS0~PS1 are used to preselect a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g., MOV R2,A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- Bit 7 (GP) General read/write bit.

5. R4 (RAM Select Register)

- Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.
- Bits 6~7 determine which bank is activated among the 4 banks.
- If no indirect addressing is used, the RSR is used as an 8-bit wide general purpose read/write register.
- See the configuration of the data memory in Fig. 4.

6. R5~R8 (Port 5 ~ Port8)

- Four 8-bit I/O registers, P74 and P76 read/write data from DATA pin. P75 and P77 read/write data from CLK pin.

7. R9 (Port 9)

- 6-bit I/O registers. The upper 2 bits of R9 are fixed "0".

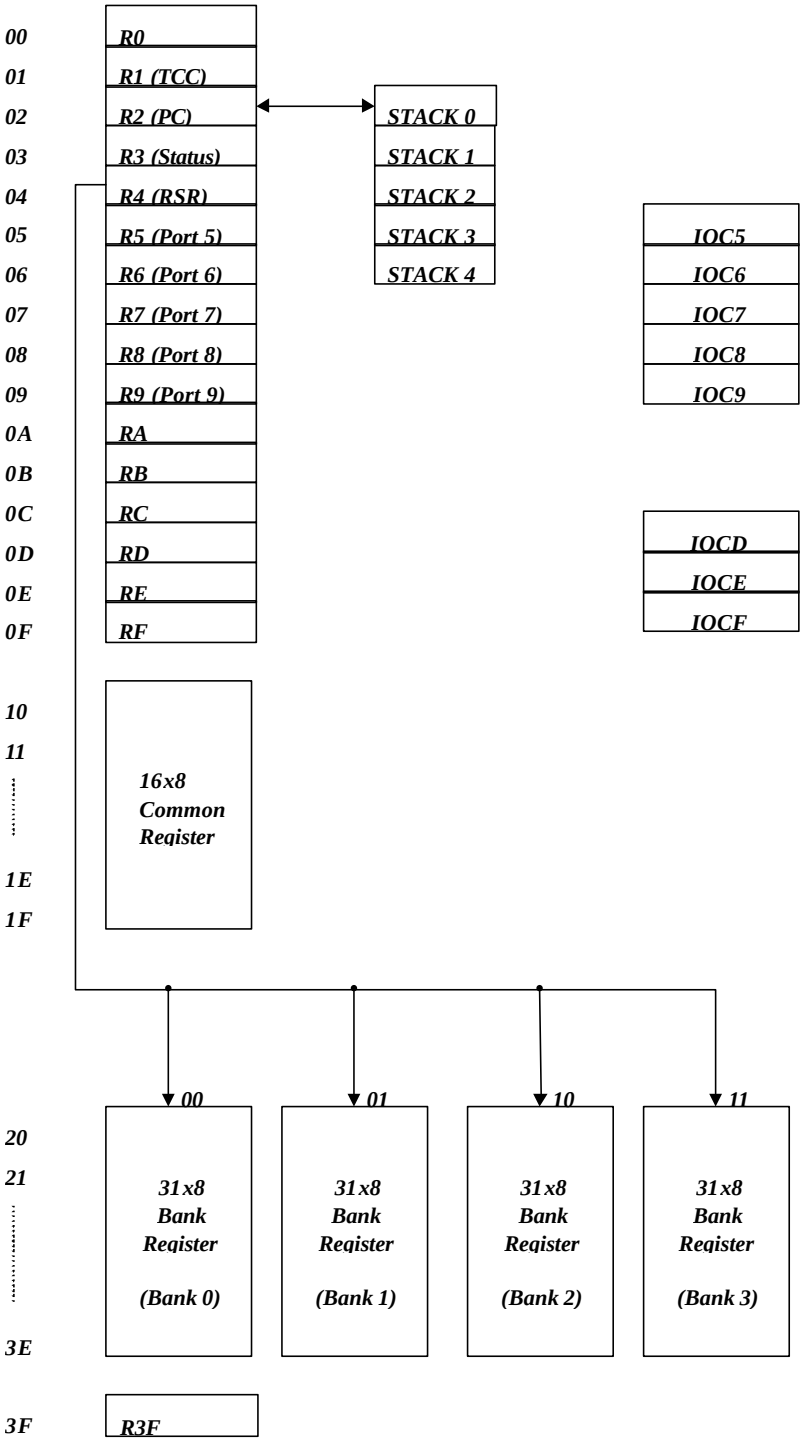


Fig. 4 Data Memory Configuration

8. RA ~ R1F, R20~R3E (General Purpose Register)

- RA~R1F and R20~R3E (including Banks 0~3) are general-purpose registers.

9. R3F (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-			EXIF	TCIF

- Bit 0 (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows, reset by software.
- Bit 1 (EXIF) External interrupt flag. Set by falling edge on /INT pin, reset by software.
- Bits 2~~7 Not used.
- "1" means interrupt request, "0" means non-interrupt.
- R3F can be cleared by instruction and cannot be set by instruction.
- IOCF is the interrupt mask register.
- Note that reading R3F by instruction will result to "logic AND" of R3F and IOCF.

4.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding.
- It is a non-addressable register.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0

- Bit 0 (PSR0)~Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- Bit 3 (PAB) Prescaler assignment bit.

  0: TCC

  1: WDT

- Bit 6 (INT) Interrupt enable flag which cannot be written by CONTW instruction.

0: interrupt masked by DISI.

1: interrupt enabled by ENI/RETI instruction.

- Bit 7 (/PHEN) I/O pin pull-high enable flag.

  0: P60~P67, P74~P75, and P90~P95 have internal pull-high.

  1: pull-high is disabled.

- Bits 0~3, 7 of CONT registers are both readable and writable.
- Bit 4,5 Not used.

3. IOC5 ~ IOC9 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
- IOC5 ~ IOC9 are five I/O direction control registers. Both P74 with P76 and P75 with P77 should not be defined as output pins at same time. Only the lower 6 bits of IOC9 are used.

4. IOCD (Pull-high Control Register)

7	6	5	4	3	2	1	0
S7	-	-	-	/PU9	/PU8	/PU6	/PU5

- PU5, PU6, PU8, PU9 Default = 1, Disable pull high.
- PU6 and PU9 are "AND" gating with PHEN, when each one is set to "0," pull high is enabled.
- S7 selects P70~P72 driving ability.

  0 : Normal output.

  1 : LEDs Driver.

5. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WDTE	SLPC	ROC	-	-	/WUE

- Bit 0 (WUE) Control bit used to enable wake-up function of P60~P67, P74~P75, P90~P91.

  0: Enable wake-up function

  1: Disable wake-up function

  WUE bit is readable and writable.

- Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pin (P80, P81) to be read by the controller. Clearing ROC will disable the R-option function. If the R-option function is used, the user must connect the P81 pin or/and P80 pin to VSS by a 560KΩ external resistor (Rex). If Rex is connected/disconnected, the status of P80(P81) will be read as "0"/"1" when ROC is set to "1" (refer to Fig. 7(b)). ROC bit is readable and writable.
- Bit 4 (SLPC) This bit is set by hardware at the falling edge of wake-up signal and is cleared by software. SLPC is used to control the oscillator operation. The oscillator is disabled (oscillator is stopped, the controller enters the SLEEP2 MODE) on high-to-low transition of SLPC bit and is

enabled (the controller is awakened from SLEEP2 MODE) on low-to-high transition of SLPC bit. In order to ensure the stable output of the oscillator, once the oscillator is disabled and is enabled again, there should be a delay of approximately 18 ms (oscillator start-up timer, (OST)) before the next program instruction is executed. The OST is always activated by wake-up from sleep mode, whether the Code Option bit ENWDT is "0" or not. After waking up, the WDT is enabled if Code Option ENWDT is "1". The block diagram of SLEEP2 MODE and wake-up caused by input triggered is depicted in Fig. 5. SLPC bit is readable and writable.

- Bit 5 (WDTE) Control bit used to enable Watchdog timer. WDTE bit is used only if the CODE Option bit ENWDT is "1". If ENWDT bit is "1", then WDT is disabled/enabled by WDTE bit.

  0: Disable WDT

  1: Enable WDT

  WDTE bit is not used if the CODE Option bit ENWDT is "0". That is, if ENWDT bit is "0", WDT is always disabled no matter what the WDTE bit is. WDTE bit is readable and writable.
- Bit 6 (ODE) Open-drain control bit.

  0: Both P76 and P77 are normal I/O pins.

  1: Both P76 and P77 pins have open-drain output, but built-in internally.

  ODE bit is readable and writable.
- Bits 1,2,7 Not used.

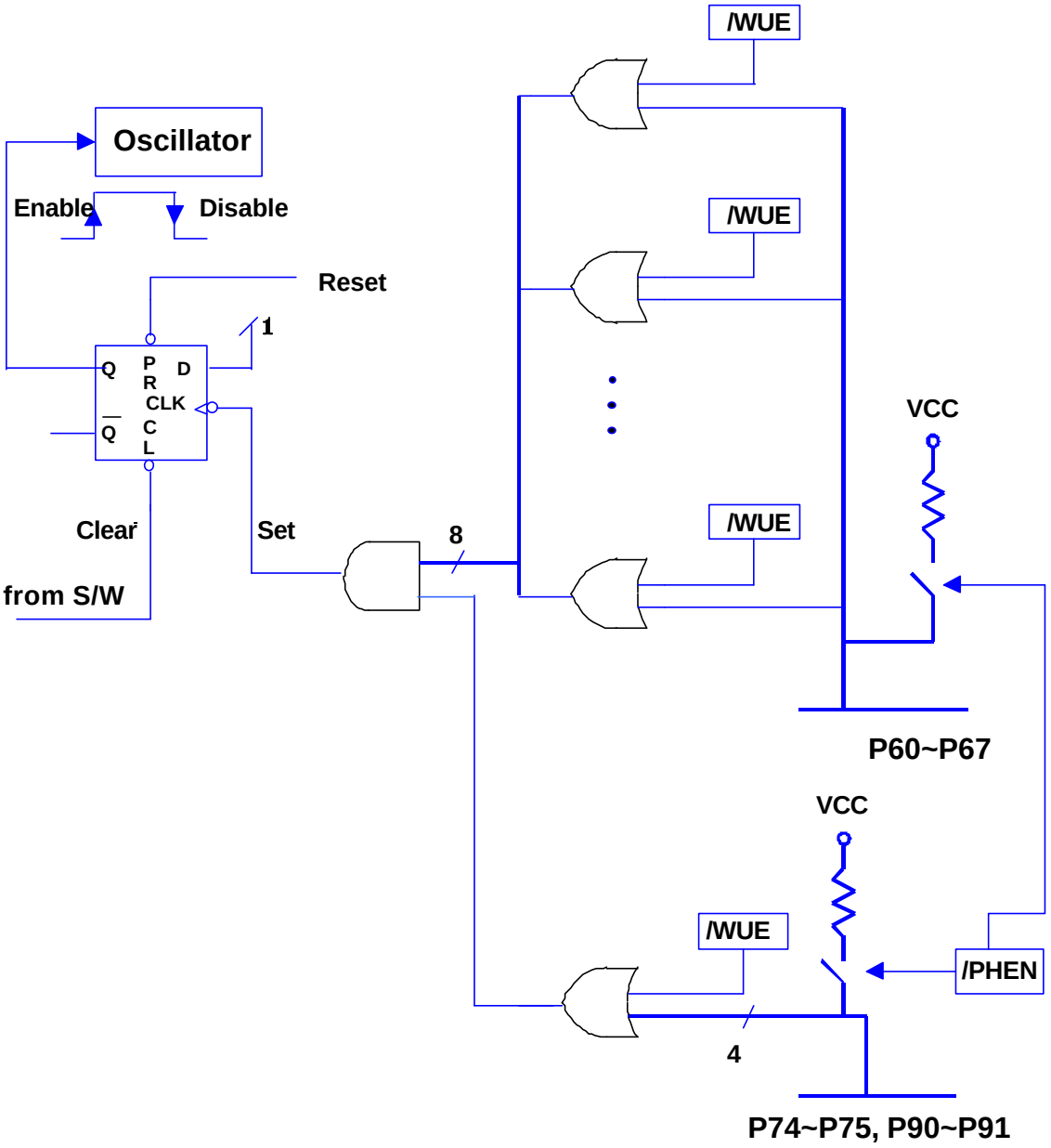


Fig. 5 Block Diagram of Sleep Mode and Wake-up Circuits on I/O Ports

6. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-			EXIE	TCIE

- Bit 0(TCIE) TCIF interrupt enable bit.

  0: disable TCIF interrupt.

  1: enable TCIF interrupt.

- Bit 1 (EXIE) EXIF interrupt enable bit

0: disable EXIF interrupt.

1: enable EXIF interrupt.

- Bits 2~7 Not used.
- Individual interrupt is enabled by setting its associated control bit in IOCF to "1".
- IOCF Register is readable and writable.

4.3 TCC/WDT Prescaler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the WDTC or SLEP instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. TCC will increase by one at every instruction cycle (without prescaler).
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during the normal mode by software programming (if Code Option bit ENWDT is "1"). Refer to WDTE bit of IOCE register. Without presacler, the WDT time-out period is approximately 18 ms[1].

4.4 I/O Ports

The I/O registers, Port 5 ~ Port 9, are bi-directional tri-state I/O ports. P60~P67, P74~P75, and P90~P91 provide internal pull-high and wake-up function through software control. P76~P77 can have open-drain output by software control. P80~P81 are the R-option pins which are enabled by software. When R-option function is used, it is recommended that P80~P81 are used as output pins. When R-option is enabled, P80~P81 must be programmed as input pins. If external resistor is connected to P80 (P81) for R-option function, the current consumption should be taken as an important factor in the applications for low power consideration.

The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5~IOC9) under

[1] Note: VDD=5V, setup time period = 16.5ms±5%

VDD=3V, setup time period = 18ms±5%

program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 7. Note that the reading path source of input and output pins is different when reading the I/O port.

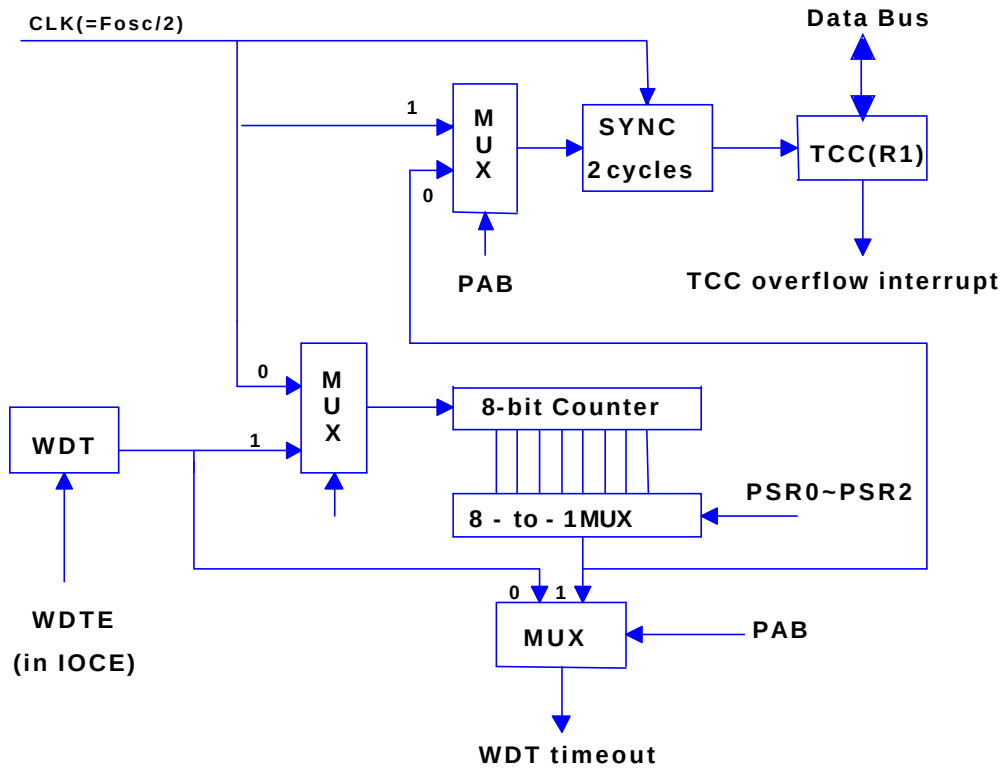


Fig. 6 Block diagram of TCC WDT

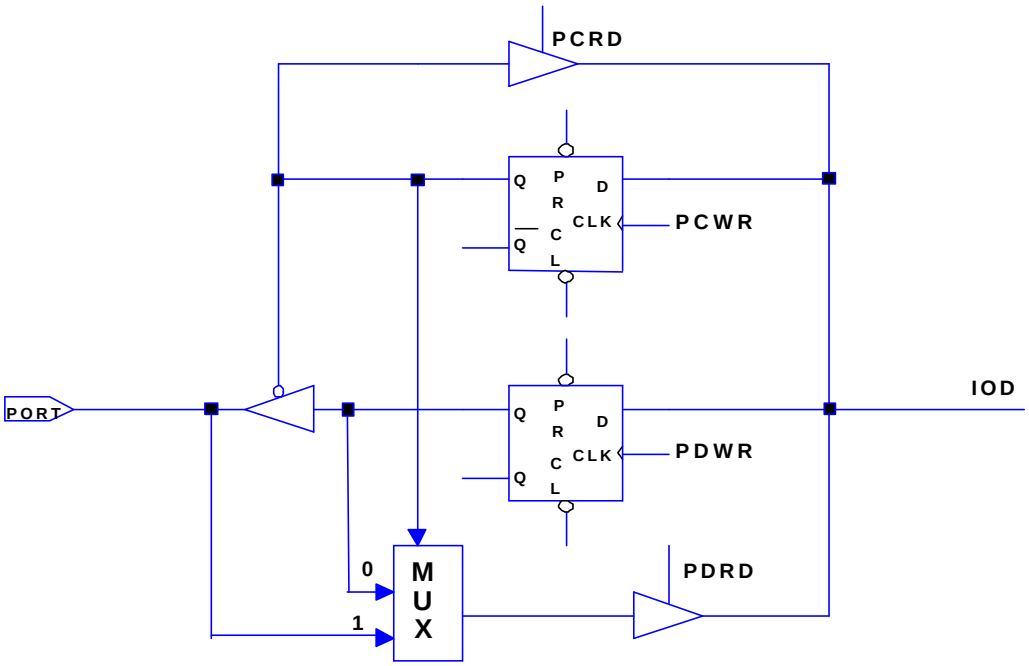


Fig. 7 (a) The Circuit of I/O Port and I/O Control Register

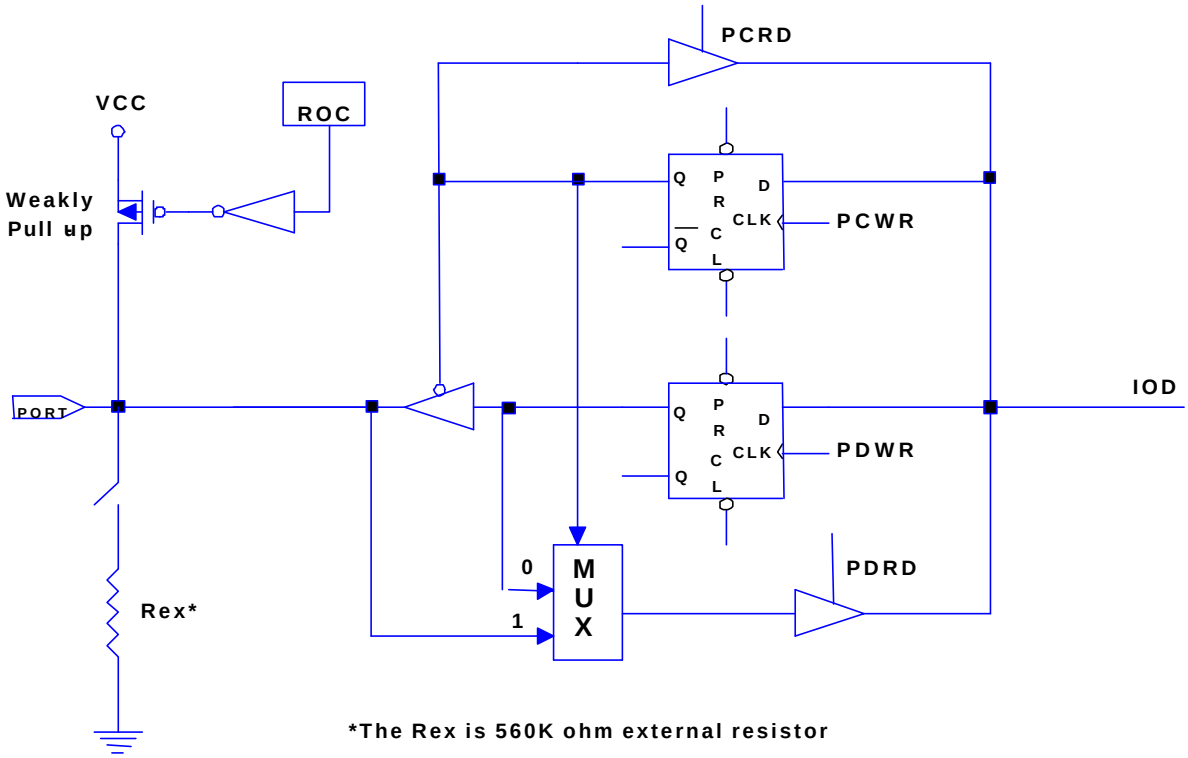


Fig.7(b) The Circuit of I/O Port with R-option (P80,P81)

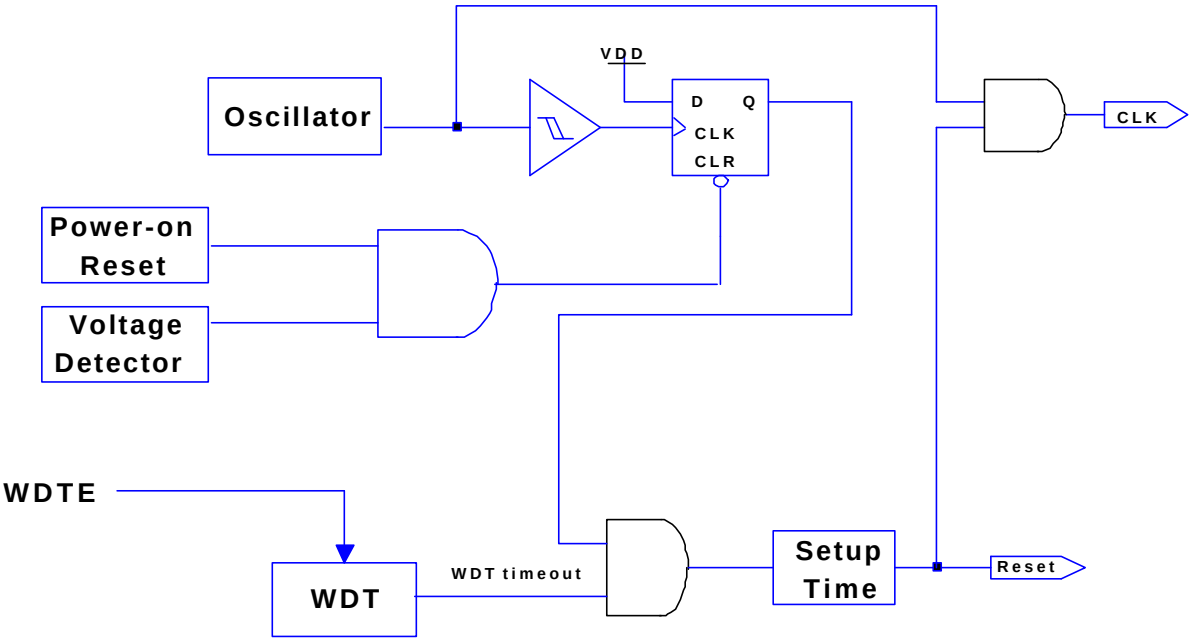


Fig. 8 Block Diagram of Reset of Controller

4.5 Reset and Wake-up

A RESET is initiated by

(1) Power on reset, or

(2) WDT timeout. (if enabled)

The device is kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1" .
- When power is switched on, the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is enabled if Code Option bit ENWDT is "1" .
- The CONT register is set to all "1" except bit 6 (INT flag).
- Bits 3,6 of IOCE register are cleared, bits 0,4~5 of IOCE register are set to "1" .
- Bits 0 of R3F and bits 0 of IOCF registers are cleared.

The sleep mode (power down) is attained by executing the SLEP instruction (designated as SLEEP1 MODE). While entering into sleep mode, the WDT (if enabled) is cleared but keeps on running. The

controller is awakened by WDT timeout (if enabled), and it will cause the controller to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78450 has another sleep mode (caused by clearing "SLPC" bit of IOCE register, designated as SLEEP2 MODE). In the SLEEP2 MODE, the controller can be awakened by-

(a) Any one of the wake-up pins is set to "0." (refer to Figure 9). Upon waking, the controller will continue to execute the program in-line. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, P74~P75, and P90~P91) should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noted is that after waking up, the WDT is enabled if Code Option bit ENWDT is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

(b) WDT time-out (if enabled). On wake-up, will cause the controller to reset.

Table 2 The Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	C87	C86	C85	C84	C83	C82	C81	C80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC9	Bit Name	C97	C96	C95	C94	C93	C92	C91	C90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U

		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	**P	**P	**P	**P	**P	**P	**P	**P
0x03	R3(SR)	Bit Name	GP	PS1	PS0	T	P	Z	DC	C
		Power-On	0	0	0	t	t	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	RSR.1	RSR.0	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5(P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6(P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	R7(P7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x08	R8(P8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x09	R9(P9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x3F	R3F(ISR)	Bit Name	-	-	-	-	-	-	EXIF	TCIF
		Power-On	U	U	U	U	U	U	0	0
		/RESET and WDT	U	U	U	U	U	U	0	0
		Wake-Up from Pin Change	U	U	U	U	U	U	P	P
0x0D	IOCD	Bit Name	S7	-	-	-	/PU9	/PU8	/PU6	/PU5
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	-	ODE	WTE	SLPC	ROC	-	-	/WUE
		Power-On	U	0	1	1	0	U	U	1
		/RESET and WDT	U	0	1	1	0	U	U	1
		Wake-Up from Pin Change	U	P	1	1	P	U	U	P

0x0F	IOCF	Bit Name	-	-	-	-	-	-	EXIE	TCIE
		Power-On	U	U	U	U	U	U	0	0
		/RESET and WDT	U	U	U	U	U	U	0	0
		Wake-Up from Pin Change	U	U	U	U	U	U	P	P
0x0A~0x3E	GPR	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

** To execute the next instruction after the "SLPC" bit status of IOCE register being on high-to-low transition.

X: Not used. U: Unknown or don't care. P: Previous value before reset. t: Check Table VI.6-1

The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events:

1. Power-on condition,
2. Watchdog timer time-out.

The values of T and P, listed in Table 3 are used to check how the processor wakes up.

Table 4 shows the events which may affect the status of T and P .

Table 3 The Values of RST, T and P after RESET

Reset Type	T	P
Power on	1	1
WDT during Operating mode	0	P
WDT wake-up during SLEEP1 mode	0	0
WDT wake-up during SLEEP2 mode	0	P
Wake-Up on pin change during SLEEP2 mode	P	P

*P: Previous status before reset

Table 4 The Status of RST, T and P being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP2 mode	P	P

*P: Previous value before reset

4.6 Interrupt

The EM78450 has the following interrupts.

(1) TCC overflow interrupt

(2) External interrupt (/INT)

R3F is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (if enabled) is generated, it will cause the next instruction to be fetched from address 001H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the R3F register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts. The flag in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI instruction. Note that reading R3F will obtain the output of logic AND of R3F and IOCF (refer to Fig. 9). The RETI instruction exits interrupt routine and enables the global interrupt (ENI instruction execution). When an interrupt is generated by INT instruction (if enabled), it causes the next instruction to be fetched from address 002H.

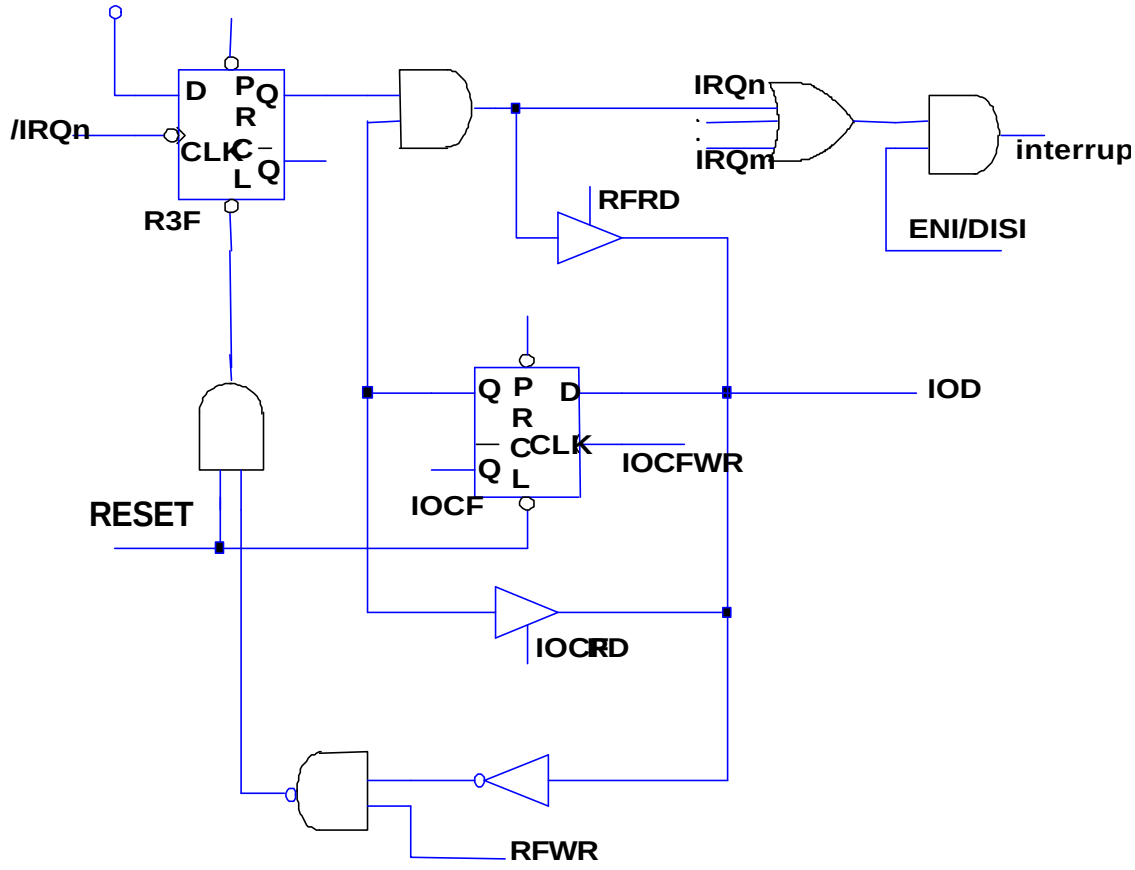


Fig. 9 Interrupt Input Circuit

4.7 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed -

(a) by executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any instruction which writes to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ···×).

(b) if CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) are tested to be true.

In these cases, the execution takes two instruction cycles.

In addition, the instruction set provides the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit designator that selects the value for the bit which is located in the register "R", and affects the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note1> This is applicable to IOC5 ~ IOC9, IOCD~IOCF only

<Note2> This instruction is not recommended for R3F operation.

<Note3> This instruction cannot operate under R3F.

4.8 CODE Option Register

The EM78450 has one CODE option register that is not the part of the normal program memory. The option bits cannot be accessed during normal program execution.

7	6	5	4	3	2	1	0
-	-	RCT	LVDD	HLF	MS	CK2	ENWDT

- Bit 0 (ENWDT): WDT option.

  0 : WDT is always disabled. Control bit WDTE in IOCE is unused.

  1 : WDT is enabled. WDT can be disabled/enabled by software programming. Control bit WDTE in IOCE register is used to disable/enable WDT.
- Bit 1 (CK2): Input clock divided by two selection.

  0 : System clock is from oscillator clock directly.

  1 : System clock is from oscillator clock divided by two.
- Bit 2 (MS): Oscillator type selection.

  0 : RC Type

  1 : XTAL Type
- Bit 3 (HLF): XTAL frequency selection.

  0 : Low frequency, 32.768KHz

  1 : High frequency
- Bit 4 (LVDD): Operating voltage.

  0 : 4V~5.5V

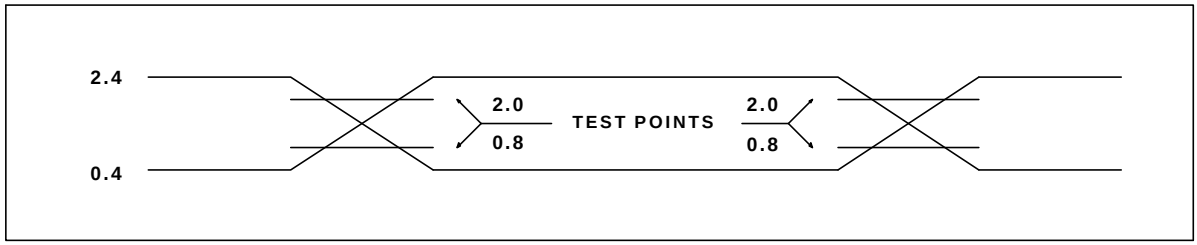
  1 : 2.3V~4V
- Bit 5 (RCT): RC mode selection

  0: Internal C, external R oscillation.

  1: External RC oscillation
- Bit 6~Bit 7 : Not used, must bt "0"s.

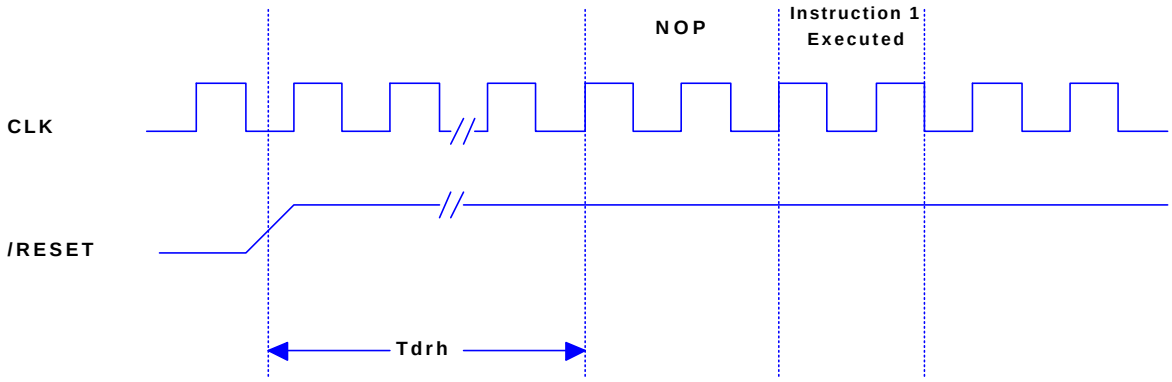
4.9 Timing Diagram

AC Test Input/Output Waveform

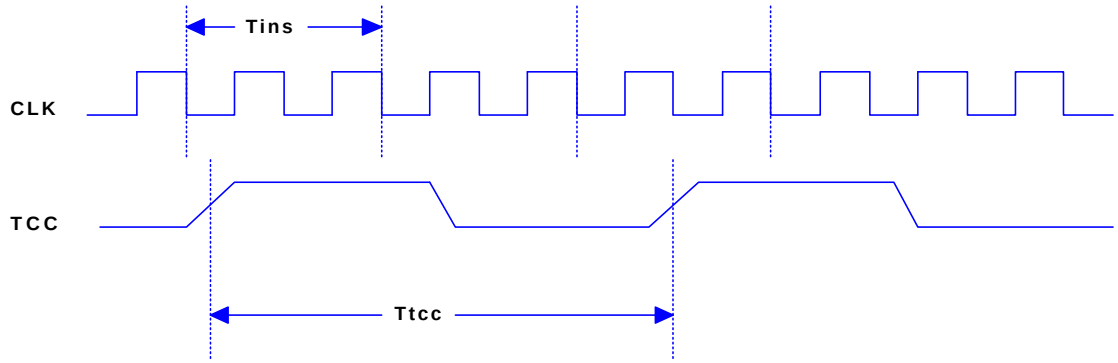


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



5. ABSOLUTE MAXIMUM RATING

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Operating Frequency (2clk)	DC	to	20MHz

6. ELECTRICAL CHARACTERISTICS

6.1 DC Characteristic

(Ta=0°C~70°C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FXT	XTAL VDD to 2.3V	Two clocks	DC		4	MHz
	XTAL VDD to 3V		DC		8	
	XTAL VDD to 5V		DC		20	
FRC	RC VDD to 2.3V	Two clocks	DC		4	MHz
	RC VDD to 3V		DC		4	
	RC VDD to 5V		DC		4	
IIL	Input Leakage Current	VIN = VDD, VSS			±1	µA
VIH1	Input High Voltage VDD=5V)		2.0			V
VIL1	Input Low Voltage (VDD=5V)				0.8	V
VIHX1	Clock Input High Voltage (VDD=5V	OSCI	2.5			V
VILX1	Clock Input Low Voltage (VDD=5V	OSCI			1.0	V
VIH2	Input High Voltage(VDD=3V)		1.5			V
VIL2	Input Low Voltage (VDD=3V)				0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.6	V
VOH1	Output High Voltage (Ports 5,6,8, P74~P77, P90~P92,P95~P97,and PF5~PF7)	IOH = -8.0mA	2.4			V
VOH2	Output High Voltage (P70~P72)	S7=1(IOCD Register bit7), IOH = -7.0mA	2	2.4		V
		S7=0(IOCD Register bit7), IOH = -7.0mA	2.4			
VOH3	Output High Voltage (P93/SDO,P94/SCK)	IOH = -5.0mA	2.4			V
VOL1	Output Low Voltage (Ports 5,6,8, P74~P77, P90~P92,P95~P97,and PF5~PF7))	IOL = 5.0mA			0.4	V
VOL2	Output Low Voltage (P70~P72)	S7=1(IOCD Register bit7), IOH = 10.0mA		0.4	0.8	V
		S7=0(IOCD Register bit7), IOH = 10.0mA			0.4	
VOL3	Output Low Voltage (P93/SDO, P94/SCK)	IOL = 7.0mA			0.4	V
VOL4	Output Low Voltage (P74~P77)	IOL = 15.0mA			0.4	
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	µA

IPH2	Pull-high current (P74,P75)	Pull-high active, input pin at VSS		1		mA
ISB	Power down current	All input and I/O pin at VDD, output pin floating, WDT enabled			10	μA
ICC	Operating supply current	/RESET="High", Fosc=1.84324MHz (CK2="0"), output pin floating			3	mA

6.2 AC Characteristic

(Ta=0°C~70°C, VDD=5V±5%, VSS=0V)

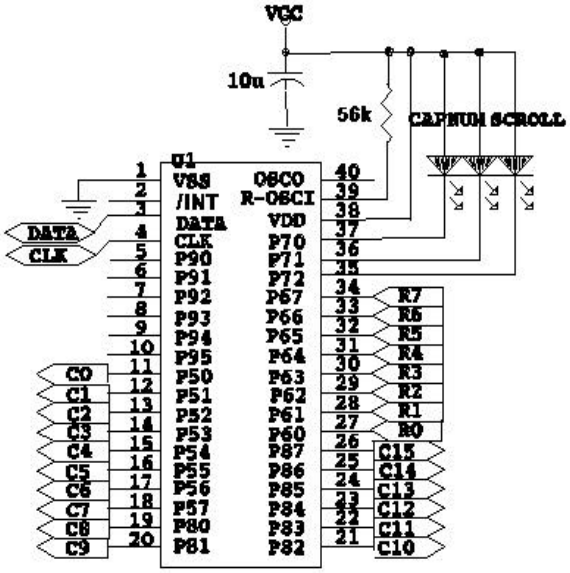
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CK2="0")	RC Type	250		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Twdt	Watchdog timer period	Ta=25°C		18		ms
Tdrh	Device reset hold period	Ta=25°C		18[1]		ms

N= selected prescaler ratio.

[1] NOTE : VDD=5V, setup time period = 16.5ms ± 5%.

VDD=3V, setup time period = 18.0ms ± 5%.

7. APPLICATION CIRCUIT



EM78450

	R0	R1	R2	R3	R4	R5	R6	R7
C0			058				064	
C1		044					057	
C2	110	016	001	002	017	031	046	
C3	045	030	112	003	018	032	047	
C4	115	114	113	004	019	033	048	
C5	035	021	006	005	020	034	049	050
C6	036	022	007	008	023	037	052	051
C7		118	119	010	025	039	054	
C8	116	015	120	121		029	043	061
C9	117	028	013	009	024	038	053	
C10	041	027	012	011	026	040	042	055
C11		092	076	122	091	093	090	084
C12	099	097	075	123	096	098	095	089
C13	104	102	085	086	101	103	100	105
C14	083		080	081	106	108	126	079
C15	060			124	125			062