T-42-31

DESCRIPTION

The ECI Semiconductor EM series has been generated to provide cost and space effective high performance analog system solutions in silicon for your specific application.

The EM family of low-cost 30v Bipolar Gridded Semicustom Arrays is optimized for analog functions. With up to 416 transistors including 90 Schottky transistors in 9 chip sizes increasing progressively from 71 x 59 mils to 178 x 140 mils, most applications can be integrated efficiently with 80 to 90% utilization.

The ECI EM family incorporates many components which are seldom found on other chips. These components include Schottky diodes for biasing and clamping purposes, high value base resistors which are less troublesome to use than implant resistors, high gain vertical PNP transistors, output lateral PNP transistors which are able to saturate without creating large amounts of substrate current and optional trimable thin film resistors for precise matching over temperature.

Biasing Schottky diodes, large-value base resistors and Lateral Output PNP transistors are not found on other chips. High performance vertical PNP transistors are seldom offered on semicustom arrays. Thin-Film resistors and second metal interconnection which are not normally offered can be added to the EM series of arrays without wasting any space for these options.

The EM Series of arrays is very flexible. Design can either be accomplished at the component level resulting in the ultimate in chip performances and silicon utilization, or take advantage of the repeated cell structure to implement macro-functions. The EM series have been designed to have compatible electrical performance with other existing arrays. Most published macro-functions can be easily implemented on the EM Series providing similar performance.

In its simplest form only the metalization layer needs to be customized for each circuit design, linking together the predesigned and preprocessed array of circuit elements in each chip. Thus the development costs and time are only a small fraction of that of a full custom design. The design of your circuit is a straightforward low risk task.

FEATURES

ALTERNATE SOURCES, INDUSTRY STANDARD: EM arrays are compatible with bipolar arrays from Plessey, Exar, Cherry, Microlinear, Analog Devices, and PMI. Second source existing circuits with little or no circuit modification and easy re-layout.

COMPACT: Up to 95 percent silicon utilization with a second metal layer.

VARIETY: Six chip sizes from 59 x 71 sq. mils. to 140 x 178 sq. mils.

WIDE RANGE OF POWER SUPPLIES: All arrays are usable with either split or positive supply(s) from 0.9V to +/-15V.

EXCELLENT MATCHING: All critical components, such as resistors and small transistors have identical size and identical orientation for best matching.

CELLS: Repeated Cell Structure common to all the arrays. Allows transfer of designs between arrays.

CAD AND SOFTWARE: Schematic capture and simulation with CAD tools at both the PC and Workstation levels.

LOW COST/ FAST TURNAROUND: The metalization layer links together the predesigned and preprocessed array of circuit elements in each chip.

SIMPLE LAYOUT: Design and layout is an elementary, low risk task. No special expertise in IC fabrication or device physics is required.

APPLICATIONS: Applications from micropower hearing aids to industrial interfaces and full MIL STD.

UNIQUE COMPONENTS: Large-value base resistors, less troublesome to use than implant resistors.
Thin-Film Resistors, for very accurate matching, low temperature coefficient and ease of trim.
Vertical PNP transistors, with high gain.
Output Lateral PNP transistors, saturate without creating large substrate currents.
Biasing Schottky Diodes to prevent latch-up problems with multiple positive supplies on the chip during power up sequence or supply malfunction.

A P P L I C A T I O N S

* Oscillators
* Power Drivers
* A/D converters
* Voltage Shifters
* Digital Circuits
* Voltage Regulators
* Analog Circuits
* D/A Converter
* Comparators
* Amplifiers
* Counters
* Timers

* Replace Obsolete:
  - Interface Parts
  - Digital Parts
  - Analog Parts
  - 4000 series

COMPONENTS

The Transistors are designed to be used for both analog and digital circuits. Since the EM series arrays use a bipolar technology with sufficient minimum features, input diodes are usually not required for ESD protection. Should your application require it, extra vertical PNP transistors and transistor tubs may be used for extra input protection.

Array Modules:

A repeated cell structure common to all arrays is optimized for analog functions. The core of the chip is a repeated Cell (or Tile) structure which contains 6 small NPN transistors, two, of which incorporate schottky diodes and 4 lateral PNP transistors combined with resistors, crossunders and large value base resistors. Thin-Film resistors and second level of metal interconnection may be added resulting in better performance and higher silicon utilization. All critical components, such as resistors and small transistors have not only identical size but identical orientation for the best possible matching.

Small NPN Transistors:

NPN transistors within each core cell have two bases each containing one emitter site and one collector site with two contacts usable as a low impedance crossunder. The collector structure uses a special deep N+ diffusion also called Sinker which acts as a very effective shield for the two transistor halves. The sinker allows simultaneous independent utilization of the two sections when applicable. The independent utilization of the two sections permits the use of 2X transistors for better current capability, current density noise and/or offset reduction, Darlington connection within a single tub, two-input NOR Gate, temperature-compensated Zener diodes and vertical PNPs which may be combined with NPNs in the same tub, etc... Matching between the two NPN halves is excellent, usually well below 1mV.

150 Milliamp NPN Transistors:

All array peripheral structures one or more large NPN transistor with 12 times the area of a single device. They are constructed with 5 independent bases each containing two emitter sites, thus allowing this single device to have multiple uses including but not limited to Darlington configuration, up to six-input Nor Gates and Zener diode.

Two separate collectors with 6 contacts each provide a low impedance crossunder. As many collectors as required may be paralleled for high current, low saturation applications. This device is an excellent 150mA transistor and may be used up to 200mA in applications where saturation resistance is not critical. The inherent excellent matching of all NPN transistors within the array allows paralleling of as many devices as required for high-current, low-saturation applications.

Lateral PNP transistors:

Lateral PNP transistors are fabricated with a special P+ diffusion in order to enhance their performance compared to regular lateral PNP transistors fabricated with the base diffusion of the NPN transistors. All lateral PNP transistors are provided with two collectors, effectively doubling their utility for current sources, active loads and Gm reduction in Op Amp input stages.

Output Lateral PNP transistors:

Output Lateral PNP transistors are located within the array periphery. The output lateral PNP transistors exhibit high gain and excellent saturation characteristics to collector currents in excess of 2 mA. The output lateral PNP transistors are usable up to 5 mA each and can be easily paralleled to handle more current. Unlike regular lateral PNP transistors, they can be used in saturating output stages without the risk of having large parasitic current flowing vertically from the emitter to the substrate.

Vertical PNP transistors:

Vertical PNP transistors are located under the Bonding Pads and are combined with nitride capacitors. The vertical PNP transistors exhibit very high gain and higher Ft than both the normal and output lateral PNP transistors and are useful up to 10 mA. The vertical PNP transistors are therefore ideally suited for follower-type of complementary output stages, low-current analog input stages for comparators & Op Amps and Low Power TTL-type input stages. Vertical PNPs located in the corners are similar but larger and are therefore useful up to 25 mA each.

Base Diffused Resistors:

400, 800 and 1200 ohm base diffused resistors are in abundance in every array cell. They can be placed in series or parallel and match very closely because of their identical orientation and relatively large width. Any resistor can also be used as a crossunder in non-critical circuit locations when straight metal connections are not practical and dedicated crossunders not available.

Large Value Base Resistors:

The EM series of arrays offer large value base resistors in lieu of implant or pinch base resistors offered in most competitive arrays. These resistors do not have the large spread, large temperature coefficient and breakdown voltage limitations of Pinch resistors. The large value base resistors are also better and less troublesome than implanted resistors and they do not exhibit the large voltage coefficient and MosFet-type modulation which are a designer's nightmare.

Low Impedance Crossunders:

Four different types of dedicated low impedance crossunders are provided in abundance to allow simple and efficient single-metal array utilization:

P+ Bus crossunder-------- 60 ohm
P+ Cell crossunder------- 60 ohm
N+ Peripheral crossunder- 15 ohm
N+ V_{EE} crossunder-------- 30 ohm

Epi Pinch Resistor:

The epi pinch resistor uses the epitaxial layer as the resistive material to generate a compact high-value resistor with quasi-constant current characteristics at high-voltage. The epi pinch resistor is most useful as a start-up resistor for low-current voltage regulators and biasing circuits for micropower applications.

Bonding Pads:

Dedicated Bonding Pads are located within the chip periphery and allow electrical connections for wafer test and packaging purposes. As described above, the bonding pads are combined with vertical PNP transistors and Nitride capacitors. The four corner pads are combined with 25 mA vertical PNP transistors.

Diodes:

Use any NPN or PNP Transistor as a diode by shorting the transistor collector and base to give the forward and reverse characteristic of the transistor emitter-base junction.

Zener Diodes:

The reverse bias characteristics of the emitter-base junction of any NPN transistor has a nominal breakdown voltage of 6.5 volts and may be used as a zener diode. These structures have a low temperature coefficient and good matching.

Schottky Diodes:

The EM series of arrays contains two types of Schottky diodes. The large schottky diodes are useful for biasing-related latch-up prevention.

The small schottky diodes are anti-saturation devices. They are included in some cell and peripheral areas. The small schottky diodes allow easy implementation of relatively fast digital and interface circuitry especially when TTL compatibility is required on some outputs.

Grid Structure:

The EM Series of arrays is fully gridded in a user's CAD sense. All metal tracks and components contacts are on a coarse grid which prevents any metal design rules violation. Forty five degree tracks are allowed to increase routability especially within active components. Users are only required to draw the tracks symbolically in pairs which are automatically processed by the proprietary software. Utilizing the grid structure saves a great deal of time and prevents risky or fatal metal design rule violation in tight areas.

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EM COMPONENTS

	Cluster	EM-21	EM-22	EM-44	EM-64	EM-83	EM-84
Chip Size--mils	18x27	71x59	71x86	107X140	160x140	178x113	178x140
Chip Area	n/a	4189	6106	14980	22400	20114	24920
Array Modules	1	2 x 1	2 x 2	4 x 4	6 x 4	8 x 3	8 x 4
Pads	2	18	22	30	38	50	54
Small NPN (2 Bases)	4	8	16	36	64	96	128
Schottky NPN 1 X	2	12	18	32	50	72	90
150 mA NPN	0	2	4	6	8	6	8
Lateral PNP (2 Collectors)	4	8	16	36	64	96	128
Output Lateral PNP	0	2	4	6	8	6	8
Vertical PNP	0	16	20	28	36	48	52
Transistor Sub total	10	48	78	144	230	324	414
ESD Input Protection	0	8	10	14	18	24	26
Total Active Components	10	56	88	158	248	348	440
Bus Crossunders	5	22	34	66	108	166	208
Cell Crossunders	8	24	48	96	160	216	288
Peripheral Crossunders	0	12	14	20	26	40	42
Vee Peripheral Crossunders	0	8	10	14	18	24	26
Base Resistor 400 ohms	12	36	72	144	240	324	432
Base Resistor 800 ohms	26	87	156	313	522	753	978
Base Resistor 1200 ohms	10	39	60	121	202	321	402
Subtotal Base R Kohm	38	131	226	453	756	1,117	1,438
8 K Large Base Resistor	4	12	20	40	68	100	132
Large Base Resistor Kohms	32	96	160	320	544	800	1056
Total Resistance Kohm	70	227	386	773	1,300	1,917	2,494

DESIGN SUPPORT

The senior designers at ECI are within easy reach to support you and your program. To begin the process just deliver your schematic and input-output requirements to ECI. We will design a chip to your written specifications and send you working prototypes normally within five weeks.

You may choose to design your own IC using ECI's full color software for your AT, 286, or 386 Personal Computer. The ECI design tools require only a minimum knowledge of bipolar characteristics. Autorouting and autoplacing are not necessary with these small EM chips. The ECI user friendly software is easy to learn and will bring you to finished design in record time. You will maintain full control of your integrated circuit while minimizing the non-recurring engineering costs. When your design is complete, just transmit it to us by Modem or mail your Floppy Disk.

ECI can supply a GDSII database with your existing design system or can provide layout sheets for hand routing.

DESIGN

If you elect to design your IC just follow these steps:

A. Send away for your floppy disk which contains

   1. Spice models for all components,

   2. Proprietary library symbols for schematic entry purposes.

   3. Proprietary Spice pre-processor.

      Note that both the library of symbols and the Spice pre-processor are exclusively designed for OrCad schematic entry software package. The OrCad schematic entry software package may be acquired separately or rented from ECI for the duration of the design along with P-Spice electrical simulator, Probe Spice graphic post-processor and the rest of the proprietary software necessary to perform Layout and Design verification on a PC. Should you desire to not use OrCad, you may create your own Spice input file calling the provided models.

B. Obtain a copy of ECI Semiconductor's Design Handbook.

C. Use P-Spice or an equivalent program with graphic post-processor to design your circuit and optimize it until you are completely satisfied. Do not forget to check circuit performance at temperature extremes within the specified range of power supply voltages. Monitor component stability, sensitivity and identify critical paths.

LAYOUT

A. Layout Generation

There are four options to generate the layout.

1. Let the ECI team perform the layout.

2. Request layout sheets to generate a pencil layout.

3. Request a GDSII data-base to layout the IC on a workstation or any suitable IC design system.

4. Buy or rent our proprietary software package which is totally integrated and is user friendly.

B. Layout Verification

Layout Versus Schematic (LVS) verification is mandatory to ensure conformity between layout and electrical schematic which is key to error-free design. True LVS can be performed by proprietary software provided that the electrical schematic is captured on OrCad in either a straight or a hierarchical way using exclusively the furnished EM library of symbols. LVS cannot be performed with any other form of schematic since the supplied OrCad symbols contain hidden substrate-related connections and parasitic components necessary for the LVS.
You may elect to execute the LVS provided that you have the proprietary software. ECI does not recommend performing a manual LVS because of the very likely chance of a layout error especially if thin-film resistors and/or second level of metal interconnection options are used.

BREADBOARDING

Integrated devices differ from discrete devices in two respects. Each component is surrounded by a junction, which can lead to stray effects. All regions and their contacts must be on one surface, which makes some parameters different.

It is therefore important to verify your design. You may verify your design with breadboarding and computer simulation. It is important to perform both verifications. A set of kit parts are available from ECI. These are the actual devices on the chip in dual-in-line packages, wired up individually for your use.

DESIGN EXAMPLES

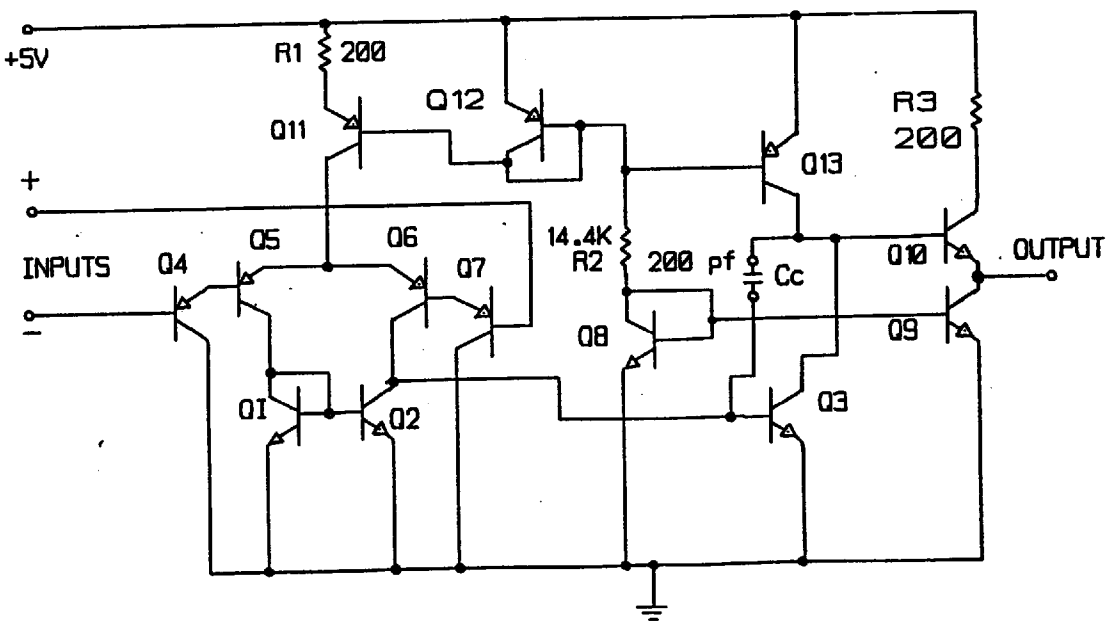
The following are examples of various circuits that can easily be laid out on this array. They are meant to provide illustrations of the many different circuit combinations that may be accommodated. These samples may be used as a guideline for your circuit development.

SINGLE SUPPLY OPERATIONAL AMPLIFIER

This circuit operates with input voltages down to ground level. Current source Q7 provides a 100 uA bias to the Darlington PNP input stage. Q1 and Q2 are the active load for the Darlington stage which gives very high gain. Q4 acts as an emitter follower and is used to increase the current source drive capability which is limited by the output resistor R4.

Key Specifications:

Power supply:	2.5 V to 25 volts
Input Current:	1 uA
Open Loop Gain:	80 dB
Unity Gain Bandwidth:	250 KHz @5V Vcc.
Input Current:	1 uA



CURRENT OUTPUT OPERATIONAL AMPLIFIER

The gain of the first stage is controlled by the ratio of the collector load resistance R1 and emitter resistance R6. The high input impedance is provided by the Darlington stage Q1 and Q2. Q10 biases the Darlington stage. Q12 and its associated resistors, R3, R11, and R13 generate the current for the Darlington stage. Q3 and Q4 are the input signal differential pair. The circuit may be used as a current amplifier or a voltage amplifier by feeding the output into a resistor.

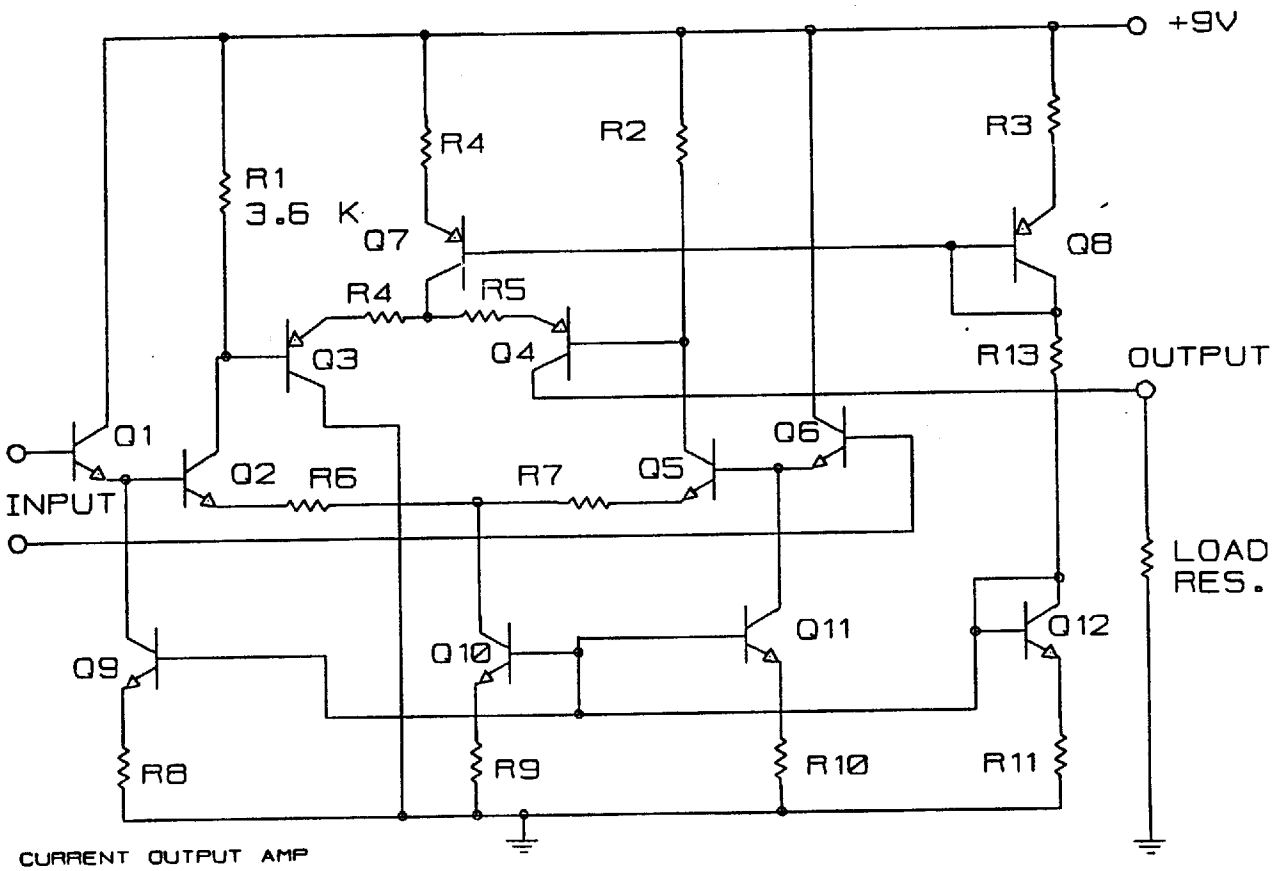
Key specifications are:

Input Current: 1 uA maximum

Gain: 19uA/mV (1 mV input change produces a 19 uA output variation)

3Db Response: 50KHz

Distortion: Less than 1 percent



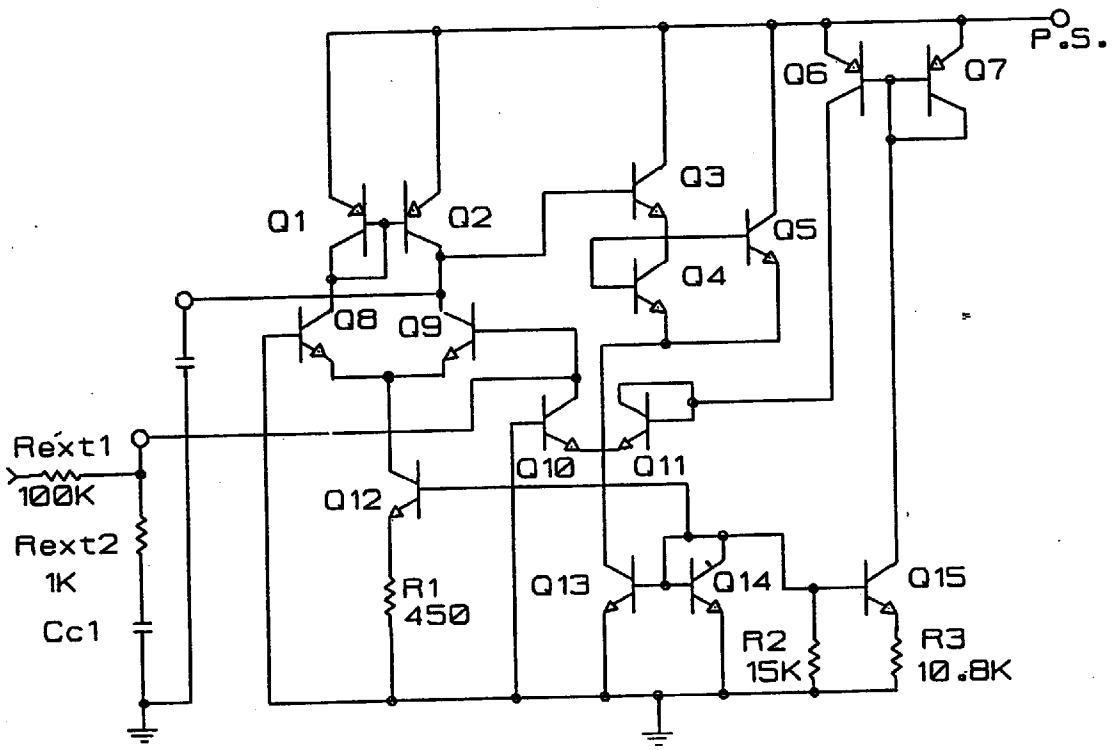
CURRENT OUTPUT AMP

LOGARITHMIC AMPLIFIER

Q10 performs the basic logarithmic function. Q10 converts the input voltage into a current and sums it with the input signal. Q8 and Q9 are the differential amplifier in the primary gain stage with the load Q10. The buffer is composed of Q2, Q3, Q4, and Q5. Temperature compensation is provided by Q3, Q6, Q11, and Q15.

An input voltage of 1 to 32 volts develops a 0 to 90 millivolt logarithmic output with an 80 microvolt offset. The circuit has an accuracy of approximately one percent. Maximum frequency of operation is 1 MHz.

$V_o = (kT/q) \ln [V_{IN}/(Rext1)(Ir)]$

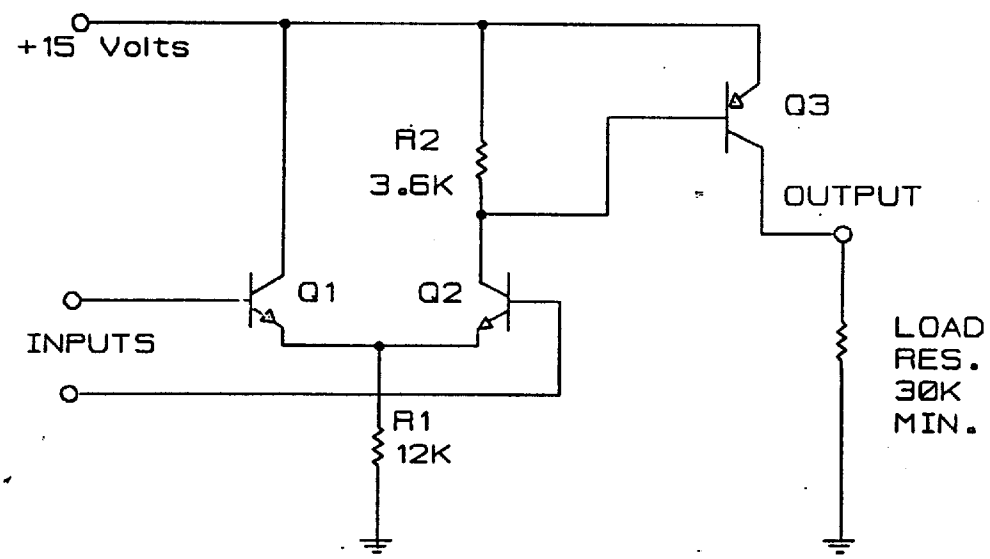


COMPARATOR

This simple comparator is extremely useful when comparison of two inputs is very unsophisticated and great accuracy is not required. Q1 and Q2 act as a differential pair. When the base of Q1 is at a higher voltage than Q2, Q1 is turned on causing Q2 to saturate.

KEY SPECIFICATIONS

Power Supply:	15 Volts
Input Current:	10uA Maximum.
Output Current Source:	500 uA Maximum.
Input indecision:	+/-50 mV
Common Mode Range	3 to 12 volts
Propagation delay:	120 ns.



COMPARATOR

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1.25 VOLT BANDGAP REFERENCE

A temperature stable 1.25 volt output is produced from a supply voltage as low as 1.4 volts. Input differental pair Q7 and Q8 provides equal voltages at the junction of R5 and R6 and the emitter of Q4. Q4 operates at eight times the current density of Q5 because equal voltages appear across R3 and R6. VbeQ4 - VbeQ5, the positive temperature coefficient voltage appears across R5. It is amplified by R6 and R4 and added to VbeQ5 to produce a temperature stable bandgap voltage at V0. Reference start up is provided by Diode Q13. Q1,Q2,Q3 set the currents in Q6 and Q12 at VbeQ3/16.2K.

SPECIFICATIONS

Input voltage:	1.5 volts
Supply current:	160 uA
Power Supply Rejection:	55 dB
Load:	10 uA
Output temp. coef.:	100 ppm max.

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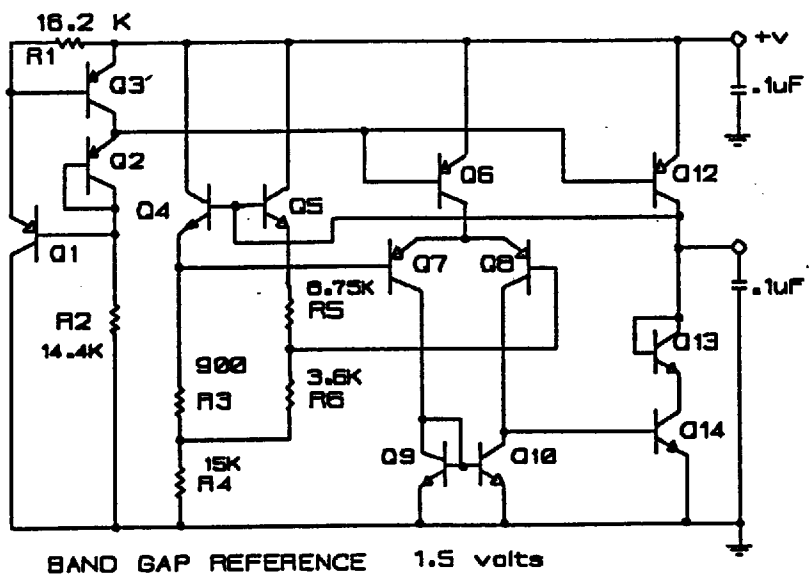


BAND GAP REFERENCE 1.5 volts

VOLTAGE TO CURRENT CONVERTER
(Current Source)

The voltage across the external current setting resistor is identical to the input voltage at the feedback loop through Q7 (except for the V_{BE} difference from V1 and V2). The collector at Q5 feeds Q6 allows the same current to flow in Q3 providing a base current for Q7.

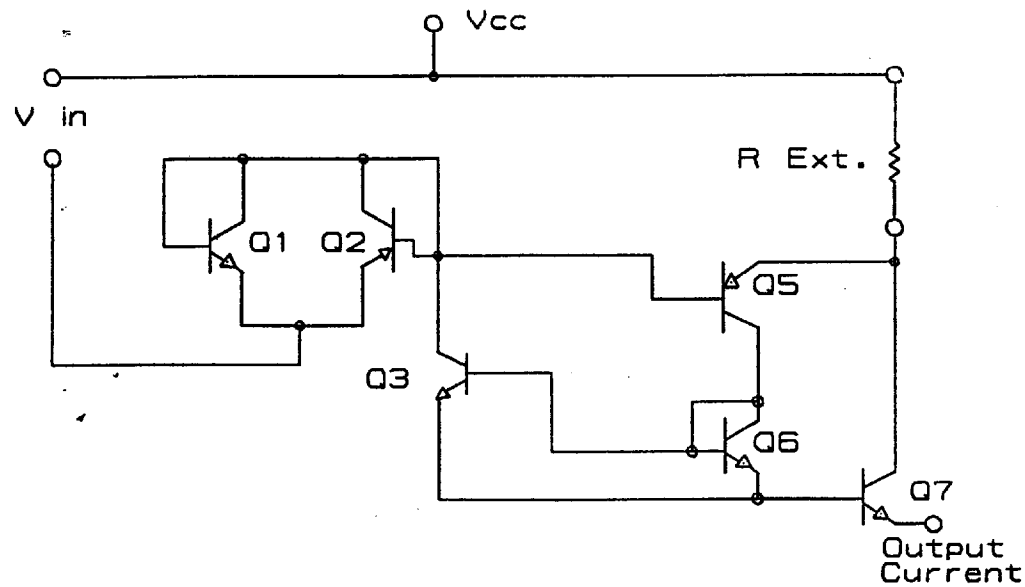
Q1 creates an initial current source for start up. The beginning input voltage should be a minimum of 1.5 volts to allow Q1 to be forward biased.

The voltage level into which the current source must be kept constant to avoid spikes at the current settling resistor.

Specifications;

The base current of Q7 introduces an error of 0.6% maximum.

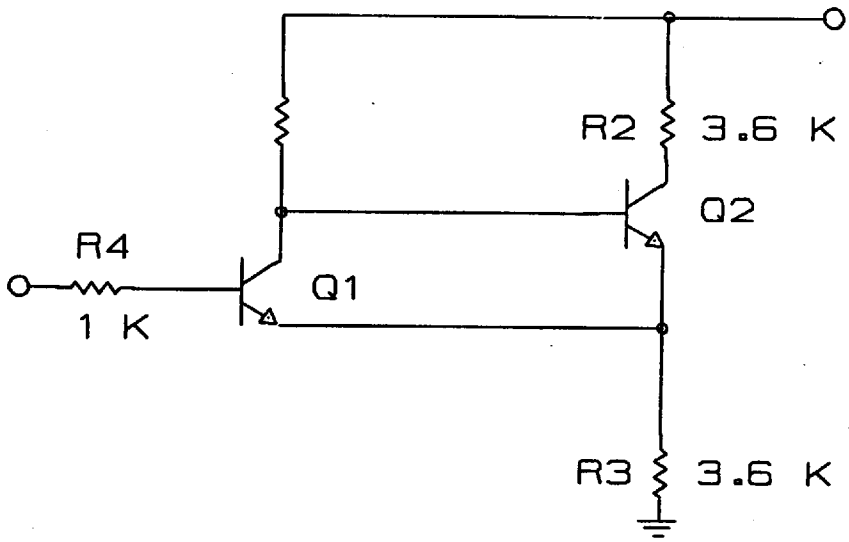
Temperature Coefficient:	40 ppm/C
Current Range:	1uA to 5mA
Supply Voltage Range:	4V to 25V
Linearity:	0.1%



VOLTAGE TO CURRENT CONVERTER (CURRENT SOURCE)

SCHMITT TRIGGER

This is the simple two transistor Schmitt trigger. With the input voltage below the switching thresholds current from R1 saturates Q2 causing a high input threshold. With the input signal above both thresholds Q2 is open causing a low input threshold voltage. Switching delay is about 100 ns.



SCHMITT TRIGGER

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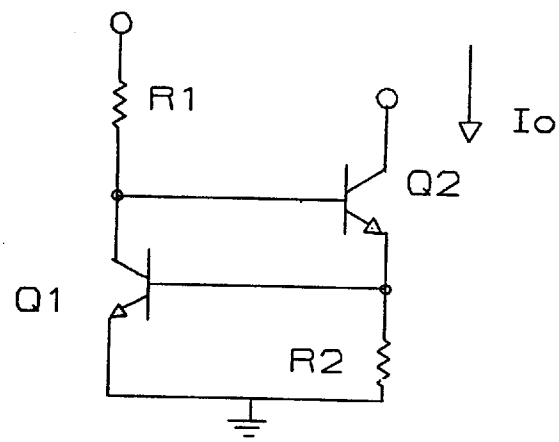
POWER SUPPLY INDEPENDENT CURRENT SOURCE

This current source provides a bias current which is substantially independent of the supply voltage. The output current is a function of beQ1/R2. Since Vbe of Q1 is relatively stable with fluctuations of power supply voltage the current also remains stable.



CURRENT SOURCE

POWER SUPPLY INDEPENDENT