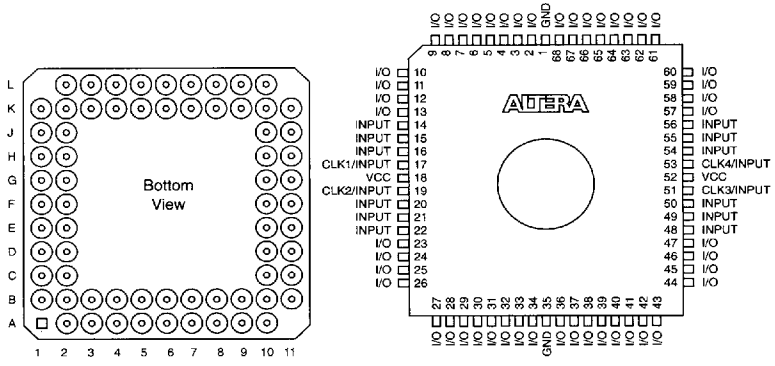
Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 20 ns
  - Counter frequencies of up to 50 MHz
  - Pipelined data rates of up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- The following devices are pin-, function-, and programming file-compatible: EP1810, EP1810T, and EP1810 MIL-STD-883-compliant
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 15):
  - Pin-grid array package (ceramic PGA only)
  - J-lead chip carrier (JLCC and PLCC)

Figure 15. EP1810 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 5 in this data sheet for PGA package pin-out information. Windows in ceramic packages only.



68-Pin PGA

EP1810
EP1810 MIL-STD-883-Compliant

68-Pin J-Lead

EP1810
EP1810T

8 Classic

Table 4 summarizes EP1810 device features.

Table 4. EP1810 Device Features

Feature	EP1810	EP1810T	EP1810 MIL-STD-883-Compliant
t_{PD}	20 ns	20 ns	45 ns
Counter frequency	50 MHz	50 MHz	22.2 MHz
Pipeline data rates	62.5 MHz	62.5 MHz	33.3 MHz
Packages	68-pin PGA 68-pin JLCC 68-pin PLCC	68-pin PLCC	68-pin PGA

General Description

The Altera EP1810 EPLD offers LSI density, TTL-equivalent speed, and low power consumption. The EP1810 has 48 macrocells, 16 dedicated input pins, and 48 I/O pins (see Figure 16). The EP1810 is divided into four quadrants, each containing 12 macrocells. Of the twelve macrocells in each quadrant, 8 have quadrant feedback and are "local" macrocells (see "Feedback Selection" on page 340 of this data sheet for more information). The remaining 4 macrocells in the quadrant are "global" macrocells. Both local and global macrocells can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

The EP1810 also has four dedicated inputs (one in each quadrant) that can be used as quadrant Clock inputs. If the dedicated input is used as a Clock pin, the input feeds the Clock input of all registers in that particular quadrant.

Figure 16. EP1810 Block Diagram

Numbers in parentheses are for J-lead packages. Numbers without parentheses are for PGA packages.

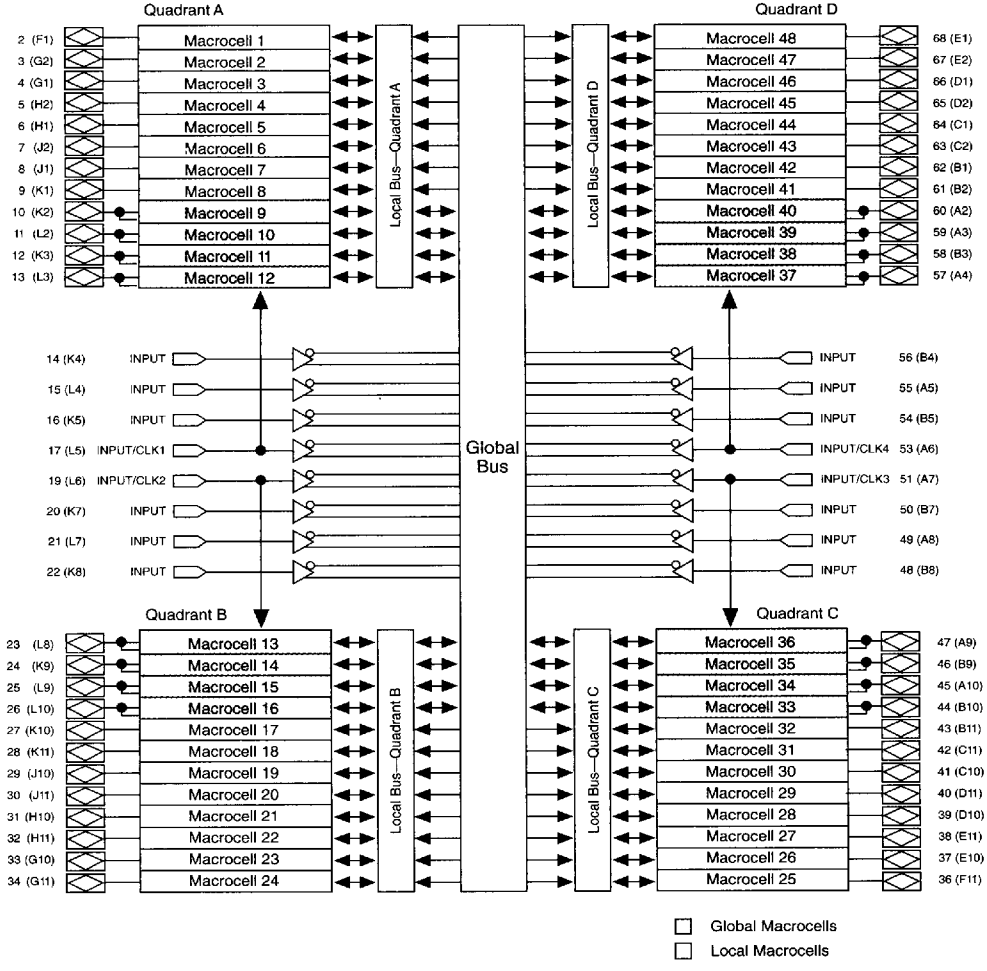
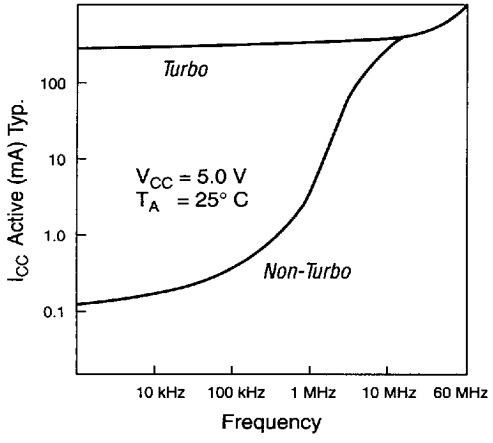


Figure 17 shows the typical supply current (I_{CC}) versus frequency for the EP1810 EPLDs.

Figure 17. EP1810 I_{CC} vs. Frequency

EP1810 & EP1810 MIL-STD-883B-Compliant EPLDs



EP1810T EPLDs

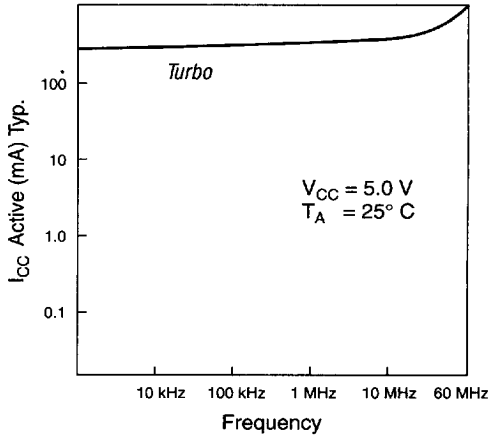
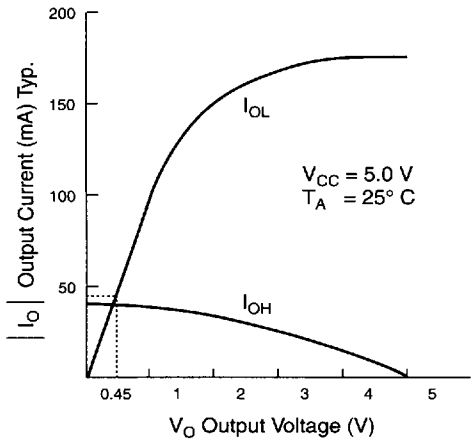


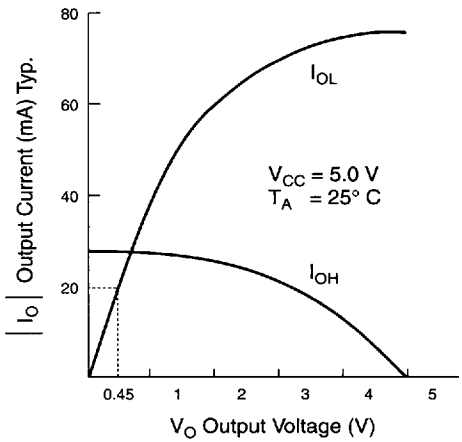
Figure 18 shows the output drive characteristics of EP1810 I/O pins.

Figure 18. EP1810 Output Drive Characteristics

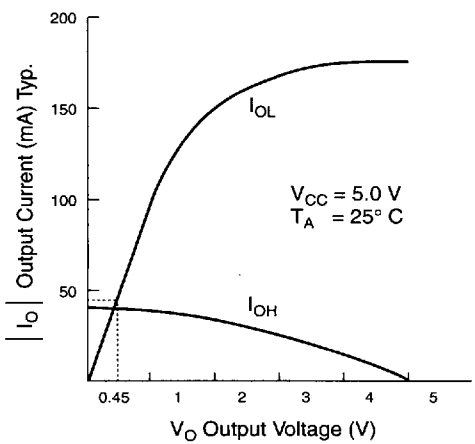
EP1810-20 & EP1810-25 EPLDs
(Including MIL-STD-883-Compliant Versions)



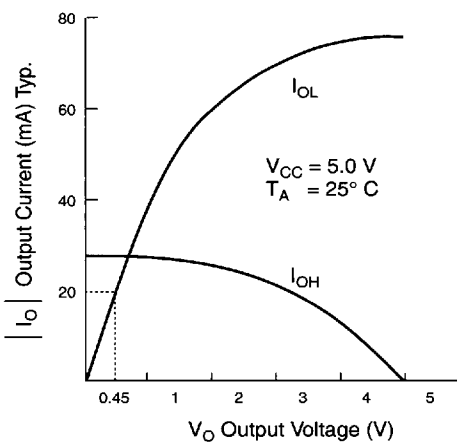
EP1810-35 & EP1810-45 EPLDs
(Including MIL-STD-883-Compliant Versions)



EP1810-20T & EP1810-25T EPLDs



EP1810-35T EPLDs



8 Classic

Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Notes (2), (3)*	–2.0 (–0.5)	7.0	V
V_I	DC input voltage		–2.0 (–0.5)	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300 (–400)	300 (400)	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1,500 (2,000)	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65 (–55)	135 (125)	° C
T_J	Junction temperature	Under bias		(150)	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (2), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (5)*		50	ns
t_F	Input fall time	*Note (5)*		50	ns

DC Operating Conditions *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (8)*	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10		10	µA

Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

I_{CC} Supply Current *Notes (2), (6), (7)*

				EP1810			EP1810T			EP1810 MIL-STD-883-Compliant			
Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, I/O = 0, *Notes (10), (11)*	-20, -25		50	150						900	µA
			-35, -45		35	150							µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (2), (10), (11), (12)*	-20, -25		20	40						40	mA
			-35, -45		10	30 (40)							mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (2), (10), (12)*	-20, -25		180	225 (250)		180	250			240	mA
			-35, -45		100	180 (240)		120	215				mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20T and EP1810-25T devices: maximum V_{PP} is 14.0 V.
(4) Maximum V_{CC} rise time is 50 ms.
(5) For EP1810 Clocks: t_R and t_F = 100 ns (50 ns for military and industrial temperature versions). For EP1810-20T and EP1810-25T Clocks: t_R and t_F = 20 ns.
(6) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(7) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(8) Tested at 25° C and 125° C only.
(9) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 19 has a maximum capacitance of 160 pF.
(10) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.
(11) Tested at 25° C only.
(12) Tested with non-output loading using a data pattern specified by Altera. Data path is correlated to four 12-bit counters.

AC Operating Conditions: EP1810-20 & EP1810-25 *Note (1)*

External Timing Parameters			EP1810-20 EP1810-20T		EP1810-25 EP1810-25T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Maximum internal frequency	*Note (3)*	50		40		0	MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	62.5		50		0	MHz

Internal Timing Parameters			EP1810-20 EP1810-20T		EP1810-25 EP1810-25T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (4)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		8		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

AC Operating Conditions: EP1810-35 & EP1810-45 *Note (1)*

External Timing Parameters			EP1810-35 EP1810-35T		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		35		45	30	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		50	30	ns
t_{SU}	Global clock setup time		25		30		30	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20		25	0	ns
t_{CH}	Global clock high time		12		15		0	ns
t_{CL}	Global clock low time		12		15		0	ns
t_{ASU}	Array clock setup time		10		11		30	ns
t_{AH}	Array clock hold time		15		18		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35		45	30	ns
t_{CNT}	Minimum global clock period			35		45	0	ns
f_{CNT}	Maximum internal frequency	*Note (3)*	28.6		22.2		0	MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	40		33.3		0	MHz

Internal Timing Parameters			EP1810-35 EP1810-35T		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{IN}	Input pad and buffer delay			7		6	0	ns
t_{IO}	I/O input pad and buffer delay			5		5	0	ns
t_{LAD}	Logic array delay			19		28	30	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9		11	0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		9		11	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (5)*		9		11	0	ns
t_{SU}	Register setup time		10		10		0	ns
t_{H}	Register hold time		15		18		0	ns
t_{IC}	Array clock delay			19		28	30	ns
t_{ICS}	Global clock delay			4		8	0	ns
t_{FD}	Feedback delay			6		7	–30	ns
t_{CLR}	Register clear time			24		32	30	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.
$V_{CC} = 5\ V \pm 10\%$, $T_C = -55°\ C$ to $125°\ C$ for military use.

(2) See "Turbo Bit" on page 336 of this data sheet.

(3) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

AC Operating Conditions: EP1810 MIL-STD-883-Compliant *Note (1)*

External Timing Parameters					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF, *Notes (2), (3)*		45	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF, *Notes (2), (3)*		55	ns
t_{SU}	Global clock setup time	*Notes (2), (3)*	30		ns
t_{H}	Global clock hold time	*Note (4)*	0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF, *Note (3)*		25	ns
t_{CH}	Global clock high time		15		ns
t_{CL}	Global clock low time		15		ns
t_{ASU}	Array clock setup time	*Notes (2), (3)*	13		ns
t_{AH}	Array clock hold time	*Notes (2), (3)*	18		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF, *Notes (2), (3)*		50	ns
t_{CNT}	Minimum global clock period	*Note (3)*		45	ns
f_{CNT}	Maximum internal frequency	*Note (5)*	22.2		MHz
f_{MAX}	Maximum clock frequency	*Notes (2), (3), (6), (7)*	33.3		MHz
t_{PZX}	Input to output enable	*Notes (2), (3)*		45	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Notes (2), (3), (8), (9)*		45	ns

Notes:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: $V_{CC} = 5\ V \pm 10\%$, $T_C = -55°\ C$ to $125°\ C$.

(2) All array-dependent delays are specified for an XOR pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM pull-down. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an XOR-like pattern in which only one pure input switches at a time.

(3) When the Turbo Bit is not set (non-turbo mode), a non-turbo adder of 30 ns maximum (40 ns for t_{ASU}) is applied. Parameters cannot be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.

(4) Tested with non-output loading using a data pattern specified by Altera. Data path is correlated to four 12-bit counters.

(5) Not tested directly, but guaranteed by testing t_{CNT} or t_{ACNT}.

(6) The f_{MAX} values represent the highest frequency for pipelined data.

(7) Not tested directly, but derived from t_{SU}.

(8) May not be tested, but is guaranteed to the limits specified in the table under "Absolute Maximum Ratings."

(9) Sample tested only for an output change of 500 mV.

Pin-Out Information

Table 5 provides pin-out information for EP1810 devices in the PGA package.

Table 5. EP1810 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O