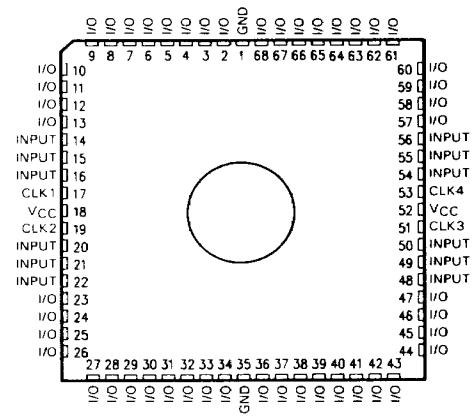
- **Erasable, User-Configurable LSI Circuit Capable of Implementing 2100 Equivalent Gates of Conventional and Custom Logic**
- **Speed Equivalent to 74LS TTL with 33-MHz Clock Rates**
- **Virtually Zero Standby Power . . . 35 μA Typ**
- **Active Power of 250 mW at 5 MHz**
- **Programmable Clock Option Allows Independent Clocking of All Registers**
- **Forty-eight Macrocells with Configurable I/O Architecture Allowing Up to 64 Inputs or 48 Outputs**
- **Accepts TTL SSI and MSI Based Macrofunction Design Inputs**
- **TTL/CMOS I/O Compatibility**
- **100% Generically Testable – Provides 100% Programming Yield**
- **CAD Support from the TI EPLD Development System Featuring Schematic Capture Design Entry with Extensive Primitive and Macrofunction Libraries**
- **Packaged in a 68-Pin J-Leaded, Ceramic (with Window) and Plastic (One-Time Programmable) Chip Carrier**

CHIP-CARRIER PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE	
		CERAMIC CHIP CARRIER (CLCC)	PLASTIC CHIP CARRIER (PLCC)
0°C to 70°C	35 ns	EP1810JC-35	EP1810LC-35
	45 ns	EP1810JC-45	EP1810LC-45
−40°C to 85°C	45 ns	EP1810JI-45	EP1810LI-45

description

The EP1810 series of CMOS EPLDs from Texas Instruments offer LSI density, TTL equivalent speed performance and low power consumption. Each device is capable of implementing over 2100 equivalent gates of SSI, MSI and custom logic circuits. The EP1810 series is packaged as a 68-Pin J-Leaded Chip Carrier, and is available in ceramic (erasable) and plastic (one-time programmable) versions.

The EP1810 series is designed as an LSI replacement for traditional low-power Schottky TTL logic circuits. Its speed and density also make it suitable for high-performance complex functions such as dedicated peripheral controllers and intelligent support chips. Integrated-circuit count and power requirements can be reduced by several orders of magnitude allowing similar reduction in total size and cost of the system, with significantly enhanced reliability.

The EP1810 architecture has been configured to facilitate design with conventional TTL SSI and MSI building blocks as well as simple, optimized gate and flip-flop elements. Schematic descriptions of these functions are stored in a library. The desired TTL logic functions are selected and interconnected "on-screen" with a low-cost personal-computer based workstation. The design processor within the TI EPLD Development System then automatically places the functions in appropriate locations within the EPLD's internal structure. Included in the Development System is EPLD programming hardware and software. The TI EPLD Development System is available for the personal computer.

The EP1810 uses a 1.2 µm CMOS EPROM technoloy employing EPROM transistors to configure logic connections. User defined logic functions are constructed by selectively programming EPROM cells within the device. The EPROM technology also allows 100% generic testing (all devices are 100% tested at the factory). The devices can be erased with ultraviolet light. Design changes are no longer costly or time consuming.

functional description

The EP1810 series of Erasable Programmable Logic Devices (EPLDs) use CMOS EPROM cells to configure logic functions within the device. The EP1810 architecture is 100% user configurable, allowing the device to accommodate a variety of independent logic functions. Externally, the EP1810 provides 16 dedicated data inputs, four of which may be used as system clock inputs. There are 48 I/O pins, which may be individually configured for input, output, or bidirectional data flow.

macrocells

Internally, the EP1810 architecture consists of a series of macrocells. All logic is implemented within these cells. Each macrocell, shown in Figure 1, contains three basic elements: a logic array, a selectable register element, and 3-state I/O buffer (see Figure 1). All combinational logic such as exclusive-OR, NAND, NOR, AND, OR and invert gates are implemented within the logic array. For register applications, each macrocell provides one of 4 possible flip-flop options: D,T,JK,SR. Each EP1810 macrocell is equivalent to over 40 2-input NAND gates.

The EP1810 is partitioned into four identical quadrants. Each quadrant contains 12 macrocells. Input signals into the macrocells come from the EP1810 internal bus structures. Macrocell outputs may drive the EP1810 external pins as well as the internal buses. Figure 2 illustrates a simple logic function that can be implemented within a single macrocell. Note that all combinational logic is implemented within the logic array, a JK flip-flop is selected, and the 3-state buffer is permanently enabled.

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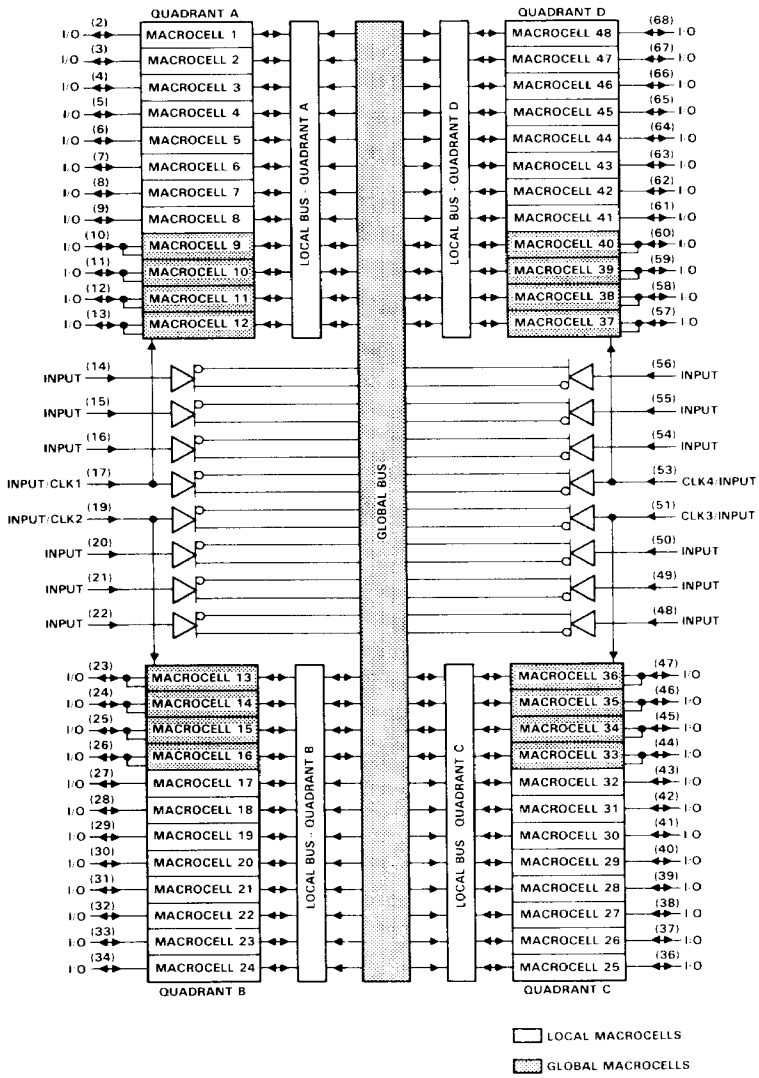
functional block diagram



Each EP1810 macrocell consists of 3 basic components (see Figure 1):

1. A logic array for gated logic.
2. A flip-flop for data storage (selectable options include D, T, JK, and SR). The flip-flop may be bypassed for purely combinational functions.
3. A 3-state I/O buffer to define input, output, or bidirectional data flow.

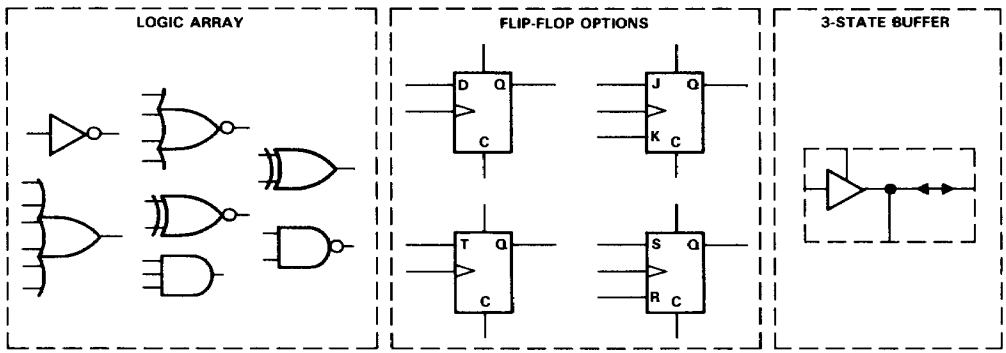


FIGURE 1. MACROCELL COMPONENTS

Typical logic functional implemented into a single macrocell. Each EP1810 macrocell can accommodate the equivalent of 40 gates.

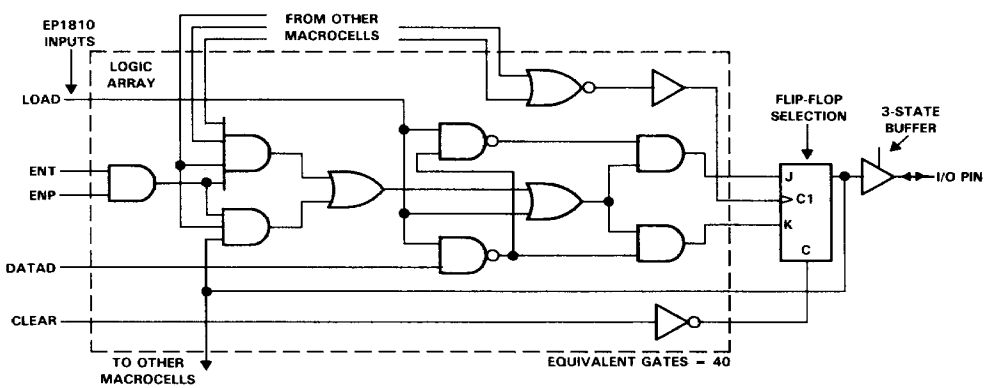


FIGURE 2. SAMPLE CIRCUIT

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The EP1810 macrocell architecture is shown in Figures 3 and 4. There are 32 macrocells called local macrocells. These macrocells offer a multiplexed feedback path (pin or internal) which drives the local bus of the respective quadrant.

There are another 16 macrocells known as the global macrocells (see Figure 4). These global macrocells have features that allow each macrocell to implement buried logic functions and, at the same time, serve as dedicated input pins. Thus, the EP1810 may have an additional 16 input pins giving a total of 32 inputs. The global macrocells have the same timing characteristics as the local macrocells.

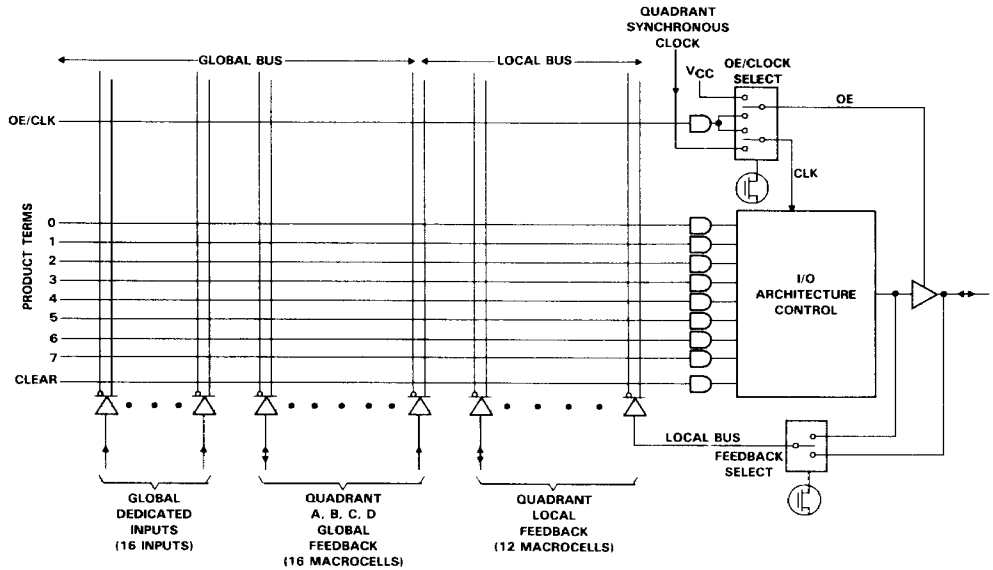

FIGURE 3. LOCAL MACROCELL LOGIC ARRAY

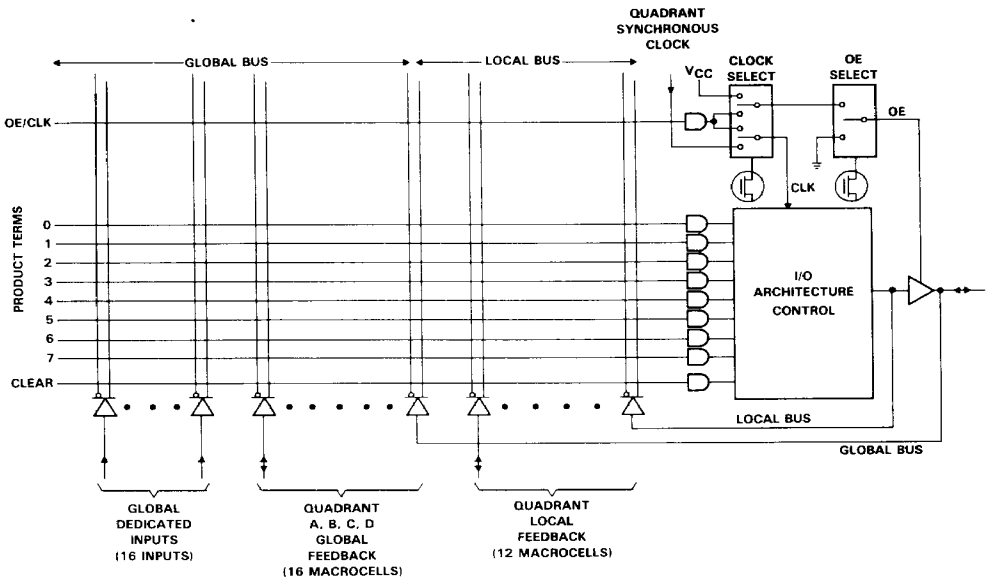

FIGURE 4. GLOBAL MACROCELL LOGIC ARRAY

clock options

Each of the EP1810 internal flip-flops may be clocked independently or in user defined groups. Any input or internal logic function may be used as a clock. These clock signals are activated by driving the flip-flop clock input with a clock buffer (CLKB) primitive. In this mode, the flip-flops can be configured for positive or negative edge triggered operation.

Four dedicated system clocks (CLK1-CLK4) also provide clock signals to the flip-flops. System clocks are connected directly from the EP1810 external pins. With this direct connection, system clocks give enhanced clock to output delay times than internally operated clock signals. There is one system clock per EP1810 quadrant. When using system clocks, the flip-flops are positive edge triggered (data transitions occur on the rising edge of the clock).

macrofunctions

The macrofunctions shown in Figure 5 allow the circuit designer to use popular TTL SSI and MSI building blocks. Many macrofunctions are standard TTL circuits such as counters, comparators, multiplexers, decoders, shift registers, etc. and are identified by their familiar TTL part numbers. Macrofunctions are constructed by combining one or more macrocells. These high-level function blocks may be combined with low-level gate and flip-flop elements to produce a complete logic design.

An automatic function built into the TI EPLD Development System ensures that the use of macrofunctions causes no loss of design efficiency. The development system analyzes the complete logic schematic and automatically removes unused gates and flip-flops from any macrofunction employed. This MacroMunching™ process allows the logic designer to employ macrofunctions without the problems of optimizing their use.

MacroMunching is a trademark of ALTERA Corporation.

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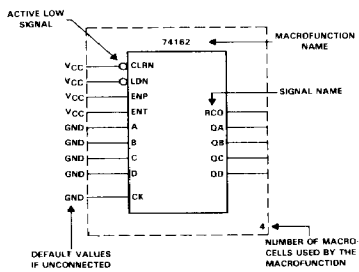
All inputs to macrofunctions are designed with intelligent-default input signal levels (V_{CC} or GND). Normally active high and low signals or unused inputs can simply be left unconnected, further improving productivity and reducing the burden placed on the designer.

Macrofunctions are TTL compatible SSI and MSI circuits giving the circuit designer a high-level approach to EPLD design. Macrofunctions include input default values to unconnected inputs and MacroMunching™ to unused outputs. The macrofunction library consists of over 100 components.



74162 FUNCTION TABLE

INPUTS									OUTPUTS				
CK	LDN	CLRN	ENP	ENT	D	C	B	A	Q_D	Q_C	Q_B	Q_A	RCO
↑	X	L	X	X					L	L	L	L	L
↑	L	H	X	X	d	c	b	a	d	c	b	a	L
↑	H	H	X	L					HOLD COUNT				L
↑	H	H	L	X					HOLD COUNT				L
↑	H	H	H	H					COUNT UP				L
↑	H	H	H	H					H	L	L	H	H

H = high level (steady state)
L = low level (steady state)
X = don't care (any input including transitions)
↑ = transition from low to high level
a,b,c,d = level of steady state input at inputs A,B,C,D

FIGURE 5. MACROFUNCTION SYMBOL

design libraries

Texas Instruments provides both primitive and macrofunction libraries within the EPLD Development System. These libraries are used with the LogiCaps™ schematic capture design entry to specify the logic. Elements from both libraries may be used in the same design, allowing full utilization of the EP1810 resources.

primitive library

The primitive library consists of 80 low-level logic gates, flip-flop, and I/O symbols. See section on primitive library in the A+PLUS™ reference guide. Basic gates provided are AND, OR, NAND, NOR, Exclusive OR and NOR, and NOT functions. De-Morgan's inversion (bubble input) of each gate is included. These logic gates have a maximum of 12 inputs. Larger gates may be constructed by chaining primitives together. Flip-flops in the form of D,T,JK and SR types are supplied. Each flip-flop has asynchronous clear capability. To connect signals to external pins, input and 3-state I/O buffers are available. For the designer's convenience, compound primitives that combine register and I/O buffers, are also supplied.

macrofunction library

The development system macrofunction library encompasses over 100 high-level building blocks that can greatly increase design productivity. See the ADLIB™ and TTL macrofunctions manual that comes with the development system. The library contains the most commonly used TTL SSI and MSI functions. In addition, a number of more specialized macrofunctions have been added. These blocks perform logic functions in an optimum manner for EPLD implementation. They include counters implemented with toggle flip-flops, inhibit gates, combinational shift-registers/counters and a variety of useful logic structures not found in standard TTL devices.

starting a design

To get started on an EP1810 design the following sequence of preliminary steps is suggested. The equations given will help estimate how to build your system with EP1810s.

partitioning

Partition the complete system into functional blocks. Major functional blocks may be expressed in standard MSI TTL form for integration within the EP1810. Should the design require a multiple EPLD solution, the I/O connections which interface between the EPLDs should be minimized. The complete schematic should be structured as a set of subsystems such as counters, shift registers, comparators, etc., to allow easy design entry.

timing specifications

Knowledge of the base-clock frequency and critical-timing paths are necessary to make the correct choice of EPLDs. The EP1810 series can support circuits operating up to 33 MHz. Critical-timing paths are determined based upon input buffer, logic array, and output buffer delays. See switching characteristics. Smaller EPLDs, such as the EP910 or EP610, can be used for circuits that demand higher speed requirements on critical paths.

estimating a fit

To estimate the amount of logic that will fit into an EP1810, the number of input and output pins and the number of macrocells must be specified.

To estimate the number of macrocells, determine the number of buried flip-flops (flip-flops that do not drive output pins) and the number of macrocells used by macrofunctions. Since basic gates are implemented within the logic array, they usually do not require an entire macrocell. Therefore, they may be safely ignored in the estimation.

Each member of the macrofunction library has a maximum number of macrocells used to build the function. This number is shown in the lower right hand corner of the symbol. Refer to the ADLIB™ and TTL macrofunction manual to determine how many macrocells each macrofunction requires. Note that some macrofunctions have no macrocell specification. These functions use only a portion of the logic array, thus other logic could be added before the entire macrocell is used.

estimation formula

The estimation formula is as follows:

1. Determine the number of output pins = OP
2. Determine the number of input pins = IP (if less than 16 enter zero)
3. Determine the number of macrocells = BFF + MR where: BFF = buried flip-flops and MR = macrofunction requirements.

If OP + IP + BFF + MR < 48, the design will most likely fit into an EP1810. Complete the design using the TI EPLD Development System.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} (t ≤ 20 ns) . . . . . −2 V to 7 V
Programming supply voltage range, V_{PP} . . . . . −0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{PP} (t ≤ 20 ns) . . . . . −2 V to 13.5 V
Input voltage range, V_I . . . . . −0.3 V to 7 V
Instantaneous input voltage range, V_I (t ≤ 20 ns) . . . . . −2 V to 7 V
V_{CC} or GND current . . . . . −400 mA to 400 mA
Power dissipation at 25°C free-air temperature (see Note 2) . . . . . 2000 mW
Operating free-air temperature, T_A . . . . . −65°C to 135°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 240 mW at 135°C at the rate of 16 mW/°C.

recommended operating conditions

PARAMETER			EP1810I MIN	EP1810I MAX	EP1810C MIN	EP1810C MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
t_r	Rise time	CLK input		50		100	ns
		Other inputs		50		100	
t_f	Fall time	CLK input		50		100	ns
		Other inputs		50		100	
T_A	Operating free-air temperature		−40	85	0	70	°C

NOTE 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		EP1810I Min	EP1810I TYP†	EP1810I MAX	EP1810C MIN	EP1810C TYP†	EP1810C MAX	UNIT
V_{OH}	High-level output voltage	TTL	I_{OH} = −4 mA		2.4			2.4			V
		CMOS	I_{OH} = −2 mA		3.84			3.84			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.45			0.45	V
I_I	Input current		V_I = V_{CC} or GND				±10			±10	µA
I_{OZ}	Off-state output current		V_O = V_{CC} or GND				±10			±10	µA
I_{CC}	Supply current	Standby	V_I = V_{CC} or GND, No load	See Note 4		0.035	0.15		0.035	0.15	mA
		Non-turbo		See Note 5		10	40		10	30	
		Turbo		See Note 5		100	240		100	180	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C			20			20	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C			20			20	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C			25			25	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. When in the non-turbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with device programmed as four 12-bit counters and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

turbo-bit on

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd1(tot)}$	Input to nonregistered output delay	C_L = 35 pF		35		45	ns
$t_{pd2(tot)}$	I/O input to nonregistered output delay			40		50	ns
t_{in}	Input pad and buffer delay			7		7	ns
t_{io}	I/O input pad and buffer delay			5		5	ns
t_{lad}	Logic array delay			19		27	ns
t_{od}	Output buffer and pad delay	C_L = 35 pF		9		11	ns
t_{PZX}	Output buffer enable time			9		11	ns
t_{PXZ}	Output buffer disable time	C_L = 5 pF, See Note 6		9		11	ns

turbo-bit off

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd1(tot)}$	Input to nonregistered output delay	C_L = 35 pF		65		75	ns
$t_{pd2(tot)}$	I/O input to nonregistered output delay			70		80	ns
t_{in}	Input pad and buffer delay			7		7	ns
t_{io}	I/O input pad and buffer delay			5		5	ns
t_{lad}	Logic array delay			49		57	ns
t_{od}	Output buffer and pad delay	C_L = 35 pF		9		11	ns
t_{PZX}	Output buffer enable time			9		11	ns
t_{PXZ}	Output buffer disable time	C_L = 5 pF, See Note 6		9		11	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTE 6: This capacitance is for an output voltage change of 500 mV.

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synchronous/asynchronous clock mode, turbo-bit on

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	40		33.3		MHz
t_{su}	Register set-up time		10		11		ns
t_h	Register hold time		15		18		ns
t_{ch}	Clock high pulse duration		12		15		ns
t_{cl}	Clock low pulse duration		12		15		ns
t_{ic}	Clock delay			19		27	ns
t_{ics}	System clock delay			4		8	ns
t_{fd}	Feedback delay			6		7	ns
t_{clr}	Register clear time nonregistered output			24		32	ns
t_{cnt}	Minimum clock period (register output feedback to register input-internal data)			35		45	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	28.6		22.2		MHz

synchronous/asynchronous clock mode, turbo-bit off

PARAMETER†		TEST CONDITIONS	EP1810-35		EP1810-45		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	40		33.3		MHz
t_{su}	Register set-up time		10		11		ns
t_h	Register hold time		15		18		ns
t_{ch}	Clock high pulse duration		12		15		ns
t_{cl}	Clock low pulse duration		12		15		ns
t_{ic}	Clock delay			49		57	ns
t_{ics}	System clock delay			4		8	ns
t_{fd}	Feedback delay			−24		−23	ns
t_{clr}	Register clear time nonregistered output			54		62	ns
t_{cnt}	Minimum clock period (register output feedback to register input-internal data)			35		45	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	28.6		22.2		MHz

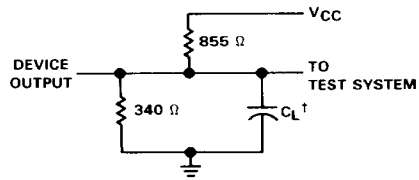
† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 5. f_{max} is measured with device programmed as four 12-bit counters.
7. The f_{max} values shown represent the highest frequency of operation without feedback.
8. The negative number shown for this specification is to compensate for the 30 ns that is being added to the t_{lad} parameter in the turbo-bit off mode. In the non-turbo mode, t_{fd} is not affected by the additional propagation delay because the logic array is already taken out of the non-turbo mode by the first transition into the array. See section on EPLD delay elements.

functional testing

The EP1810 is functionallly tested including complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP1810 allows test program patterns to be used and then erased.

Figure 6 shows the dynamic test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast-ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



†Includes jig capacitance

FIGURE 6. DYNAMIC TEST CIRCUIT

design security

The EP1810 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

turbo bit

Some EPLDs contain a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set using the TI EPLD Development System. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low power) mode is shown in Figure 7. All dynamic parameters are tested with the turbo bit on. Figure 8 shows the relationship between the output drive currents and the corresponding output voltages.

Figures 7 and 8 show the I_{CC} vs f_{max}, and output current vs output voltage.

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SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

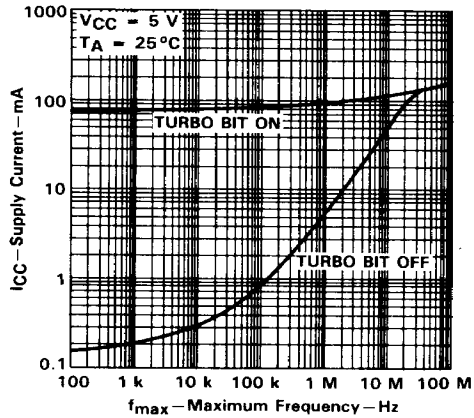


FIGURE 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

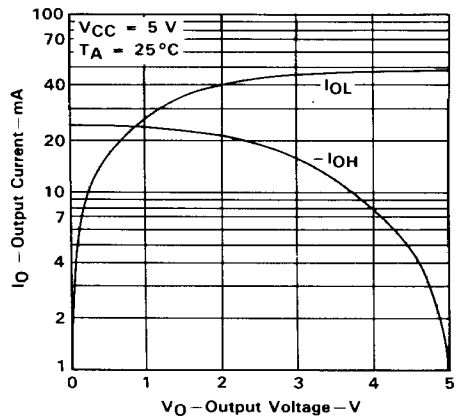
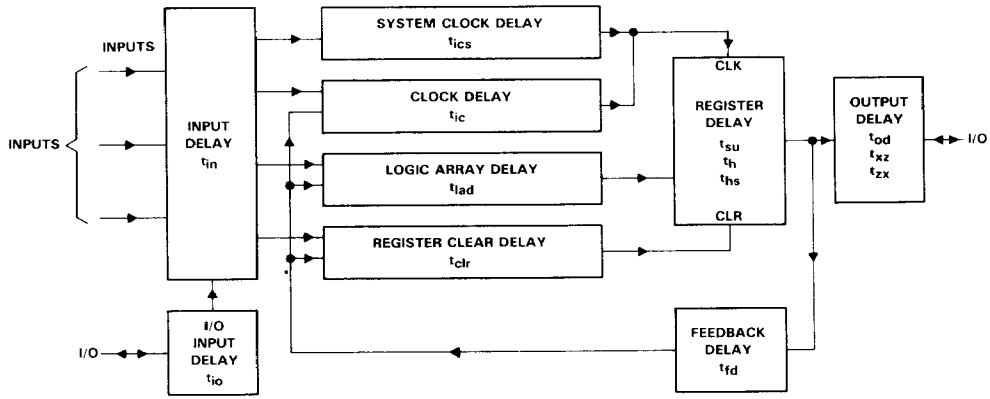


FIGURE 8

If the design requires low-power operation, the turbo bit should be off (disabled). When operating in this mode, some dynamic parameters are subject to increases.



NOTE: For combinatorial outputs, the delay between the logic array and the output buffer is zero. (i.e., $t_{su} = 0$ or $t_h = 0$)

FIGURE 9. EPLD MACROCELL DELAY PATHS MODEL

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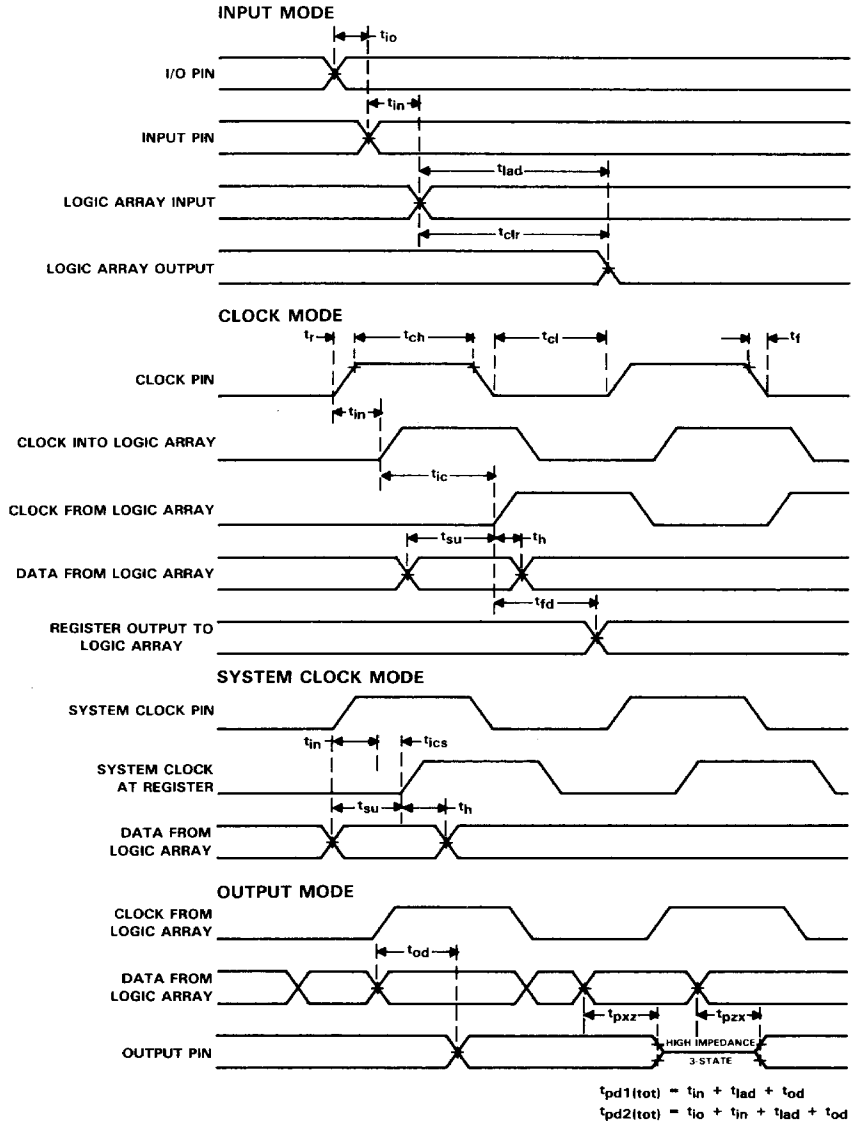

FIGURE 10. SWITCHING WAVEFORMS

understanding EPLD timing characteristics

introduction

One of the most important benefits of using an EPLD in any design is the integration of complex logic functions into single chip solutions in most cases. However, when the functional compatibility of a design has been determined, timing analysis should be completed to ensure AC parameter compatibility.

The purpose of this applications supplement is to discuss the timing delays which exist in the TI EPLDs. The focus here is on the inherent delay paths that exist in every EPLD and their relation to the data sheet switching specifications. This should aid designers in modelling and simulating their logic designs.

gate delays vs EPLD timing characteristics

Accurately modelling the timing characteristics requires an understanding of how a given application is implemented within the EPLD. Most designs targeted for EPLDs contain basic gates, and TTL macrofunctions, which are emulated by the EPLD general macrocell structure. The macrocell structure is an array of logic in an AND/OR configuration with a programmable inversion followed by an optional flip-flop and feedback, (See Figure 11).

When designing with EPLDs, the term "gate delay" is not a useful measure. Within the EPLD AND array are product terms. A product term is simply an n-input AND gate where n is the number of connections. Depending on the logic implemented, a single product term may represent one to several gate equivalents. Therefore, gate delays do not necessarily provide EPLD timing characteristics.

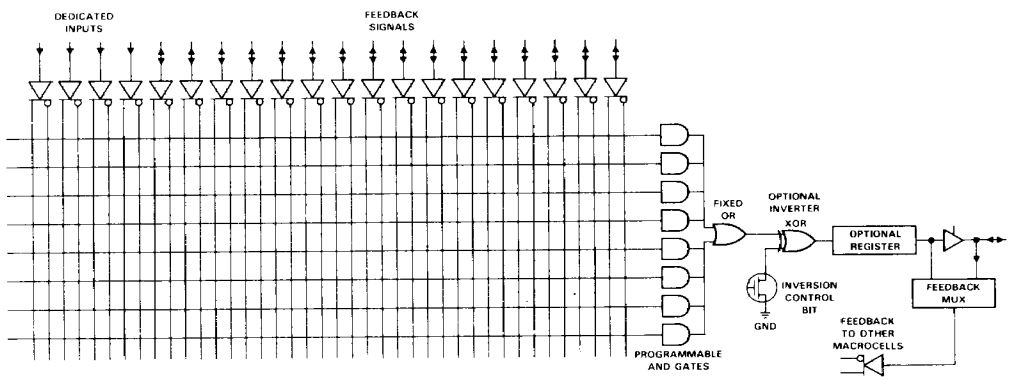

FIGURE 11. EPLD MACROCELL

AND/OR/INV structure

The AND portion consists of a column of AND gates, each of which has a very large number of possible inputs selected by EPROM bits. The EPROM bits serve as electrical switches. An erased bit passes the input into the AND gate (switch on), while a programmed bit cuts it off (switch off). All bits are initially erased.

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The number of possible inputs to an AND gate varies from 40 (EP610) to 88 (EP1810). In the EP610 and EP910 every dedicated input and its inversion and every macrocell feedback and its inversion are possible inputs to the AND gate. In the EP1810 which has local and global bussing, not all of the macrocell feedback is available at every AND gate. The reason larger devices such as the EP1810 do not have all feedbacks feeding the AND gates is to preserve the speed characteristics of the device.

Following the AND gates is a fixed 8 input OR function. This structure is called a fixed OR because the AND functions are hard wired into the OR gates, and cannot be redistributed if unused.

The OR gate feeds a programmable inverter (XOR). A dedicated EPROM bit either programs the inversion function on or off.

EPLD delay elements

The simplest solution to the architectural requirements is to model time through the logic array as a constant. This parameter is called t_{lad}. The rest of the elements in the timing model are similar to those found in conventional logic. There are input and output delay parameters (t_{in}, t_{io}, t_{od}); register parameters (t_{su}, t_h, t_{clr}, t_{hs}, t_{ics}, t_{ic}); and internal connection parameters (t_{fd}). A detailed diagram of an EPLD Macrocell Delay Paths Model is shown in Figure 9 with a description of the signals.

glossary – internal delay elements

t_{clr} - Asynchronous register clear time. This is the amount of time it takes for a low signal to appear at the output of a register after the transition at the logic array, including the time required to go through the logic array.

t_{fd} - Feedback delay. In registered applications, this is the delay from the output of the register to the input of the logic array. In combinational applications, it is the delay from the combinational feedback to the input of the logic array.

t_h - Register hold time. This is the internal hold time of the register inside a macrocell: measured from the register clock to the register data input.

t_{lad} - Logic array delay. This parameter incorporates all delay from an input or feedback through the AND/OR structure.

t_{ic} - Clock delay. This delay incorporates all the delay incurred between the output of an input pad or I/O pad and the clock input of a register including the time required to go through the logic array. This delay is differentiated from the system clock delay tics by the need to pass through a CLKB primitive, which specifies individual register clocking.

t_{ics} - System clock delay. This delay incorporates all delays incurred between the output of the input pad and the clock input of the registers for dedicated clock pins.

t_{in} - Input pad and buffer delay which direct the true and complement data input signals into the AND array.

t_{io} - I/O input pad delay. This delay applies to I/O pins committed as inputs.

t_{od} - Output buffer and pad delay. For registered applications, this incorporates the clock to output delay of the flip flop. In combinational applications, it incorporates delay from the output of the array to the output of the device.

t_{su} - Register setup time. This is the internal setup time of the register inside a macrocell - measured from the register data input until the register clock.

t_{xz} - Time to 3-state output delay. This delay incorporates the time between a high-to-low transition on the enable input of the 3-state buffer to assertion of a high impedance value at an output pin.

t_{zx} - 3-state to active output delay. This delay incorporates the time between a low-to-high transition on the enable input of the 3-state buffer to assertion of a high or low logic level at an output pin.

explaining the EPLD data sheet specifications

The data sheet for each TI EPLD references timing parameters which characterize the switching operating specifications. These parameters are measured values, derived from extensive device characterization and 100% device testing. Among the switching characteristics are the following: $t_{aco1(tot)}$, $t_{acnt(tot)}$, $t_{ah(tot)}$, $t_{asu(tot)}$, $t_{co1(tot)}$, $t_{clr(tot)}$, $t_{cnt(tot)}$, $t_{h(tot)}$, $t_{pd1(tot)}$, $t_{pd2(tot)}$, $t_{PXZ(tot)}$, $t_{PZX(tot)}$, $t_{su(tot)}$. These parameters, described below in detail, may be represented by the EPLD internal delay elements. (See Figure 12)

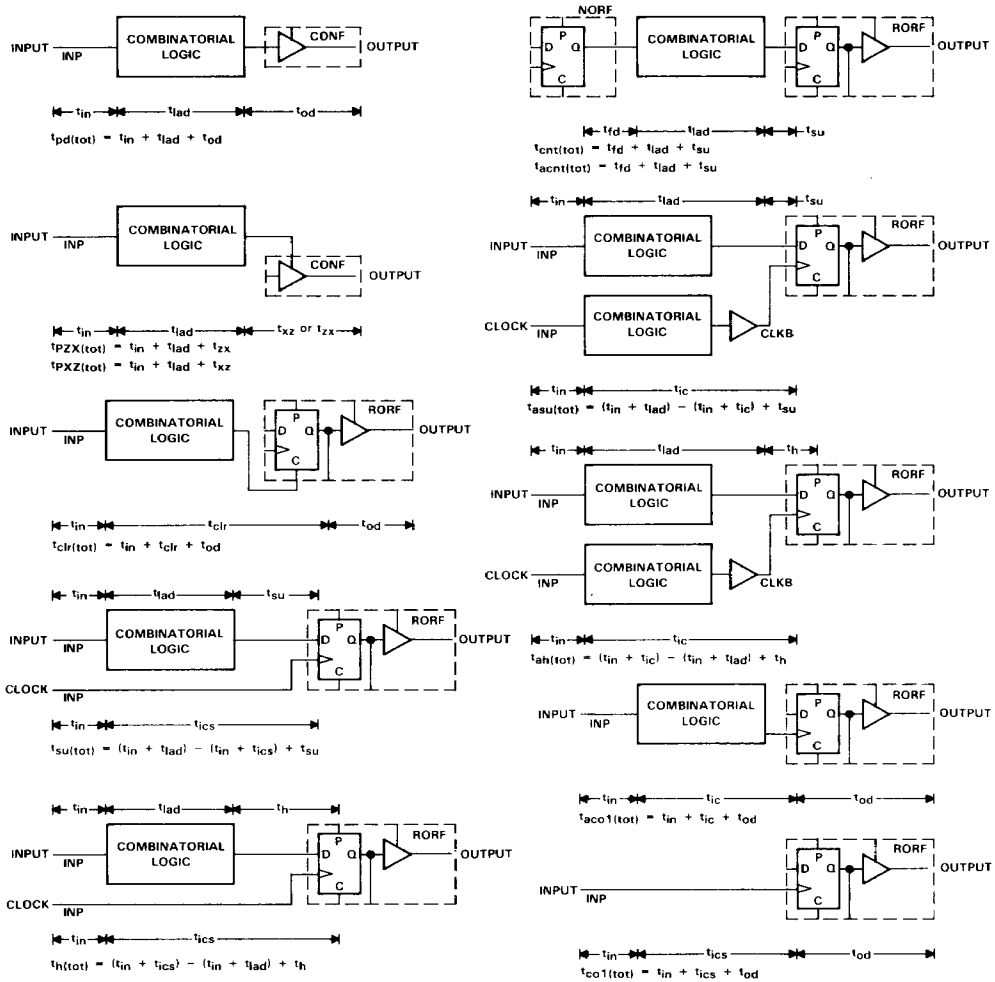

FIGURE 12. TI EPLD TIMING EQUATIONS

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glossary — external delay elements

$t_{aco1(tot)}$ - Defined as the asynchronous clock to output delay. It is the time required to obtain a valid output after a clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the output delay (t_{od}).

$t_{acnt(tot)}$ - Defined as the asynchronous clocked counter period. It is the minimum period a counter can maintain when asynchronously clocked. This delay is the sum of the feedback delay (t_{fd}) and the logic array delay (t_{lad}), and the register setup time (t_{su}).

$t_{ah(tot)}$ - Defined as the asynchronous hold time. It is the amount of time required for data to be present after an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the hold time (t_h) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{asu(tot)}$ - Defined as asynchronous setup time. It is the time required for data to be present at the input to the register before an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), array delay (t_{lad}) and the register setup time (t_{su}) and the sum of the input delay (t_{in}) and the clock delay (t_{ic}).

$t_{co1(tot)}$ - Defined as system clock to output delay. It is the time required to obtain a valid output after the system clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the system clock delay (t_{ics}), and the output delay (t_{od}).

$t_{clr(tot)}$ - Defined as delay required to clear register. It is the time required to change the output from high to low through a register clear measured from an input transition. This delay is the sum of input delay (t_{in}), register clear delay (t_{clr}), and the output delay (t_{od}).

$t_{cnt(tot)}$ - Defined as the system clock counter period. It is the minimum period a counter can maintain. This delay is the sum of the feedback delay (t_{fd}), the logic array delay (t_{lad}), and the internal register setup time (t_{su}).

$t_{h(tot)}$ - Defined as hold time for the register. It is the amount of time the data must be valid after the system clock. It is the difference between the sum of the internal input delay (t_{in}), the system clock (t_{ics}), and the system-clock hold time (t_{hs}) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{pd1(tot)}$ - Propagation Delay; Defined as the delay from a dedicated input to a non-registered output. This is the time required for data to propagate through the logic array and appear at the EPLD external output pin. This delay is the sum of input delay (t_{in}), array delay (t_{lad}) and output delay (t_{od}).

$t_{pd2(tot)}$ - Propagation Delay; Defined as the delay from I/O pin to a nonregistered output. This is the time required for data from any external I/O input to propagate through any combinational logic and appear at the external output pin of an EPLD. This delay is the sum of the I/O delay (t_{io}), input delay (t_{in}), array delay (t_{lad}), and the output delay (t_{od}).

$t_{PXZ(tot)}$ - Defined as the time to enter into 3-state. It is the time required to change an external output from a valid high or low logic level to 3-state from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to activate the 3-state buffer (t_{xz}).

$t_{PZX(tot)}$ - Defined as the delay from high impedance to active output. It is the time required to change an external output from 3-state to a valid high or low logic level measured from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to de-activate the 3-state buffer (t_{zx}).

$t_{su(tot)}$ - Defined as set up time for the register. It is the time required for data to be present at the register before the system clock. This value is the difference between the sum of input delay (t_{in}), array delay (t_{lad}), and an internal register setup time (t_{su}) and the sum of the input delay (t_{in}) and the system clock delay (t_{ics}).

conclusion

To understand timing relationships in the EP1810 and all EPLDs, it is very important to break up the internal paths into meaningful microparameters that model portions of the EPLD architecture. Once internal paths are decomposed, it is then possible to obtain accurate timing information by summing the appropriate combinations of these microparameters. The EP1810 data sheet and relevant EPLD data sheets provide architectural information on which the parameters apply and how the primitives are implemented.The TI EPLD Development System provides minimized files that aid in the decomposition of designs. The combination of these elements and the knowledge of the architecture of each device allow characterization of any timing path within an EPLD.

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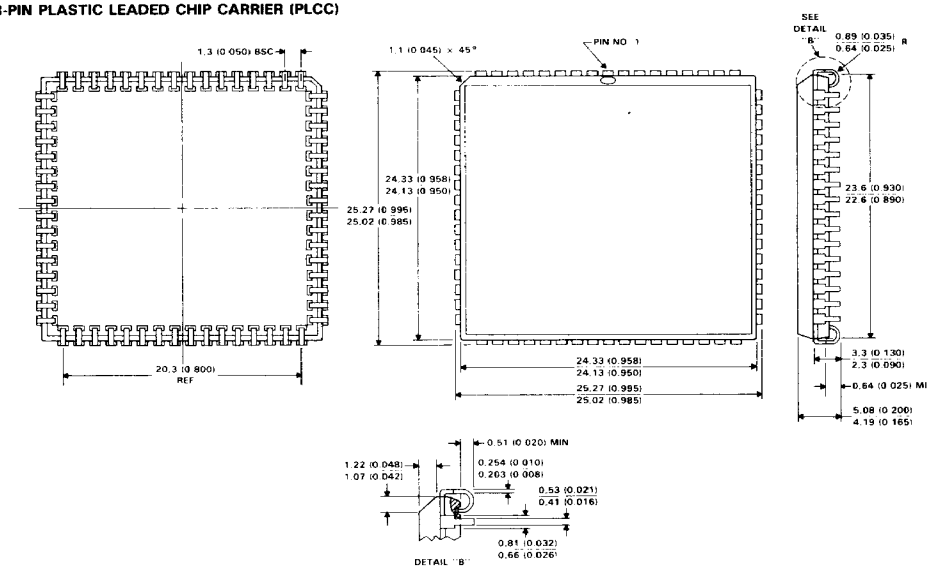
MECHANICAL DATA

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



68-PIN CLCC CERAMIC