MPLDs
Mask-Programmed Logic Devices

September 1991, ver. 1 — **Data Sheet**

Features

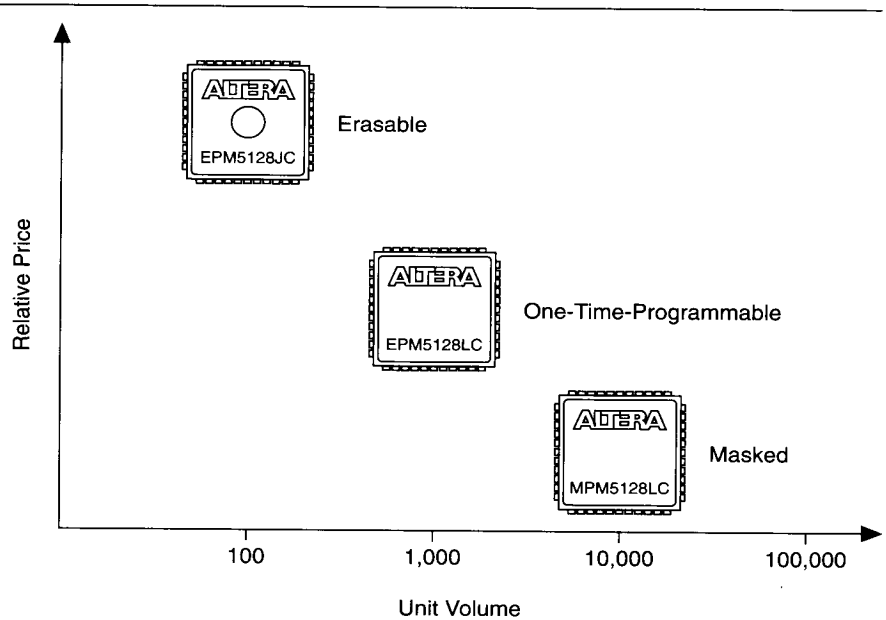
- Masked versions of EPLD designs
- Reduced cost for large-volume applications
- Available for EP1810, EPM5032, EPM5064, EPM5128, EPM5130, EPM5192, and EPS464 EPLDs
- Pin-, function-, and timing-compatible with original EPLD design
- Conversion process handled by Altera
- Fast turn-around to reduce time-to-market
- Test vectors generated by Altera
- Low power
- *N*-to-1 option combines multiple EPLDs into a single MPLD

General Description

The Altera Mask-Programmed Logic Devices (MPLDs) provide a masked alternative to EPLD designs. By using a generic CMOS process and removing all EPROM cells, Altera passes considerable savings on to customers who anticipate high-volume production. The combination of Altera EPLDs and MPLDs provides the best of both worlds: the fast time-to-market offered by EPLDs, and the low cost and low risk offered by MPLDs. See Figure 1.

Figure 1. EPLD/MPLD Economics

As volumes increase during production, a design can move from windowed ceramic EPLDs to one-time-programmable EPLDs, and finally to MPLDs.



The EPLD-to-MPLD conversion is handled by Altera so that no redesign effort is required. Altera guarantees that the MPLD meets the worst-case AC and DC parameters of the original EPLD design. In addition, Altera automatically generates test vectors with over 95% fault coverage.

EPLD/MPLD Compatibility

An Altera MPLD is guaranteed to be pin-, function-, and timing-compatible with the original EPLD design. This guarantee ensures that the MPLD can replace the EPLD without interrupting production.

Pin compatibility guarantees that both the pin-out and DC specifications of the MPLD match those of the original EPLD design. In addition, the MPLD typically will consume less than one-tenth of the power of the equivalent EPLD, depending on the design and operating conditions.

Functional compatibility of the MPLD is ensured by directly mapping the primitives within the EPLD (product terms, programmable flip-flops, etc.) to specially designed elements within the MPLD. Altera employs a proprietary logic synthesis program that uses the Simulator Netlist File (.SNF) generated by MAX+PLUS or MAX+PLUS II software. (Designs developed with A+PLUS software are converted to MAX+PLUS II format.) The SNF reflects the final synthesis, placement, and routing of the original EPLD design. The conversion process pays special attention to the wide fan-in of product terms and the wide fan-out of registers commonly found in EPLD applications.

An MPLD is guaranteed to meet the worst-case timing parameters of the corresponding EPLD, as specified in the EPLD data sheet. Provided that the design engineer performs worst-case analysis of the EPLD, the same analysis will hold for the MPLD. Therefore, the timing of the original design and the overall system is maintained when the EPLD is replaced with an MPLD.

Design for Testability

Test vector generation is one of the most time-consuming tasks required for ASIC design. A significant advantage of EPLDs is that they are fully tested before they are shipped and are verified at programming time; test vectors are not required.

MPLD designs include a partial-scan testing structure that parallels the testability available in EPLDs. The partial-scan structure allows Altera to create test vectors with over 95% fault coverage for all stuck-at and open faults. This high fault coverage is maintained regardless of whether synchronous or asynchronous design techniques are used.

The built-in design-for-testability frees the design engineer from the burden of creating a testable design and test vectors. In fact, customer-provided simulation vectors are optional for EPLD-to-MPLD conversions.

N-to-1 MPLD Conversion Option

Many applications use multiple EPLDs on a single board for both prototyping and production. In some applications it may be desirable to perform prototyping with multiple EPLDs, but shift to a single-device implementation for high-volume production. Altera's EPLD-to-MPLD conversion program provides this capability with the "*N*-to-1" conversion option, which offers the benefits of developing with EPLDs even when production constraints require a high-density single-device solution.

The *N*-to-1 MPLD conversion works in conjunction with the design partitioning feature in MAX+PLUS II software. Partitioning allows a design engineer to create a large design without concern for design size or fitting constraints. MAX+PLUS II automatically partitions the design and fits each portion into a separate EPLD. Multiple EPLDs can be used for design prototyping while simulation and timing analysis can be completed on the top-level design.

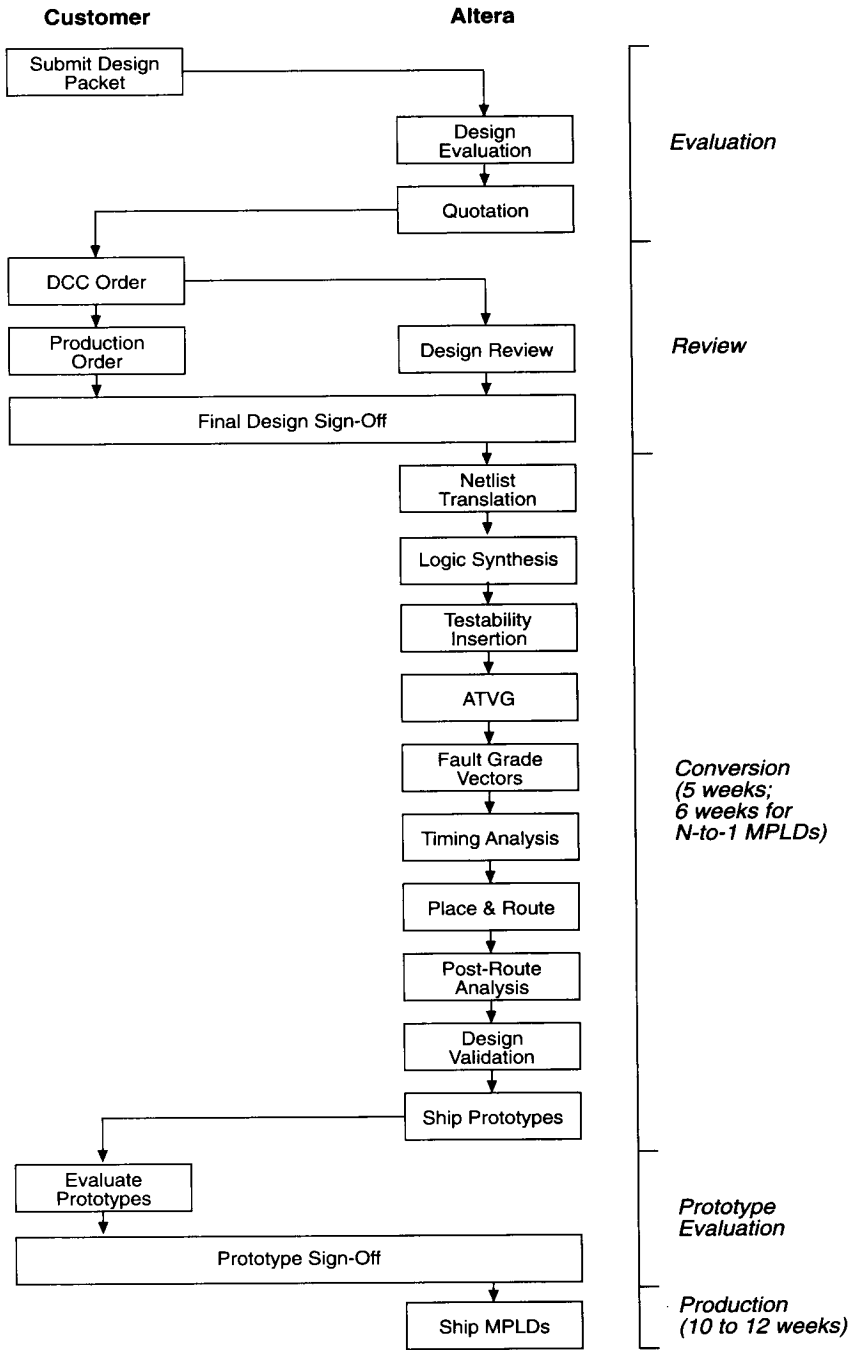
The *N*-to-1 option combines a multi-EPLD design into a single MPLD that is function- and timing-compatible with the original multi-EPLD solution. The package and pin-out are determined by the application's requirements. A wide range of package options is available.

Quick, Seamless Conversion

One of the principal objectives of Altera's EPLD-to-MPLD conversion program is to minimize the design engineer's involvement in the conversion. The engineer simply submits design files created with A+PLUS, MAX+PLUS, or MAX+PLUS II software and Altera delivers MPLDs within weeks of the design sign-off. By handling the conversion process, Altera frees the engineer to begin developing the next-generation project.

The MPLD design flow chart (see Figure 2) shows how easily an EPLD can be converted to an MPLD. To submit a design for quotation, an ***MPLD Conversion Information & Order Forms*** workbook can be obtained from the local Altera representative. The design engineer needs only to submit the design files and the workbook's *Checklist*, *Information Form*, and *Questionnaire* to Altera. Altera then performs a design evaluation and returns a price quote for the conversion.

Figure 2. MPLD Conversion Design Flow



After the customer submits an order for the Design Conversion Cost (DCC), an Altera engineer reviews the design and submits a *Final Design Sign-Off Form* for customer approval. This form describes the specifications of the MPLD in detail. After sign-off, Altera begins the design conversion.

The design conversion includes netlist translation, logic synthesis, testability insertion, Automatic Test Vector Generation (ATVG), fault grading, timing analysis, place-and-route, post-route timing analysis, design validation, and the manufacture of the prototypes. The entire conversion, from final design sign-off to prototype delivery, takes less than 5 weeks (6 weeks for *N*-to-1 conversion). Production quantities are delivered 10 to 12 weeks after the customer returns the *Prototype Sign-Off Form.*

Conclusion

The two most important design goals faced by engineers today are reducing time-to-market and system cost. The combination of Altera EPLDs and MPLDs provides a solution that fills these needs, allowing a company to take a product to market quickly, without raising the cost or risk of production.