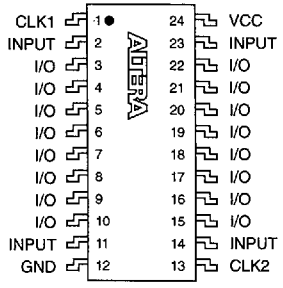
Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 clock pins
- EP610, EP610I, and EP600I devices that are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 7):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin ceramic and plastic dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

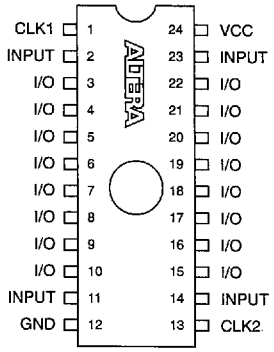
Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



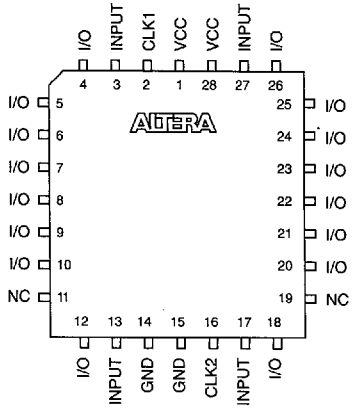
24-Pin SOIC

EP610



24-Pin DIP

EP610
EP610I



28-Pin PLCC

EP610
EP610I

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 signal is a dedicated clock input for the registers in macrocells 9 through 16. The CLK2 signal is a dedicated clock input for registers in macrocells 1 through 8.

Figure 8. EP610 Block Diagram

Numbers without parentheses are for both DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

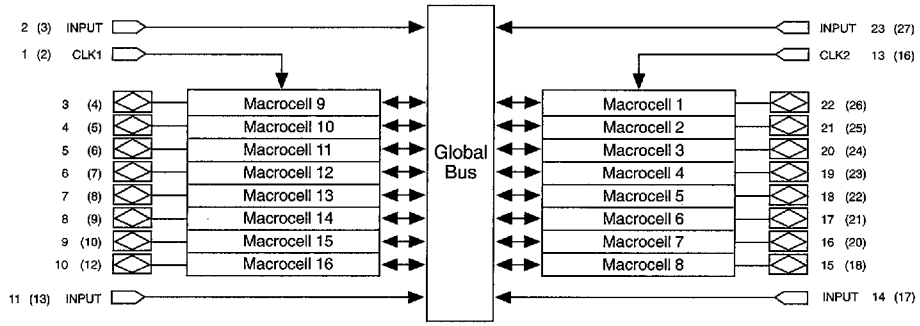


Figure 9 shows the typical supply current (I_{CC}) versus frequency for EP610 devices.

Figure 9. I_{CC} vs. Frequency of EP610 Devices

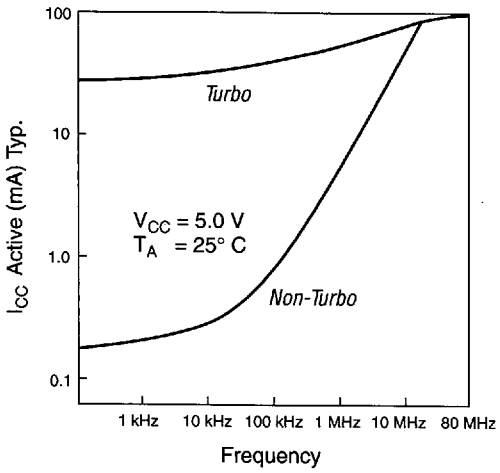
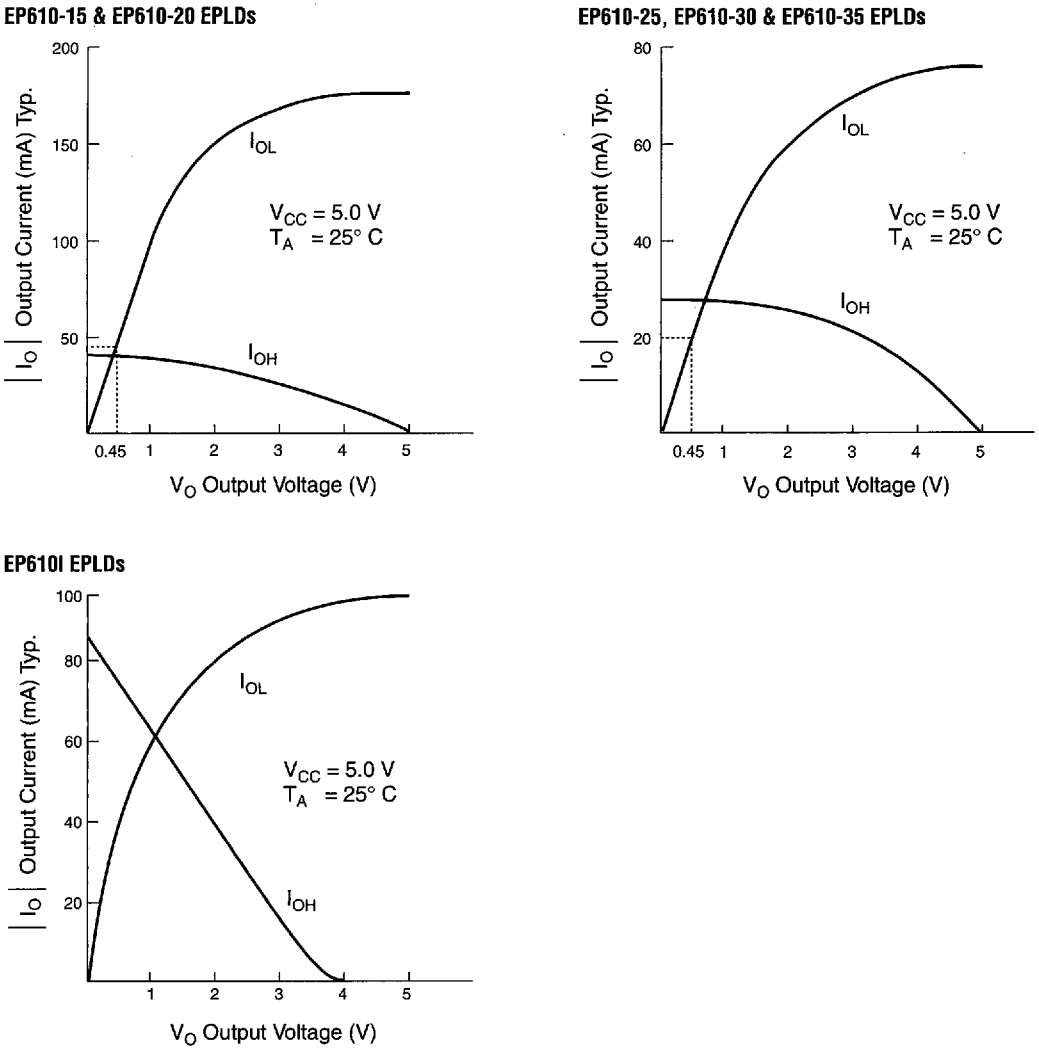


Figure 10 shows the maximum output drive characteristics of EP610 devices.

Figure 10. Output Drive Characteristics of EP610 Devices



EP610 & EP610I Device Absolute Maximum Ratings *Notes (1), (2)*

			EP610		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to GND, *Note (3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or GND current		–175	175			mA
I_{OUT}	DC output current, per pin		–25	25			mA
P_D	Power dissipation			1,000			mW
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135 (125)	–10	85	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

EP610 & EP610I Device Recommended Operating Conditions *Notes (2), (4)*

			EP610		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Note (5)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	–40	85	° C
t_R	Input rise time	*Note (6)*		100 (50)		500	ns
t_F	Input fall time	*Note (6)*		100 (50)		500	ns

EP610 & EP610I Device DC Operating Conditions *Notes (2), (4)*

Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC *Notes (8), (9)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10	10	µA

8 Classic

EP610 & EP610I Device Capacitance *Note (10)*

			EP610I		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		12	pF

EP610 Device I_{CC} Supply Current *Notes (2), (7)*

				EP610			
Symbol	**Parameter**	**Conditions**	**Speed Grade**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or GND, no load *Notes (11), (12), (13)*			20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or GND, no load f = 1.0 MHz, *Note (13)*			5	10 (15)	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	*Notes (12), (13)*	-15, -20		60	90 (115)	mA
			-25, -30, -35		45	60 (75)	mA

EP610I Device I_{CC} Supply Current *Note (7)*

			EP610I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or GND, no load, *Notes (11), (12), (13)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (11), (13)*		3	8	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (11), (13)*		65	105	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range versions.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(4) Operating conditions: $V_{CC} = 5.0\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5.0\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.
(5) For EP610 devices, maximum V_{CC} rise time is 50 ms. For EP610I devices, V_{CC} rise time is unlimited with monotonic rise.
(6) For EP610-15 and EP610-20 EPLDs: t_R and $t_F = 40$ ns.
For EP610-15 and EP610-20 clocks: t_R and $t_F = 20$ ns.
(7) Typical values are for $T_A = 25°\ C$ and $V_{CC} = 5\ V$.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) This parameter does not apply to EP610I devices.
(10) The device capacitance was measured at 25° C and was sample-tested only. The clock-pin capacitance is for dedicated clock inputs only. For EP610-25, EP610-30, and EP610-35: Pin 13 has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and $C_{CLK} = 20$ pF.
(11) When the Turbo Bit is not set (non-Turbo mode), an EP610 EPLD enters standby mode if no logic transitions occur for 100 ns after the last transition. When the Turbo Bit is not set, an EP610I device enters standby mode if no logic transitions occur for 75 ns after the last transition.
(12) Measured with a device programmed as a 16-bit counter. The I_{CC} was measured at 0° C.
(13) Data path is programmed as a 16-bit counter.

EP610-15 & EP610-20 Device AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17		22	20	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
f_{MAX}	Maximum clock frequency	*Note (5)*	83.3		62.5		0	MHz
t_{SU}	Global clock input setup time		9		11		20	ns
t_{H}	Global clock input hold time		0		0		0	ns
t_{CH}	Global clock high time		6		8		0	ns
t_{CL}	Global clock low time		6		8		0	ns
t_{CO1}	Global clock to output delay			11		13	0	ns
t_{CNT}	Global clock minimum period			12		16	0	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	83.3		62.5		0	MHz
t_{ASU}	Array clock input setup time		6		8		20	ns
t_{AH}	Array clock input hold time		6		8		0	ns
t_{ACH}	Array clock high time		7		9		0	ns
t_{ACL}	Array clock low time		7		9		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (7)*	1		1		1	ns
t_{ACO1}	Array clock to output delay			15		20	20	ns
t_{ACNT}	Array clock minimum period			14		18	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	71.4		55.6		0	MHz

Internal Timing Parameters			EP610-15		EP610-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			4		4	ns
t_{IO}	I/O input pad and buffer delay			2		2	ns
t_{LAD}	Logic array delay			6		11	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		5		4		ns
t_{H}	Register hold time		4		7		ns
t_{IC}	Array clock delay			6		11	ns
t_{ICS}	Global clock delay			2		4	ns
t_{FD}	Feedback delay			1		1	ns
t_{CLR}	Register clear time			6		11	ns

EP610-25, EP610-30 & EP610-35 AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (11)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
f_{MAX}	Maximum frequency	*Note (5)*	47.6		41.7		37		0	MHz
t_{SU}	Global clock input setup time		21		24		27		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		10		11		12		0	ns
t_{CL}	Global clock low time		10		11		12		0	ns
t_{CO1}	Global clock to output delay			15		17		20	0	ns
t_{CNT}	Global clock minimum period			25		30		35	0	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	40		33.3		28.6		0	MHz
t_{ASU}	Array clock input setup time		8		8		8		30	ns
t_{AH}	Array clock input hold time		12		12		12		0	ns
t_{ACH}	Array clock high time		10		11		12		0	ns
t_{ACL}	Array clock low time		10		11		12		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (7)*	1		1		1			ns
t_{ACO1}	Array clock to output delay			27		32		37	30	ns
t_{ACNT}	Array clock minimum period			25		30		35	0	ns
f_{ACNT}	Max. internal global clock frequency	*Note (6)*	40		33.3		28.6		0	MHz

Internal Timing Parameters			EP610-25		EP610-30		EP610-35		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			8		9		11	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	ns
t_{LAD}	Logic array delay			11		14		15	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		7		9	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		7		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		7		9	ns
t_{SU}	Register setup time		11		11		12		ns
t_{H}	Register hold time		10		10		10		ns
t_{IC}	Array clock delay			13		16		17	ns
t_{ICS}	Global clock delay			1		1		0	ns
t_{FD}	Feedback delay			3		5		8	ns
t_{CLR}	Register clear time			13		16		17	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book for additional internal timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit is off.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 16-bit counter. I_{CC} is measured at 0° C.

(7) Sample tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

EP610 Device AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			EP610I-10		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output, *Note (4)*	C1 = 35 pF		10	25	ns
t_{PD2}	I/O input to non-registered output, *Note (4)*			10	25	ns
t_{PZX}	Input to output enable			15	25	ns
t_{PXZ}	Input to output disable, *Note (5)*	C1 = 5 pF *Note (4)*		13	25	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		13	25	ns
f_{MAX}	Maximum frequency	*Note (5)*	125		0	MHz
t_{SU}	Global clock input setup time		7		25	ns
t_H	Global clock input hold time		0		0	ns
t_{CH}	Global clock high time		5		0	ns
t_{CL}	Global clock low time		5		0	ns
t_{CO1}	Global clock to output delay			6.5	0	ns
t_{CNT}	Global clock minimum period			10	25	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	100		0	MHz
t_{ASU}	Array clock input setup time		1.5		25	ns
t_{AH}	Array clock input hold time		5.5		0	ns
t_{ACH}	Array clock high time		5		0	ns
t_{ACL}	Array clock low time		5		0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (7)*	1		0	ns
t_{ACO1}	Array clock to output delay			12	25	ns
t_{ACNT}	Array clock minimum period	*Note (6)*		10	25	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	100		0	MHz

Internal Timing Parameters			EP610I-10		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			1.5	ns
t_{IO}	I/O input pad and buffer delay			0.0	ns
t_{LAD}	Logic array delay			5.5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		8.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0	ns
t_{SU}	Register setup time		3.5		ns
t_{H}	Register hold time		3.5		ns
t_{IC}	Array clock delay			7.5	ns
t_{ICS}	Global clock delay			2.0	ns
t_{FD}	Feedback delay			1.0	ns
t_{CLR}	Register clear time			8.5	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) See *Application Note 78 (Understanding MAX 7000, MAX 5000 & Classic Timing)* in this data book for additional internal timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit is off.

(4) Measured with eight outputs switching.

(5) Sample-tested only for an output change of 500 mV.

(6) Measured with a device programmed as a 16-bit counter.

(7) Sample tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.