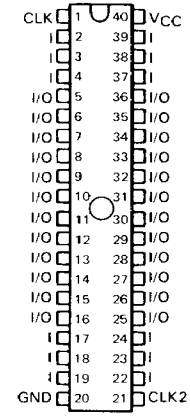
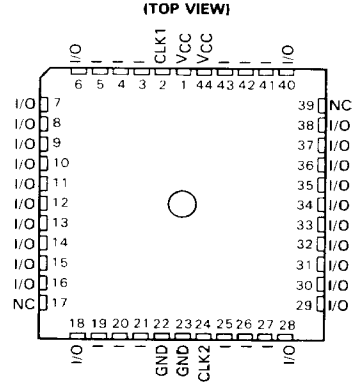
- High-Density (Over 900 Gates) Replacement for TTL and 74HC
- Virtually Zero Standby Power . . . Typ 20 µA
- High Speed:
  Propagation Delay Time . . . 30 ns
- Asynchronous Clocking of All Registers or Banked Register Operation from 2 Synchronous Clocks
- 24 Macrocells with Configurable I/O Architecture Allowing for Up to 36 Inputs and 24 Outputs
- Each Output Macrocell User-Programmable for D, T, SR, or JK Flip-Flops with Individual Clear Control or Combinational Operation
- UV-Light-Erasable Cell Technology Allows for:
  Reconfigurable Logic
  Reprogrammable Cells
  Full Factory Testing for 100% Programming Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State Machine Design Entry
- Package Options Include Plastic [For One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Packages and J-Leaded Chip Carriers

DUAL-IN-LINE PACKAGE
(TOP VIEW)



CHIP-CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE			
		CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	CERAMIC CHIP CARRIER (CLCC)	PLASTIC† DUAL-IN-LINE PACKAGE (PDIP)	PLASTIC† CHIP CARRIER (PLCC)
0°C – 70°C	30 ns	EP910DC-30	EP910JC-30	EP910PC-30	EP910LC-30
	35 ns	EP910DC-35	EP910JC-35	EP910PC-35	EP910LC-35
	40 ns	EP910DC-40	EP910JC-40	EP910PC-40	EP910LC-40
–40°C – 85°C	45 ns	EP910DI-45	EP910JI-45	EP910PI-45	EP910LI-45

†This package is for One-Time-Programmable (OTP) devices.

description

general

The Texas Instruments EP910 Erasable Programmable Logic Device is capable of implementing over 900 equivalent gates of SSI and MSI logic functions accommodating up to 36 inputs and 24 outputs all in plastic and ceramic space-saving 40-pin, 600-mil dual-in-line (DIP) packages and 44-pin chip-carrier packages.

Each of the 24 macrocells contains a programmable-AND, fixed-OR PLA structure that yields 8 product terms for logic implementation and a single product term for output-enable and asynchronous-clear control functions. The architecture of the output logic macrocell allows the EP910 user to program output and feedback paths for both combinational or registered operation, active high or active low.

For increased flexibility, the EP910 also includes programmable registers. Each of the 24 internal registers may be programmed to be a D, T, SR, or JK flip-flop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

In addition to density and flexibility, the performance characteristics allow the EP910 to be used in the widest possible range of applications. The CMOS EPROM technology reduces the power consumption to less than 20% of equivalent bipolar devices without sacrificing speed performance. Another advantage is 100% generic testing. The device can be erased with ultraviolet (UV) light. Design changes are no longer costly, nor is there a need for post-programming testing.

Programming the EP910 is accomplished by using the TI EPLD Development System, which supports four different design entry methods. When the design has been entered, the software performs automatic translation into logical equations, Boolean minimization, and design fitting directly into an EP910. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

functional

The EP910 is an Erasable Programmable Logic Device (EPLD) that uses a CMOS EPROM technology to implement logic designs in a programmable AND-logic array. The device also contains a revolutionary programmable I/O architecture that provides advanced functional capability for user programmable logic.

Externally, the EP910 provides 12 dedicated data inputs and 24 I/O pins, which may be configured for input, output, or bidirectional operation. Figure 1 shows the EP910 basic macrocell. The internal architecture is organized with the familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from the true and complement signal from 12 dedicated data inputs and 24 feedback signals originating from each of the 24 I/O architectural control blocks. The 72-input AND array encompasses 240 product terms, which are distributed among 24 available macrocells. Each EP910 product term represents a 72-input AND gate.

At the intersection point between each AND array input and each product term, there is an EPROM control cell. In the erased state, all connections are made. This means both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement form of any array input signal.

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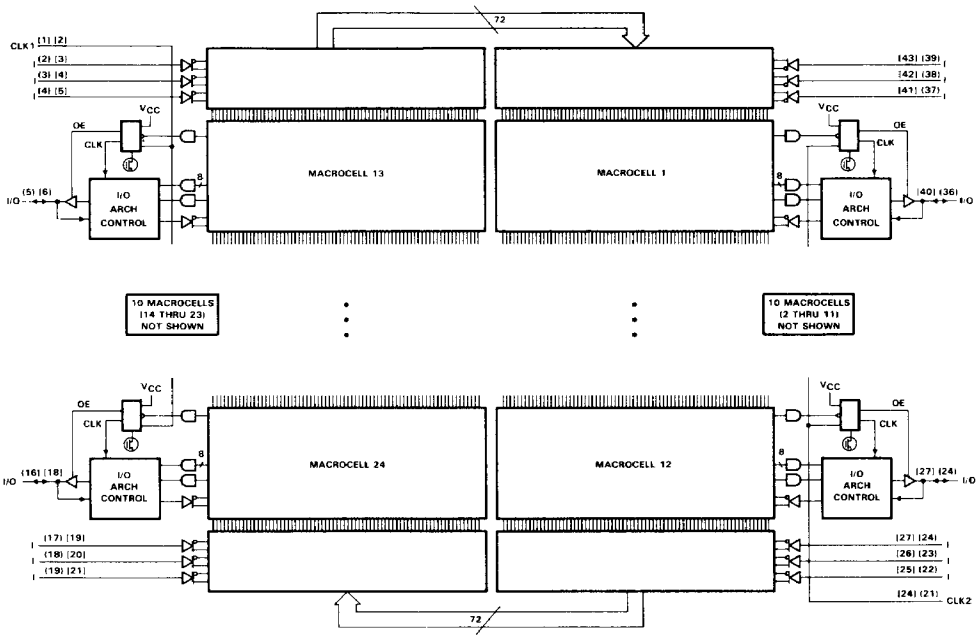
functional block diagram

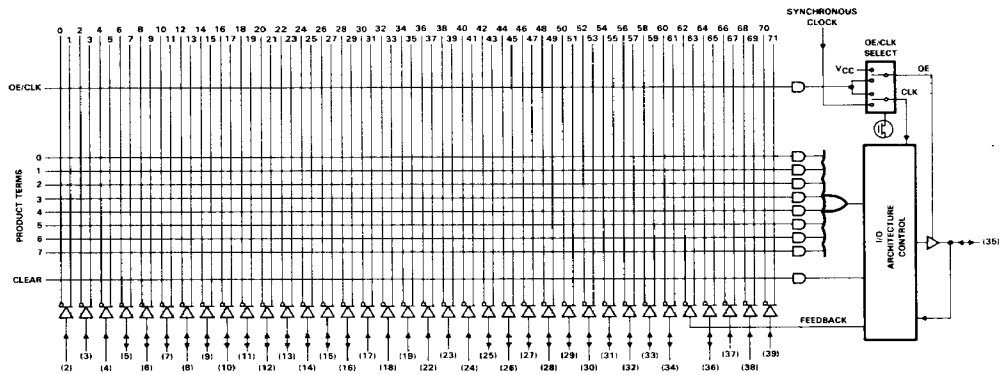


Pin numbers in parenthesis are for DIP packages. Pin numbers in brackets are for chip-carrier packages.

When both the true and complement of an array input signal are connected, a logical false results on the output of the AND gate. When both the true and complement forms of any array input signal are programmed open, then a logical "don't care" results for that input. If all 72 inputs for a given product term are programmed open, then a logical true state results on the output of the corresponding AND gate. Two dedicated clock inputs (not available in the AND array) provide the clock signals used for asynchronous clocking of the EP910 internal registers. Each of these clock signals is positive-edge triggered and has control over a bank of 12 registers. CLK1 controls registers associated with macrocells 13 through 24. CLK2 controls registers associated with macrocells 1 through 12. The EP910 advanced I/O architecture allows the number of synchronous registers to be user defined, from 1 to 24. Both dedicated clock inputs are positive-edge triggered.

I/O architecture

The EP910 input/output architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinational or registered output, with programmable output polarity. Four different types of registers (D, T, JK, and SR) can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP910 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.



Pin numbers shown are for dual-in-line packages.

FIGURE 1. LOGIC ARRAY MACROCELL (MACROCELL 1 ILLUSTRATED)

OE/CLK selection

Figure 2 shows the two modes of operation that are provided by the OE/CLK select multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each of the EP910 I/O pins. In Mode 0, the 3-state output buffer is controlled by the OE/CLK product term. If the output of the AND gate is true, the output buffer is enabled. If the output of the AND gate is false, the output buffer is in the high-impedance state. In this mode, the macrocell flip-flop is clocked by its respective synchronous clock input signal (CLK1 or CLK2). After erasure, the OE/CLK select multiplexer is configured in Mode 0.

In Mode 1, the output-enable buffer is always enabled. The macrocell flip-flop may now be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flip-flops from any of the 72 available AND array input signals. Because both true and complement signals reside in the AND array, the flip-flop may be configured for positive- or negative-edge-triggered operation. With the clock now controlled by a product term, gated clock structures are also possible.

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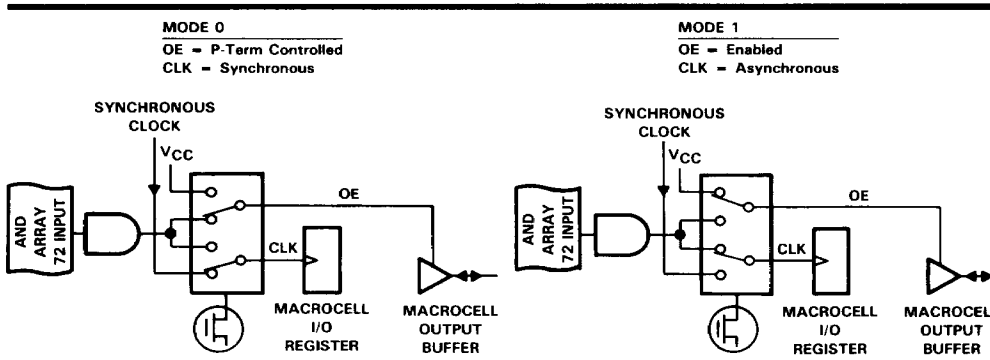


The register is clocked by the synchronous clock signal, which is common to 11 other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP910.

FIGURE 2. OE/CLK SELECT MULTIPLEXER

output/feedback selection

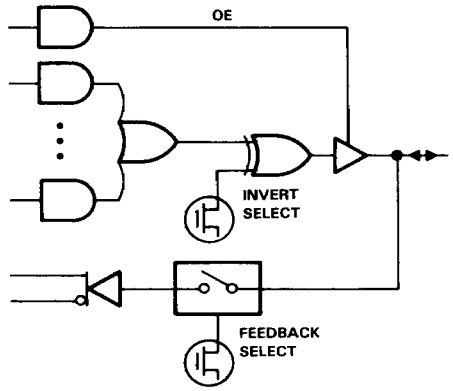
Figure 3 shows the EP910 basic output configurations. Along with combinational output, 4 register types are available. Each macrocell I/O may be independently configured. All registers have individual asynchronous-clear control from a dedicated product term. When the product term is asserted, the macrocell register will immediately be loaded with a zero independently of the clock. On power-up, the EP910 performs the clear function automatically.

In the combinational configuration, 8 product terms are ORed together to acquire the output signal. The invert-select EPROM bit controls output polarity and the output-enable buffer is product term controlled. The feedback-select multiplexer enables registered I/O (pin), feedback, or no feedback to the AND array.

When the D or T register is selected, 8 product terms are ORed together and made available to the register input. The invert select EPROM bit determines output polarity. The OE/CLK select multiplexer is used to configure the mode of operation to Mode 0 or Mode 1 (see Figure 2). The feedback-select multiplexer enables registered I/O (pin) or no feedback to the AND array.

If the JK or SR registers are selected, the 8 product terms are shared among two OR gates whose outputs feed the two primary register inputs. The allocation of product terms for each register input is optimized by the TI EPLD Development System. The invert select EPROM bit controls output polarity while the OE/CLK select multiplexer allows the mode of operation be Mode 0 or Mode 1. The feedback-select multiplexer enables registered I/O (pin) or no feedback to the AND array.

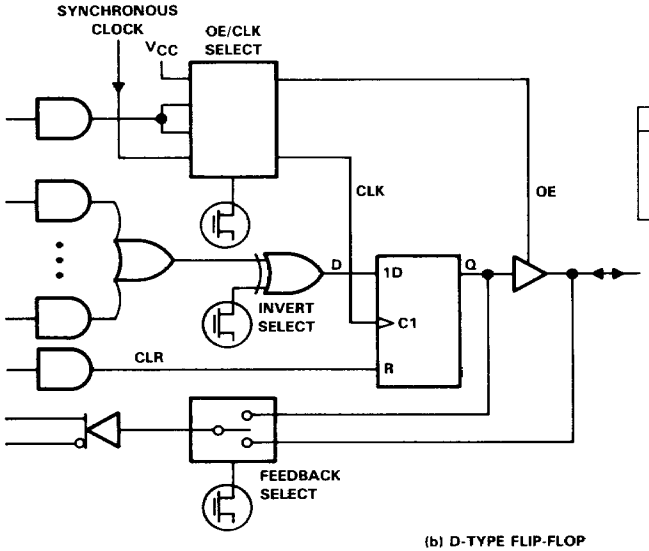
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the macrocell output buffer. In the erased state, I/O is configured for combinational active-low output with input (pin) feedback.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinational/high	Pin, None
Combinational/low	Pin, None
None	Pin

(a) COMBINATIONAL



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D Register/high	D Register, Pin, None
D Register/low	D Register, Pin, None
None	D Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L or H	X	Q_0
H	X	X	L

(b) D-TYPE FLIP-FLOP

FIGURE 3. I/O CONFIGURATIONS

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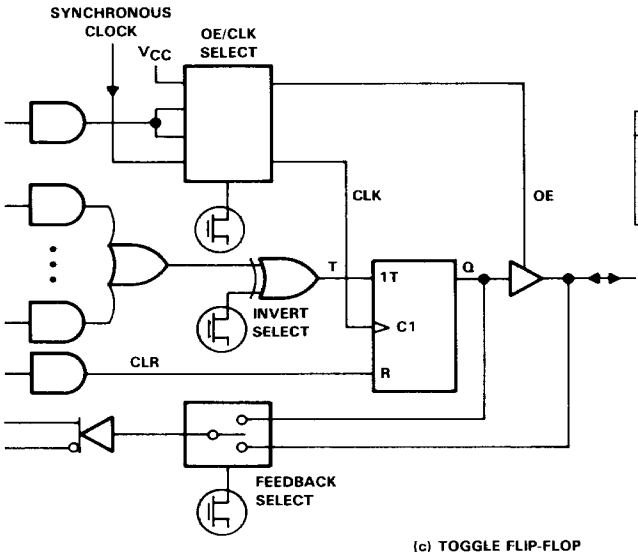


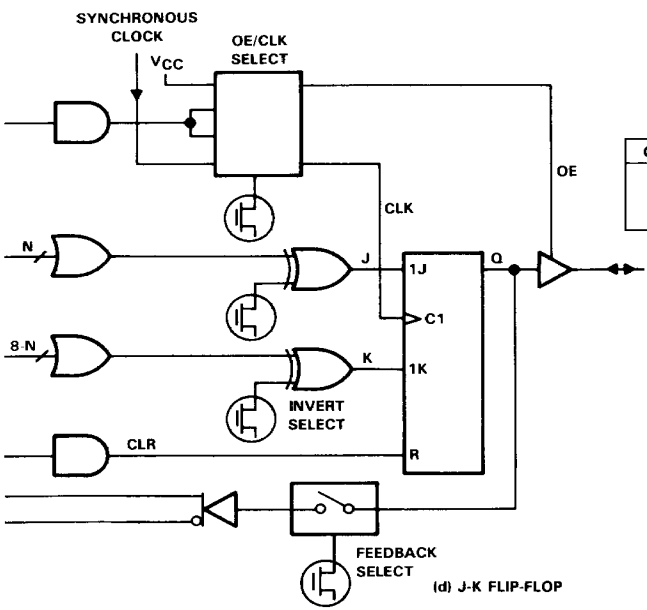
(c) TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T Register/high	T Register, Pin, None
T Register/low	T Register, Pin, None
None	T Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	T	Q
L	↑	L	Q_0
L	↑	H	$\overline{Q}_0$
L	L or H	X	Q_0
H	X	X	L



(d) J-K FLIP-FLOP

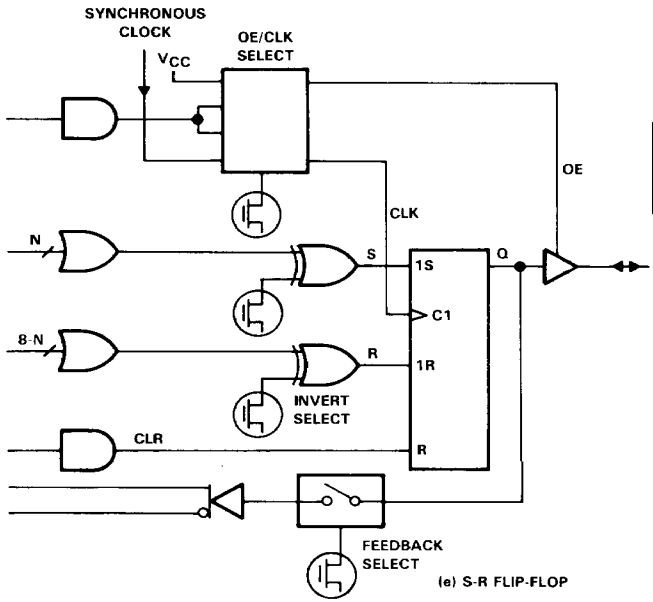
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	J	K	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	$\overline{Q}_0$
L	L or H	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/high	SR Register, None
SR Register/low	SR Register, None
None	SR Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	S	R	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	Undefined
L	L or H	X	X	Q_0
H	X	X	X	L

FIGURE 3. I/O CONFIGURATIONS (CONTINUED)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) . . . . . −2 V to 7 V
Programming supply voltage range, V_{pp} . . . . . −0.3 V to 13.5 V
Instantaneous programming supply voltage range, V_{pp} ($t \leq 20$ ns) . . . . . −2 V to 13.5 V
Input voltage range, V_I . . . . . −0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) . . . . . −2 V to 7 V
V_{CC} or GND current . . . . . −250 mA to 250 mA
Power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1200 mW
Operating free-air temperature, T_A . . . . . −65°C to 135°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 144 mW at 135°C at the rate of 9.6 mW/°C.

recommended operating conditions

PARAMETER			EP910I		EP910C		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
t_r	Rise time	CLK input		50		100	ns
		Other inputs		50		100	
t_f	Fall time	CLK input		50		100	ns
		Other inputs		50		100	
T_A	Operating free-air temperature		−40	85	0	70	°C

Note 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		EP910I			EP910C			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	TTL	I_{OH} = −4 mA		2.4			2.4			V
		CMOS	I_{OH} = −2 mA		3.84			3.84			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.45			0.45	V
I_I	Input current		V_I = V_{CC} or GND				±10			±10	µA
I_{OZ}	Off-state output current		V_O = V_{CC} or GND				±10			±10	µA
I_{CC}	Supply current	Standby	V_I = V_{CC} or GND, No load	See Note 4		0.02	0.15		0.02	0.1	mA
		Non-turbo		See Note 5		6	30		6	20	
		Turbo		See Note 5		45	100		45	80	
C_i	Input capacitance		V_I = 0, f = 1 MHz, T_A = 25°C				20			20	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz, T_A = 25°C				20			20	pF
C_{clk}‡	Clock capacitance		V_I = 0, f = 1 MHz, T_A = 25°C				20			20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ During programming, the clock capacitance of CLK2 is 60 pF maximum.
NOTES: 4. When in the non-turbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with device programmed as a 16-bit counter, and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER†		TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output	C_L = 35 pF		30		35		40	ns
t_{pd2}	I/O input to nonregistered output			33		38		43	ns
t_{PZX}	Input to output enable			30		35		40	ns
t_{PXZ}	Input to output disable	C_L = 5 pF, See Note 6		30		35		40	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		33		38		43	ns
t_{io}	I/O input buffer delay			3		3		3	ns

combinational mode, turbo bit off

PARAMETER†		TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output	C_L = 35 pF		60		65		70	ns
t_{pd2}	I/O input to nonregistered output			63		68		73	ns
t_{PZX}	Input to output enable			60		65		70	ns
t_{PXZ}	Input to output disable	C_L = 5 pF, See Note 6		60		65		70	ns
t_{clr}	Asynchronous output clear time	C_L = 35 pF		63		68		73	ns
t_{io}	I/O input buffer delay			3		3		3	ns

synchronous clock mode

PARAMETER†		TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	See Note 7	41.7		37		32.3		MHz
t_{co1}	Clock to output delay time			18		21		24	ns
t_{cnt}	Minimum clock period (register feedback to register output)	See Note 5		30		35		40	ns
f_{cnt}	Maximum frequency with feedback	See Note 5	33.3		28.6		25		MHz

asynchronous clock mode

PARAMETER†			TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency		See Note 7	33.3		31.3		29.4		MHz
t_{aco1}	Clock to output delay time	Turbo bit on			33		38		43	ns
		Turbo bit off			63		68		73	
t_{acnt}	Minimum clock period (register feedback to register output)				30		35		40	ns
f_{cnt}	Maximum frequency with feedback			33.3		28.6		25		MHz

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 5. These parameters are measured with device programmed as a 16-bit counter, and f = 1 MHz.
6. This is for an output voltage change of 500 mV.
7. The f_{max} values shown represent the highest frequency of operation without feedback.

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timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode

PARAMETER†			TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Input setup time	Turbo bit on		24		27		31		ns
		Turbo bit off		54		57		61		
t_h	Input hold time			0		0		0		ns
t_{ch}	Clock high pulse duration			12		13		15		ns
t_{cl}	Clock low pulse duration			12		13		15		ns

asynchronous clock mode

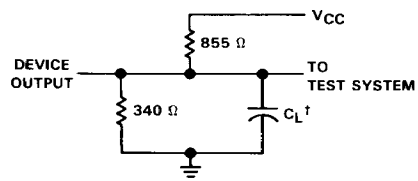
PARAMETER†			TEST CONDITIONS	EP910-30		EP910-35		EP910-40		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{asu}	Input setup time	Turbo bit on		10		10		10		ns
		Turbo bit off		40		40		40		
t_{ah}	Input hold time			15		15		15		ns
t_{ach}	Clock high pulse duration			15		16		17		ns
t_{acl}	Clock low pulse duration			15		16		17		ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

functional testing

The EP910 is functionally tested including complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP910 allows test program patterns to be used and then erased.

Figure 4 shows the dynamic test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurments, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast-ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.



†Includes jig capacitance

FIGURE 4. DYNAMIC TEST CIRCUIT

design security

The EP910 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

turbo bit

Some EPLDs contain a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set using the TI EPLD Development System. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low power) mode is shown in Figure 5. All dynamic parameters are tested with the turbo bit on. Figure 6 shows the relationship between the output drive currents and the corresponding output voltages.

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SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

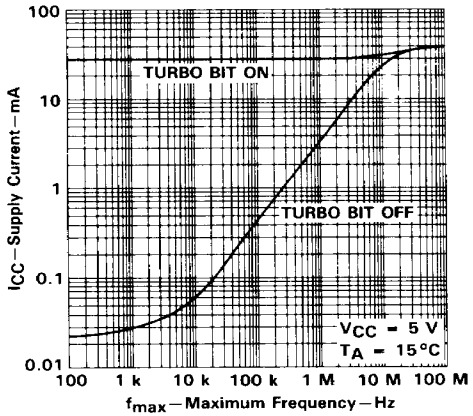


FIGURE 5

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

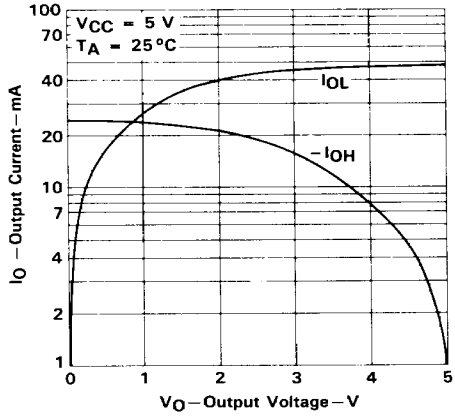
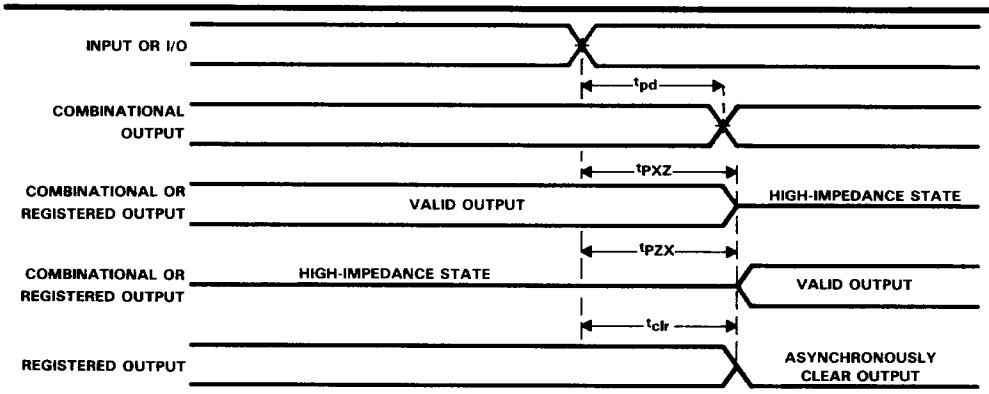
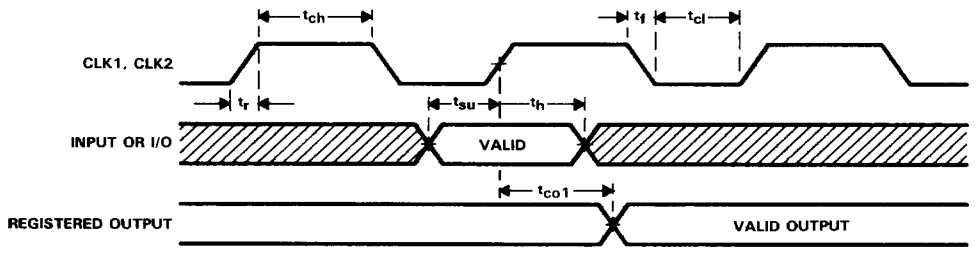


FIGURE 6

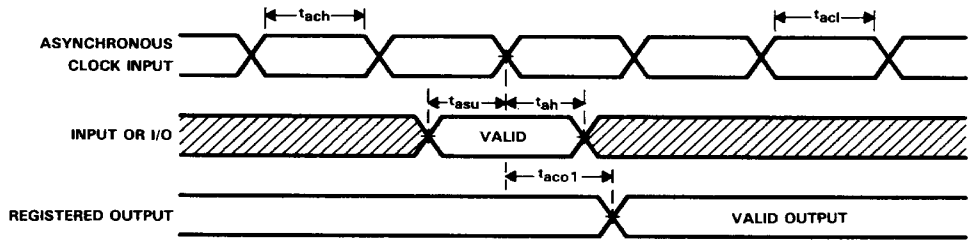
If the design requires low-power operation, the turbo bit should be (disabled) off. When operating in this mode, some dynamic parameters are subject to increases.



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE



(c) ASYNCHRONOUS CLOCK MODE

FIGURE 7. SWITCHING WAVEFORMS

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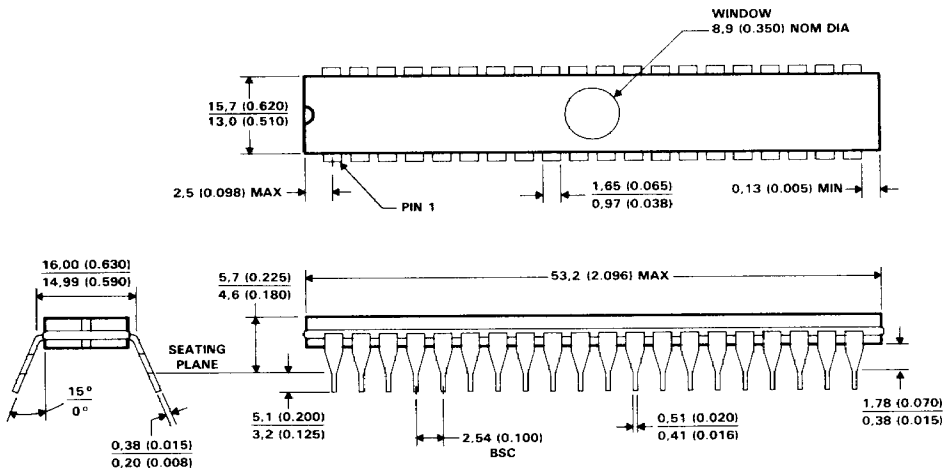
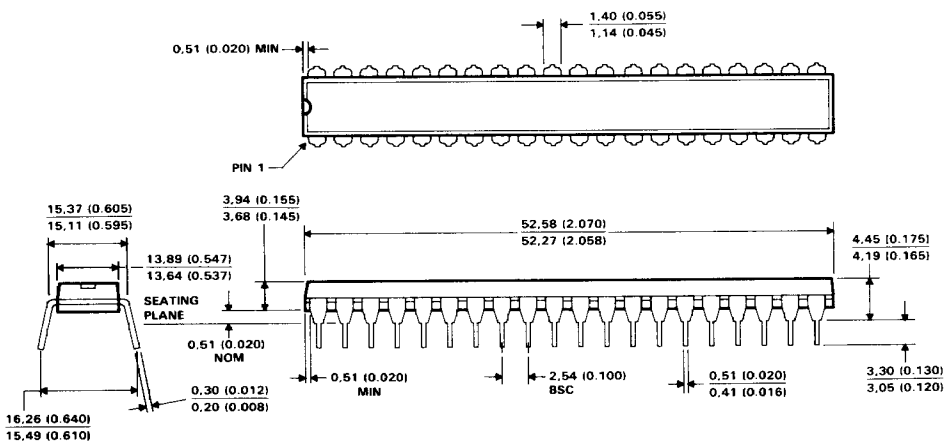
MECHANICAL DATA

40-PIN CERAMIC DIP (CDIP)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

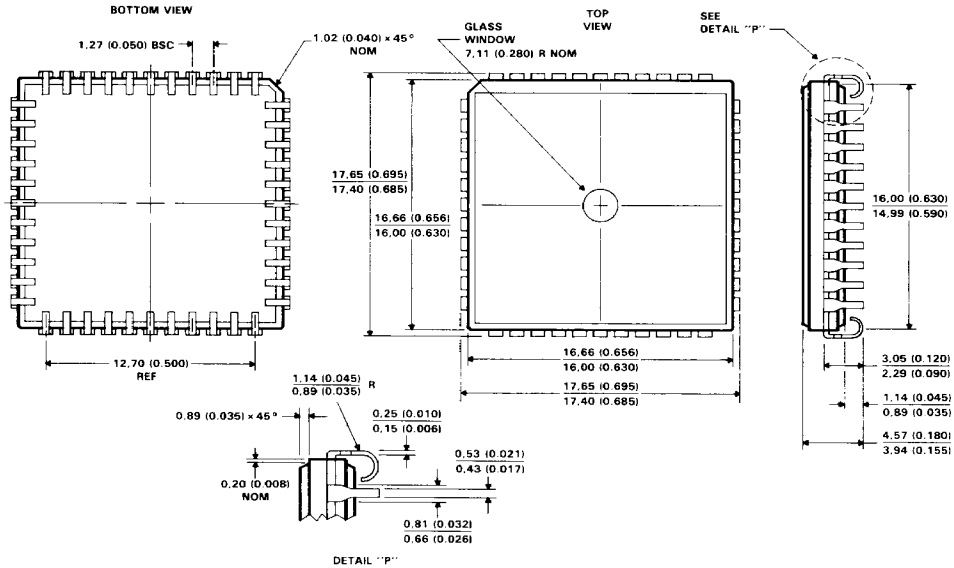
40-PIN PLASTIC DIP (PDIP)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

44-PIN CERAMIC LEADED CHIP CARRIER (CLCC)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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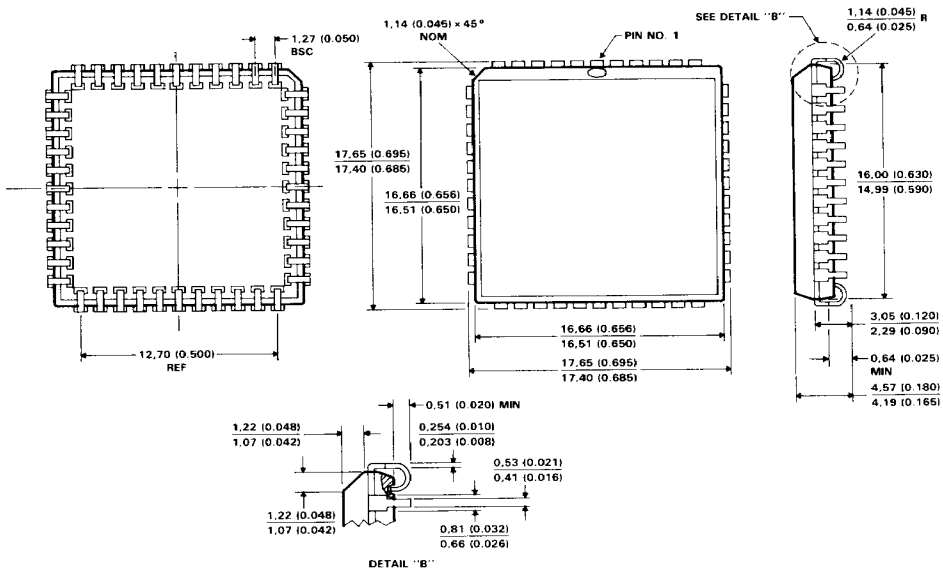
MECHANICAL DATA

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES