

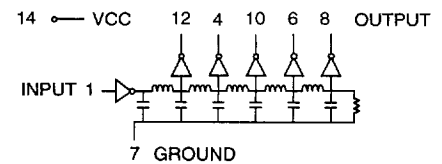
14 Pin DIL 5 Tap TTL Compatible Active Delay Lines

TAP DELAYS ±5% or 2 nS†	TOTAL DELAYS ±5% or 2 nS†	PART NUMBER	TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER
5, 10, 15, 20	25	EP9810-25	80, 160, 240, 320	400	EP9810-400
6, 12, 18, 24	30	EP9810-30	84, 168, 252, 336	420	EP9810-420
7, 14, 21, 28	35	EP9810-35	88, 176, 264, 352	440	EP9810-440
8, 16, 24, 32	40	EP9810-40	90, 180, 270, 360	450	EP9810-450
9, 18, 27, 36	45	EP9810-45	94, 188, 282, 376	470	EP9810-470
10, 20, 30, 40	50	EP9810-50	100, 200, 300, 400	500	EP9810-500
12, 24, 36, 48	60	EP9810-60	110, 220, 330, 440	550	EP9810-550
15, 30, 45, 60	75	EP9810-75	120, 240, 360, 480	600	EP9810-600
20, 40, 60, 80	100	EP9810-100	130, 260, 390, 520	650	EP9810-650
25, 50, 75, 100	125	EP9810-125	140, 280, 420, 560	700	EP9810-700
30, 60, 90, 120	150	EP9810-150	150, 300, 450, 600	750	EP9810-750
35, 70, 105, 140	175	EP9810-175	160, 320, 480, 640	800	EP9810-800
40, 80, 120, 160	200	EP9810-200	170, 340, 510, 680	850	EP9810-850
45, 90, 135, 180	225	EP9810-225	180, 360, 540, 720	900	EP9810-900
50, 100, 150, 200	250	EP9810-250	190, 380, 570, 760	950	EP9810-950
60, 120, 180, 240	300	EP9810-300	200, 400, 600, 800	1000	EP9810-1000
70, 140, 210, 280	350	EP9810-350			

† Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.

DC Electrical Characteristics		Test Conditions		Min	Max	Unit
V _{OH}	High-Level Output Voltage	V _{CC} = min. V _{IL} = max. I _{OH} = max	2.7			V
V _{OL}	Low-Level Output Voltage	V _{CC} = min. V _{IH} = min. I _{OL} = max		0.5		V
V _{IK}	Input Clamp Voltage	V _{CC} = min. I _I = I _{IK}		-1.2		V
I _{IH}	High-Level Input Current	V _{CC} = max. V _{IN} = 2.7V		50		µA
		V _{CC} = max. V _{IN} = 5.25V		1.0		mA
I _{IL}	Low-Level Input Current	V _{CC} = max. V _{IN} = 0.5V		-2		mA
I _{OS}	Short Circuit Output Current	V _{CC} = max. V _{OUT} = 0.	-40	-100		mA
		(One output at a time)				
I _{CC}	High-Level Supply Current	V _{CC} = max. V _{IN} = OPEN		75		mA
I _{CCL}	Low-Level Supply Current	V _{CC} = max. V _{IN} = 0		75		mA
T _{RO}	Output Rise Time	T _d ≤ 500 nS (0.75 to 2.4 Volts)		4		nS
		T _d > 500 nS		5		nS
N _H	Fanout High-Level Output	V _{CC} = max. V _{OH} = 2.7V		20	TTL LOAD	
N _L	Fanout Low-Level Output	V _{CC} = max. V _{OL} = 0.5V		10	TTL LOAD	

Schematic

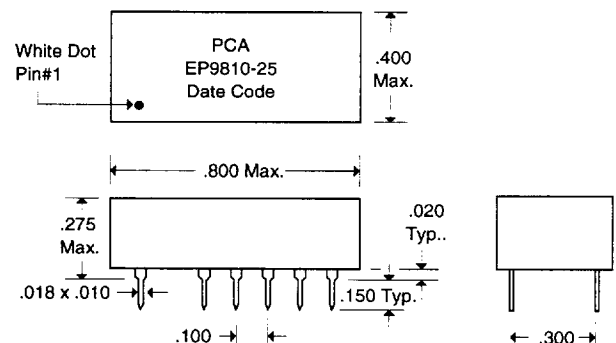


Recommended Operating Conditions		Min	Max	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High-Level Input Voltage	2.0		V
V _{IL}	Low-Level Input Voltage		0.8	V
I _{IK}	Input Clamp Current		-18	mA
I _{OH}	High-Level Output Current		-1.0	mA
I _{OL}	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T _A	Operating Free-Air Temperature	0	+70	°C

*These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C			Unit
E _{IN}	Pulse Input Voltage	3.2	Volts
PW	Pulse Width % of Total Delay	110	%
T _{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P _{RR}	Pulse Repetition Rate @ T _d ≤ 200 nS	1.0	MHz
	Pulse Repetition Rate @ T _d > 200 nS	100	KHz
V _{CC}	Supply Voltage	5.0	Volts

Package Dimensions



DSD9810 Rev. A 2/5/96

6852109 0000585 600

QAF-CS01 Rev. B 8/25/94

Unless Otherwise Noted Dimensions in Inches

Tolerances:

Fractional = ± 1/32

26 .XX = ± .030 .XXX = ± .010



16799 SCHOENBORN ST.
NORTH HILLS, CA 91343
TEL: (818) 892-0761
FAX: (818) 894-5791