Configuration EPROMs for FLEX Devices

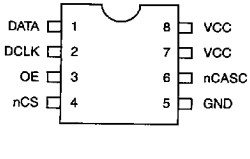
June 1996, ver. 5 — Data Sheet

Features

- Serial EPROM family for configuring FLEX devices
- Simple, easy-to-use 4-pin interface to FLEX devices
- Low current during configuration and near-zero standby current
- 5.0-V and 3.3-V operation
- Software design support with Altera's MAX+PLUS II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from Data I/O and other manufacturers
- Available in compact, one-time-programmable (OTP) plastic packages (see Figure 1)
  - 8-pin plastic dual in-line package (PDIP)
  - 20-pin plastic J-lead chip carrier package (PLCC)
  - 32-pin plastic thin quad flat pack (TQFP)

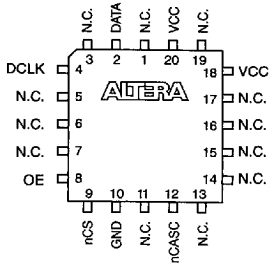
Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



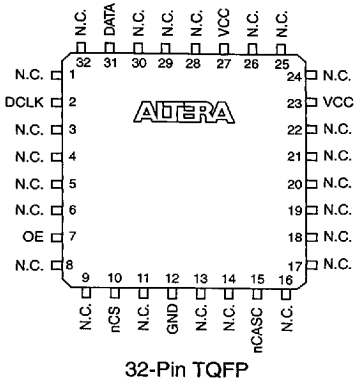
8-Pin PDIP

EPC1
EPC1V
EPC1064
EPC1064V
EPC1213



20-Pin PLCC

EPC1
EPC1V
EPC1064
EPC1064V
EPC1213



32-Pin TQFP

EPC1064
EPC1064V

Functional Description

In SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is needed. Altera's serial Configuration EPROMs store configuration data for SRAM-based Altera FLEX devices. Table 1 lists the Configuration EPROMs provided by Altera.

Table 1. Configuration EPROMs

Device	Description
EPC1	1,046,496 × 1 bit device with 5.0-V operation
EPC1V	1,046,496 × 1 bit device with 3.3-V operation
EPC1064	65,536 × 1 bit device with 5.0-V operation
EPC1064V	65,536 × 1 bit device with 3.3-V operation
EPC1213	212,942 × 1 bit device with 5.0-V operation

Table 2 shows the appropriate Configuration EPROM for each FLEX device.

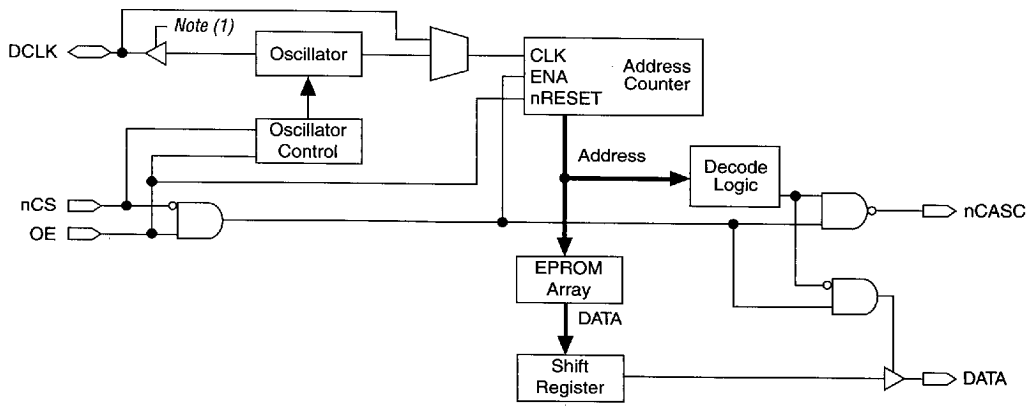
Table 2. Appropriate Configuration EPROM for Each FLEX Device

FLEX Device	Configuration EPROM
EPF10K10	EPC1
EPF10K20	EPC1
EPF10K30	EPC1
EPF10K40	EPC1
EPF10K50	EPC1
EPF10K70	EPC1
EPF10K100	Two EPC1 devices
EPF8282A	EPC1 or EPC1064
EPF8282AV	EPC1V or EPC1064V
EPF8452A	EPC1 or EPC1064
EPF8636A	EPC1 or EPC1213
EPF8820A	EPC1 or EPC1213
EPF81188A	EPC1 or EPC1213
EPF81500A	EPC1 or two EPC1213 devices

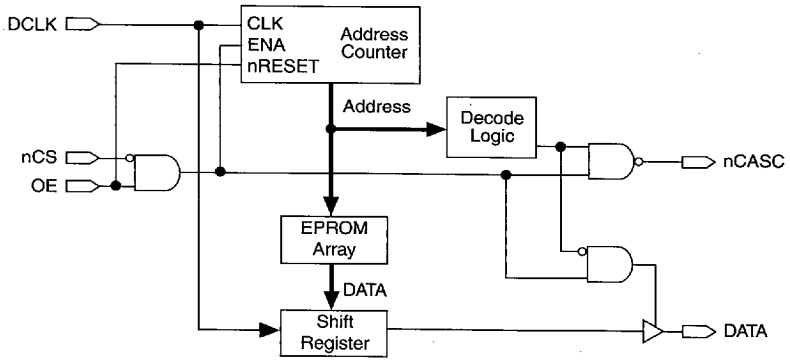
Figure 2 shows block diagrams of the Configuration EPROM devices.

Figure 2. Configuration EPROM Block Diagram

EPC1



EPC1064 & EPC1213



Note:

(1) This output enable controls the operation of the DCLK pin on the EPC1 device. The operation of the DCLK pin is determined by the configuration mode programmed into the EPC1 device.

Device Configuration

The control signals for Configuration EPROMs—nCS, OE, and DCLK—interface directly to the FLEX device control signals. All FLEX devices can control the entire configuration process and retrieve data from the Configuration EPROM without requiring an external intelligent controller.

The configuration EPROM device's OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter (and the oscillator in the EPC1 device). When OE is driven low, the Configuration EPROM device resets the address counter and tri-states its DATA pin. For the EPC1, the device determines its operation mode and whether it should use FLEX 10K or FLEX 8000 protocols when OE is driven high again. The nCS pin controls timing. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and the DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

When the Configuration EPROM has driven out all of its data and nCASC is driven low, the device tri-states the DATA pin to avoid contention with other Configuration EPROMs. Upon power-up, the address counter is automatically reset.

FLEX 10K Device Configuration

FLEX 10K devices can be configured with the EPC1 Configuration EPROM. The EPC1 device stores configuration data in its EPROM array and clocks the data out serially with its internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The EPC1 device sends a serial bitstream of configuration data to its DATA pin, which is routed to the DATA0 input pin on the FLEX 10K device.

When configuration data for a FLEX 10K device exceeds the capacity of a single EPC1 device, multiple EPC1 devices can be linked together serially. When multiple EPC1 devices are required, the nCASC and nCS pins provide handshaking between the EPC1 devices. The position of an EPC1 device in a chain determines its operation. The first EPC1 device in the Configuration EPROM chain is powered up or reset with nCS low and is configured for FLEX 10K protocol. The first EPC1 device supplies all clock pulses to one or more FLEX 10K devices and to any downstream EPC1 devices during configuration. The first EPC1 device also provides the first stream of data to the FLEX 10K devices during multi-device configuration. Once this EPC1 device finishes sending configuration data, it drives its nCASC pin low, which drives the nCS pin of the next EPC1 device in the chain low, activating the next EPC1 device. The first EPC1 device clocks all subsequent EPC1 devices until configuration is complete. Once all configuration data is transferred and nCS is driven high by CONF_DONE on the FLEX 10K device, the first EPC1 device clocks 16 additional cycles to initialize the FLEX 10K device, and then goes into Zero-power (idle) state. If nCS is driven high before all configuration data is transferred, the nSTATUS pin is pulled low, indicating a configuration error.

All downstream EPC1 devices in the Configuration EPROM chain are powered up or reset when nCS goes high and the device is configured for FLEX 10K protocol. Downstream EPC1 devices are clocked by the first EPC1 device. Each downstream EPC1 supplies configuration data after its nCS pin is driven low by the previous EPC1 device's nCASC pin. This EPC1 device then activates the next EPC1 device in the configuration chain. An inactive downstream EPC1 device waits in a zero-power (idle) state.

Table 3 describes EPC1 and EPC1V pin functions during FLEX 10K device configuration.

Table 3. EPC1 & EPC1V Pin Functions during FLEX 10K Device Configuration

Pin Name	Pin Number		Pin Type	Description
	8-Pin PDIP	20-Pin PLCC		
DATA	1	2	Output	Serial data output.
DCLK	2	4	I/O	Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device (otherwise, in FLEX 10K master mode, the DCLK pin drives low.)
OE	3	8	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. In FLEX 10K mode, if this pin is low (reset), the internal oscillator becomes inactive and DCLK drives low.
nCS	4	9	Input	Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the EPC1 is reset with nCS low, the device initializes as the first device in a daisy-chain. If the EPC1 is reset with nCS high, the device initializes as a subsequent EPC1 device in the chain.
nCASC	6	12	Output	Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a daisy-chain of EPC1 devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK to clock data from the next EPC1 device in the chain.
GND	5	10	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	Power	Power pin.

FLEX 8000 Device Configuration

FLEX 8000 devices have internal oscillators that can provide a DCLK signal to the Configuration EPROM. The Configuration EPROM device sends configuration data out as a serial bitstream on the DATA output pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC and nCS pins provide handshaking between multiple Configuration EPROMs, allowing several linked Configuration EPROM devices to serially configure multiple FLEX devices. FLEX 8000 devices can be configured with the EPC1, EPC1064, or EPC1213 Configuration EPROMs.

Configuration with EPC1

The EPC1 can replace the EPC1064 and EPC1213 Configuration EPROMs, which are also used to configure FLEX 8000 devices. EPC1 devices automatically emulate the EPC1064 or EPC1213 when it is programmed with the appropriate Programmer Object File (**.pof**). When the EPC1 device is programmed with a POF, the FLEX 8000 device drives the EPC1 device's OE pin high and clocks the EPC1 device. One EPC1 device can store more configuration data than either the EPC1064 or EPC1213 device. Therefore designers can use one type of Configuration EPROM, the EPC1, for all FLEX devices.

Configuration with EPC1064 & EPC1213

FLEX 8000 device configuration with EPC1064 and EPC1213 Configuration EPROMs is described under "Device Configuration" on page 395. Table 4 describes the pin functions of the EPC1, EPC1213, and EPC1064 during FLEX 8000 device configuration.

Table 4. Configuration EPROM Pin Functions during FLEX 8000 Device Configuration

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP	20-Pin PLCC	32-Pin TQFP *Note (1)*		
DATA	1	2	31	Output	Serial data output.
DCLK	2	4	2	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	7	Input	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	15	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. The nCASC output is usually connected to the nCS input of the next Configuration EPROM in a daisy-chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	12	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	23, 27	Power	Power pin.

Note:
(1) EPC1064 and EPC1064V devices only.

Active serial (AS) and multi-device sequential active serial (MD-SAS) configuration schemes use an EPC1 Configuration EPROM as a data source for FLEX 8000 devices.

For information on FLEX 10K and FLEX 8000 devices and how to configure them, see the following documents:

- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *FLEX 8000 Programmable Logic Device Family Data Sheet*
- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. The MAX+PLUS II software automatically generates a Programmer Object File (**.pof**) for every Configuration EPROM in a project. In a multi-device project, MAX+PLUS II can combine the programming files for multiple FLEX devices into one or more Configuration EPROMs. MAX+PLUS II allows you to select the appropriate Configuration EPROM to most efficiently store the data for each FLEX device.

The POF includes a preamble, cyclic redundancy code (CRC), and synchronization data that allow it to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with MAX+PLUS II and a Configuration EPROM programming adapter. Many programming hardware manufacturers, including Data I/O, support programming of Configuration EPROMs.

For more information on programming hardware, see the *Altera Programming Hardware Data Sheet* and *Programming Hardware Manufacturers* in this data book.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND *Note (2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V device		4.75	5.25	V
	Supply voltage for 3.3-V device		3.0	3.6	V
V_I	Input voltage	With respect to GND, *Note (2)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V device high-level TTL output voltage	I_{OH} = –4 mA DC, *Note (5)*	2.4		V
	3.3-V device high-level TTL output voltage	I_{OH} = –0.1 mA DC, *Note (5)*	V_{CC} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (5)*		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10	10	µA

EPC1064, EPC1064V & EPC1213 Device I_{CC} Supply Current Values *Note (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 6 MHz		10		mA

EPC1 & EPC1V Device I_{CC} Supply Current Values *Note (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 10 MHz		10	50	mA

Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

FLEX 10K Device Configuration Timing Parameters Using EPC1 *Note (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				200	ns
t_{OEZX}	OE high to data output enabled				160	ns
t_{CO}	DCLK to data out delay				30	ns
t_{MCH}	DCLK high time in master mode		30	50		ns
t_{MCL}	DCLK low time in master mode		30	50		ns
t_{SCH}	DCLK high time in slave mode		30			ns
t_{SCL}	DCLK low time in slave mode		30			ns
t_{CASC}	CLK rising edge to nCASC				20	ns
t_{CCA}	nCS to nCASC cascade delay				10	ns
t_{CDOE}	CLK to data enable/disable				30	ns
t_{OEC}	OE low to CLK disable delay				45	ns
t_{OH}	DATA hold from CLK rising edge		0		10	ns
t_{NRCAS}	OE low (reset) to nCASC delay				25	ns
t_{NRR}	OE low time (reset) minimum		100			ns

FLEX 8000 Device Configuration Timing Parameters Using EPC1, EPC1V, EPC1064, EPC1064V & EPC1213

			EPC1064V		EPC1064 EPC1213		EPC1 *Note (6)*		EPC1V *Note (6)*		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OEZX}	OE high to DATA output enabled			75		50		50			ns
t_{CSZX}	nCS low to DATA output enabled			75		50		50			ns
t_{CSXZ}	nCS high to DATA output disabled			75		50		50			ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		50				ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		0				ns
t_{DSU}	Data setup time before rising edge on DCLK, *Note (8)*		75		50		50				ns
t_{DH}	Data hold time after rising edge on DCLK, *Note (8)*		0		0		0				ns
t_{CO}	DCLK to DATA out delay, *Note (6)*			100		75		75			ns
t_{CK}	Clock period		240		160		100				ns
f_{CK}	Clock frequency			4		6		10			MHz
t_{CL}	DCLK low time		120		80		50				ns
t_{CH}	DCLK high time		120		80		50				ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50		50			ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		100				ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60		50			ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50		50			ns
t_{CEOUT}	nCS high to nCASC high delay			150		100		100			ns

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for $T_A = 25°$ C and $V_{CC} = 5.0$ V.
(4) Operating conditions: $V_{CC} = 5.0$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 5.0$ V ± 10%, $T_A = -40°$ C to 85° C for industrial use.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Parameters for EPC1 devices are preliminary. Contact Altera Applications for information on EPC1V devices.
(7) Capacitance is sample-tested only.
(8) This parameter applies to FLEX 8000 devices.