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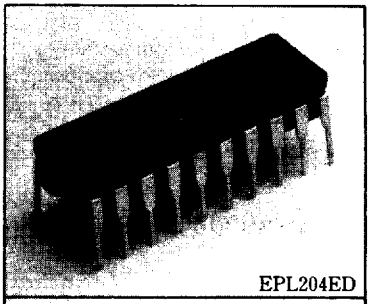
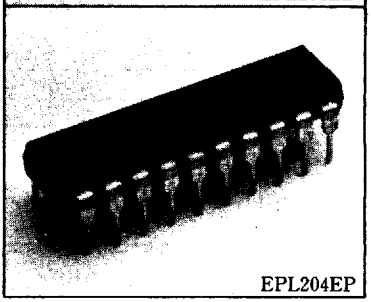
# EPL204ED/EP

## CMOS ELECTRICALLY PROGRAMMABLE LOGIC



EPL204ED



EPL204EP

## ■ OUTLINE

The EPL204 is a field programmable logic array manufactured by using CMOS EPROM processes. It is a programmable "and" fixed "or" array with registered outputs in the 26P8 configuration.

Programming is possible with popular PAL® programmers such as Data I/O or Ricoh's IBM P.C. Writer. Programming is similar to all EPROM Devices. Development of CMOS Gate Arrays using one or more of those devices to support larger I/O's is simple and immediate using off the shelf plastic OTP (One Time Programmable) devices.

Input/Output configurations are flexible using 8 programmable macro cells. Feedback, combinatorial or registered outputs and polarity are user definable. Register clocks can be from the internal array or on the conventional external Pin 1 clock terminal.

## ■ FEATURES

- Low power consumption and high reliability characteristics of the CMOS-EPROM process
- 20 Pin DIP Plastic OTP (EPL 204EP 300 mil) 20 Pin Window DIP with window (EPL 204ED 300 mil)
- Ultra Violet Reprogramming with window packages – 1000 reprogram cycles
- Data copy protection
- Input/Output propagation delay 25ns maximum
- Flexible I/O capability using I/O macro cells
  - A. Selection of combinational or registered outputs
  - B. Selection of output enable (External $\overline{OE}$, Internal OE)
  - C. Polarity of outputs
  - D. Clock selection (external or internal)
  - E. Asynchronous resets (AR1, AR2)
  - F. Synchronous presets (SP1, SP2)

## ■ ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Condition | Rating | Unit |
|---|---|---|---|---|
| Vcc | Vcc Supply Voltage | with respect to GND | −0.3 ~ 7.0 | V |
| Vpp | Vpp Supply Voltage | | −0.3 ~ 14.5 | V |
| Vi | Input Voltage | | −0.3 ~ Vcc + 0.3 | V |
| Vo | Output Voltage | | −0.3 ~ Vcc + 0.3 | V |
| Pd | Maximum Power Consumption | Ta = 25°C | 0.8 | W |
| Topr | Operating Ambient Temperature | | −20 ~ 85 | °C |
| Tstg | Storage Temperature | | −40 ~ 125 | °C |

## ■ RECOMMENDED OPERATING CONDITION (Ta = 0 ~ 70°C)

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vcc | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | "H" Input Voltage | 2.0 | | Vcc + 0.3 | V |
| $V_{IL}$ | "L" Input Voltage | −0.3 | | 0.8 | V |

## ■ CAPACITANCE

| Symbol | Parameter | Condition | Specified Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| | Input Pin | f = 1 MHz, Vcc = 0V | | 5 | | pF |
| | I/O Pin | | | 8 | | |
| | Vpp Pin | | | 10 | | |

## ■ D.C. CHARACTERISTICS (Ta = −20 ~ 85°C Vcc = 5V ± 5%)

| Symbol | Parameter | Condition | Specified Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $I_{LI}$ | Input Leakage Current | Vin = 0V ~ Vcc | −20 | | 20 | μA |
| $I_{LO}$ | Output Leakage Current for OFF State | Vo = 0V ~ Vcc | −20 | | 20 | μA |
| $V_{IL}$ | "L" Input Voltage | | −0.3 | | 0.8 | V |
| $V_{IH}$ | "H" Input Voltage | | 2.0 | | Vcc + 0.3 | V |
| $V_{OL}$ | "L" Output Voltage | Vcc = MIN $I_{OL}$ = 8 mA | | | 0.5 | V |
| $V_{OH}$ | "H" Output Voltage | Vcc=MIN $I_{OH}$=−3.2mA | 2.4 | | | V |
| $Icc_1$ | Power Supply Current (Standby) | Vcc = MAX f = 0 MHz Vin = GND or Vcc | | | 60 | mA |
| $Icc_2$ | Power Supply Current (Operation) | Vcc = MAX f = 10 MHz Vin = GND or Vcc | | | 70 | mA |

## ■ AC CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 5V ± 5%)

| Symbol | 項 Parameter 目 | | Condition | Specified Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | Clock | Parameters | | Min | Typ | Max | |
| $t_{PD}$ | | Input or I/O input to non-registered output | | | | 25 | nS |
| $t_{PIX}$ | | Input or I/O input to output disable | | | | 25 | nS |
| $t_{PIZ}$ | | Input or I/O input to output enable | | | | 25 | nS |
| $t_{PXZ}$ | | /OE (pin 11) to output disable | CL=50pF | | | 20 | nS |
| $t_{PZX}$ | | /OE (pin 11) to output enable | | | | 20 | nS |
| $t_{SU1}$ | | Input or I/O input setup time | | 18 | | | nS |
| $t_{H1}$ | External | Input or I/O input hold time | R1=560Ω | 0 | | | nS |
| $t_{CLK1}$ | Clock | Clock to output delay | | | | 15 | nS |
| $t_{FPD1}$ | | Clock to non-registered output from registered feed back | R2=1.1KΩ | | | 35 | nS |
| $t_{W1}$ | | External clock width | | 15 | | | nS |
| $t_{PS1}$ | CLK (1pin) | Synchronous preset input setup time | | 18 | | | nS |
| $t_{SET1}$ | | Clock to register preset | | | | 15 | nS |
| $t_{RST}$ | | Input or I/O input to asynchronous reset | | | | 25 | nS |
| $t_{P1}$ | | Minimum clock period ($t_{SU1}+t_{CLK1}$) | | | | 33 | nS |
| $f_1$ | | Maximum frequency ($1/t_{P1}$) | | 30 | | | MHz |
| $t_{PH1}$ | | Synchronous preset input hold time | | 0 | | | nS |
| $t_{SU2}$ | Internal | Input or I/O input setup time | | 5 | | | nS |
| $t_{H2}$ | Clock | Input or I/O input hold time | | 10 | | | nS |
| $t_{CLK2}$ | | Clock P.T. input to output delay | | | | 30 | nS |
| $t_{FPD2}$ | CKPn (n=1~8) | Clock P.T. input to non-registered output from registered feed back | CL=50pF | | | 50 | nS |
| $t_{W2}$ | | Clock P.T. input width | | 15 | | | nS |
| $t_{PS2}$ | | Synchronous preset input set up time | R1=560Ω | 5 | | | nS |
| $t_{SET2}$ | | Clock P.T. input to register preset | R2=1.1KΩ | | | 30 | nS |
| $t_{P2}$ | | Minimum Clock period ($t_{SU2}+t_{CLK2}$) | | | | 35 | nS |
| $t_{PH2}$ | | Synchronous preset input hold time | | 10 | | | nS |
| $f_2$ | | Maximum frequency ($1/t_{P2}$) | | 28.6 | | | MHz |
| $t_{PON}$ | | Power on reset time | | 45 | | | μS |

## ■ TIMING CHART

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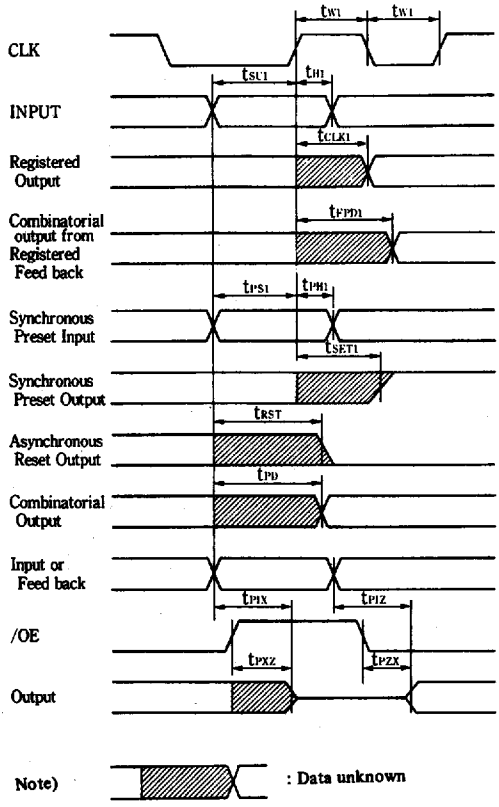
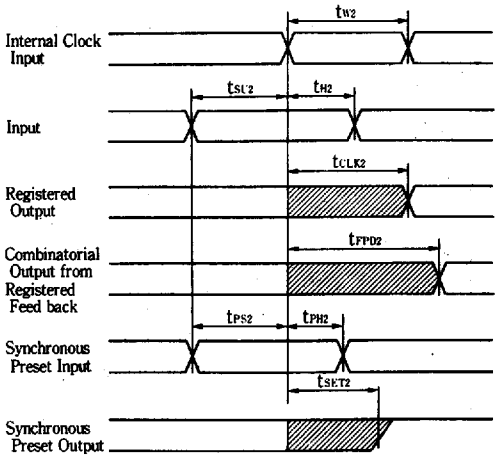
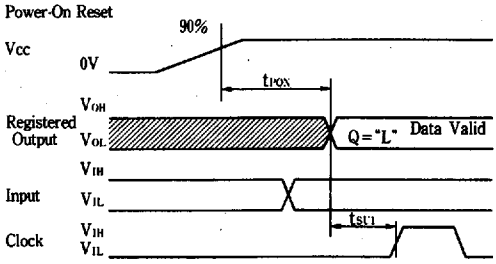
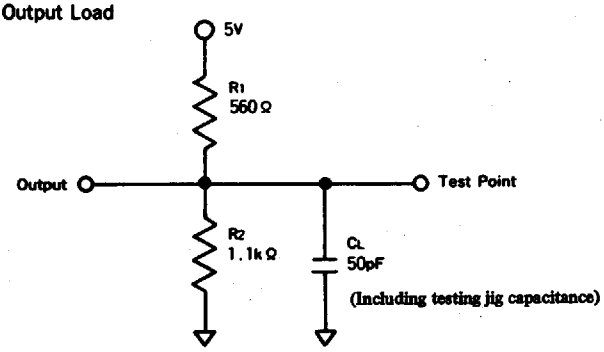


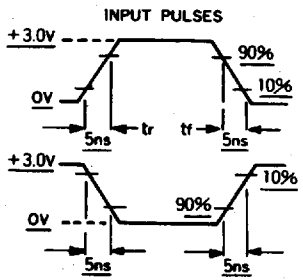




### Output Load




### Input Waveform




NOTE : This is the A.C. characteristic measurement with a voltage of 1.5V on both the input and output.

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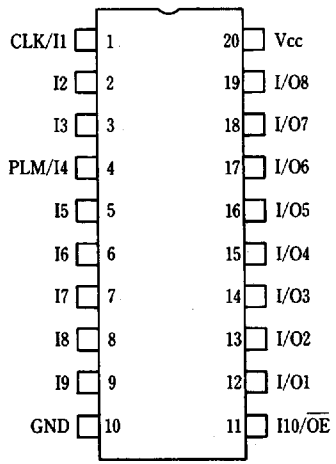
## ■ PIN DESCRIPTION

| PIN No. | PIN Name | | Function | | |
|---|---|---|---|---|---|
| | Logic Mode | Program Mode | Logic Mode | | Program Mode |
| 1 | CLK/I1 | Vpp | Input | Clock | Programing Power Supply |
| 2 | I2 | CA4 | | | Column Address Input |
| 3 | I3 | CA3 | | | |
| 4 | PLM/I4 | CA2 | | Pre-load | |
| 5 | I5 | CA1 | | | |
| 6 | I6 | CA0 | | | |
| 7 | I7 | RA5 | Input | | Row Address Input |
| 8 | I8 | RA4 | | | |
| 9 | I9 | NC | | | NC |
| 10 | GND | GND | GND | | GND |
| 11 | I10/$\overline{OE}$ | PGM/$\overline{OE}$ | Input/Output Enable | | Programming Control/Output Enable |
| 12 | I/O1 | D0 | Input/Output | | DATA Input/Output |
| 13 | I/O2 | D1 | | | |
| 14 | I/O3 | D2 | | | |
| 15 | I/O4 | D3 | | | |
| 16 | I/O5 | RA3 | | | Row Address Input |
| 17 | I/O6 | RA2 | | | |
| 18 | I/O7 | RA1 | | | |
| 19 | I/O8 | RA0 | | | |
| 20 | Vcc | Vcc | Vcc | | Vcc |

## ■ PIN CONFIGURATION



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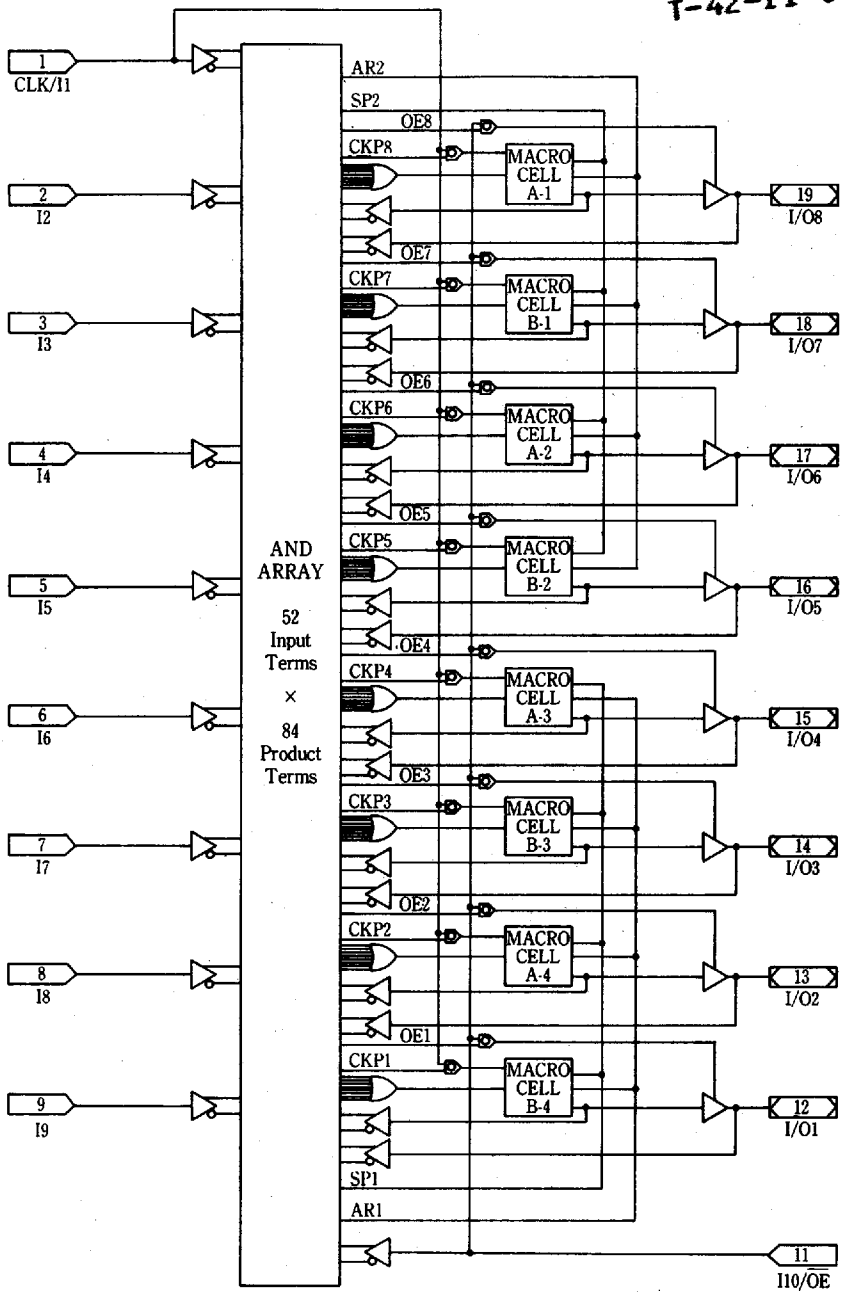
## ■ BLOCK DIAGRAM



## ■ MACRO I/O CELL

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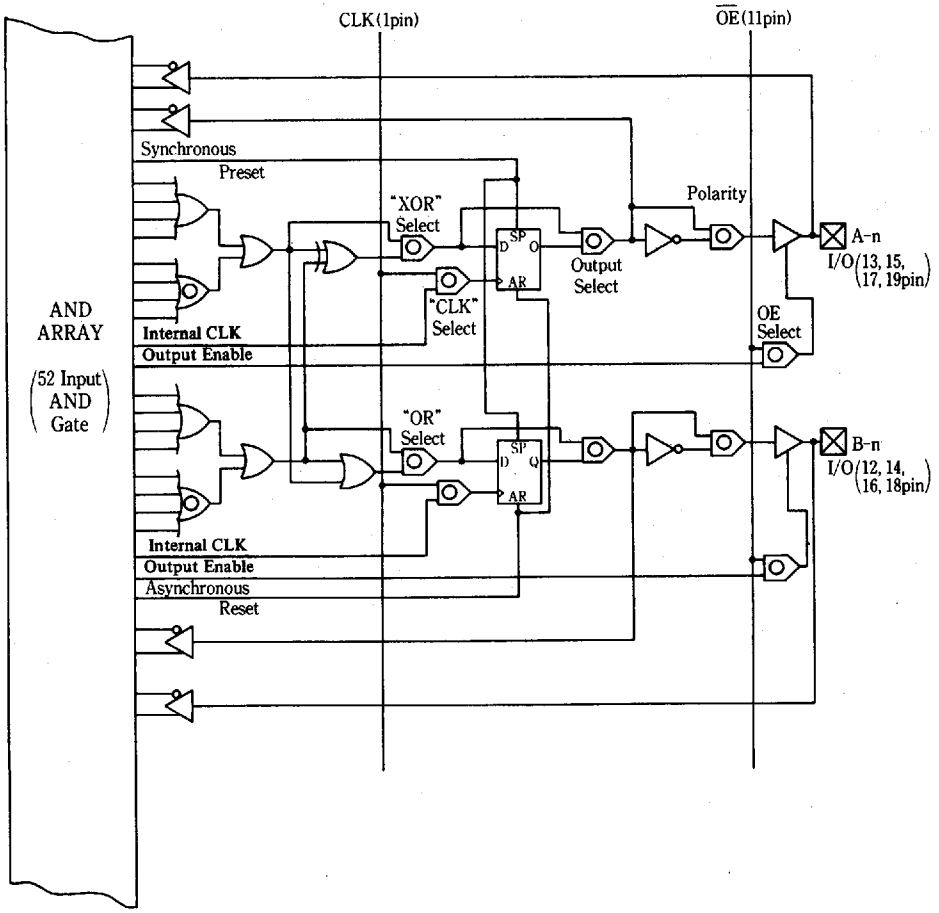

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## ■ FUNCTIONS AND OPERATIONS

The EPL204 is an electrically reprogrammable logic array. The configuration of the EPL204 is 52 input terms (18 external inputs and 8 feedbacks).

All inputs are TTL levels. Control of all registers for asynchronous and synchronous operation and output polarity is user definable.

All product terms and input terms to the "AND" array have ultra violet EPROM cells connections. In the unprogrammed state all intersections are connected.

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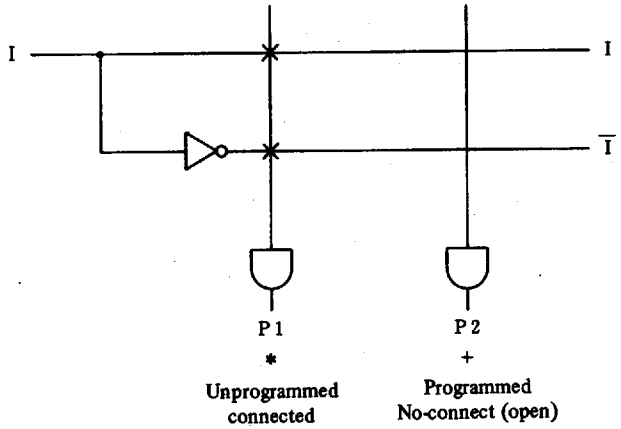


Fig. 1

All macro I/O cells have "XOR" or "OR" selections and output polarity selections.

**(1) "OR"/"XOR" select**

Eight product terms are ORed or XORed or fed straight through to each output.

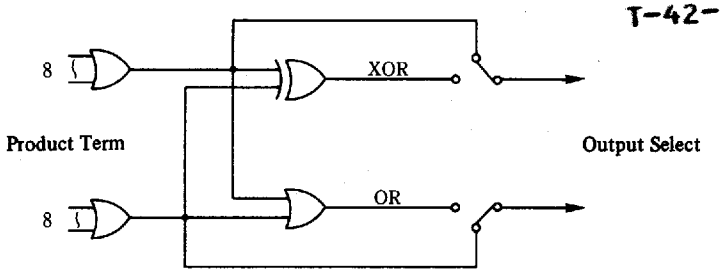


Fig. 2 "OR" "XOR" Select

**(2) OE select**

Each macro cell can be selected via pin 11 or from the internal product term.

**(3) Output select, CLK select**

CLK select of each macro cell register can be clocked from the conventional CLK (pin 1) or from an internal clock out of the array. Each register has a synchronous preset and an asynchronous reset.

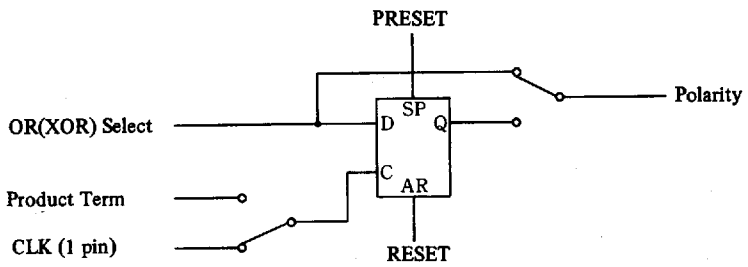


Fig. 3 Output Select, CLK Select

**(4) Polarity**

You can select the polarity of the output signal.

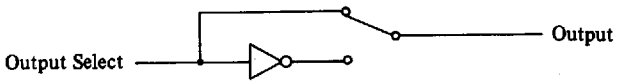


Fig. 4 Polarity

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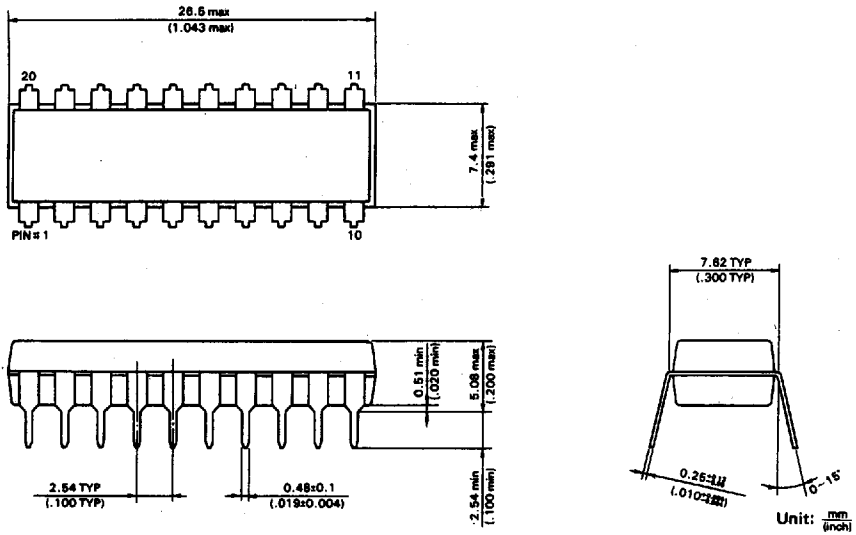
## ■ PACKAGE DIMENSION

- **Mold DIP Package**
  (DIP-20-P1)



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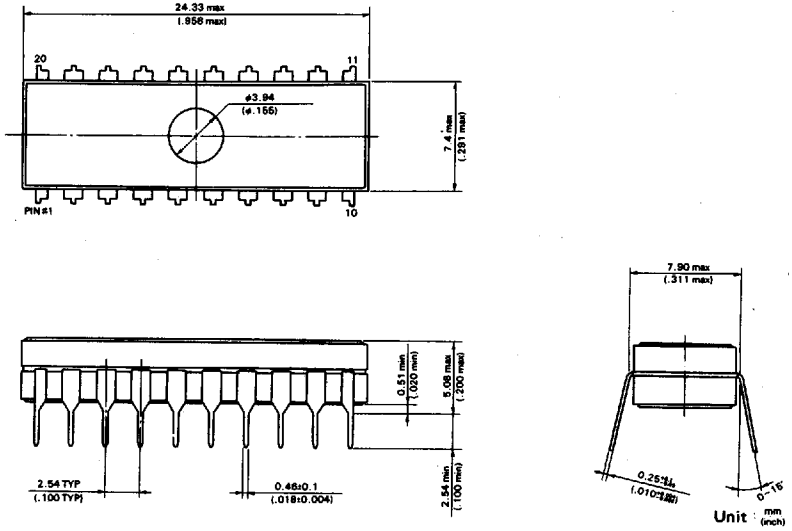
- **CER DIP Package**
  (DIP-20-G1)

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