Elan Microelectronics Crop.

EPL43102

43 COM / 102 SEG LCD DRIVER

September 7, 2001
Version 1.1

EPL43102 Specification Revision History		
Version	**Content**	**Date**
0.1	Initial version	November 20,2000
0.2	Add 1/3 , 1/3.5 bias	February 15,2001
0.3	1.Add one more one VDD and VSS pad 2.Modify Pad sequence and configuration	March 2,2001
0.4	1.Modify DC and AC characteristics	July 17,2001
0.5	1.Add pin configuration 2.Add program example 3.Modify DC characteristics	July 25,2001
1.1	Modify operating temperature range –30 to 80 ^{O}C	September 7, 2001

Contents

GENERAL DESCRIPTION

The EPL43102 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It can be interfaced to the MPU via serial or 8-bit interface. It contains 43 common and 102 segment driver circuits. With one chip, it is possible to drive a graphic display system with a maximum of 102 x 43 dots.

FEATURES

1. Direct Correspondence between Display Data RAM and LCD Pixel
2. Display Data RAM : 102 x 43 = 4386 bits
3. 145 LCD Drivers : 102-seg segment drivers, 42-common drivers and 1-icon
4. Serial Interface (SPI) or 8-Bit Parallel Interface Mode (80-series , 68-series MPU)
5. On-chip oscillator circuit
6. Multi-chip operation (Master, Slave) available
7. Programmable Duty Ratio :

Duty ratio	Common	Segment
1: 42 (+ ICON)	42 (+ ICON)	102
1: 36 (+ ICON)	36 (+ ICON)	102
1: 32 (+ ICON)	32 (+ ICON)	102
1: 24 (+ ICON)	24 (+ ICON)	102
1: 16 (+ ICON)	16 (+ ICON)	102
1: 8 (+ ICON)	8 (+ ICON)	102

NOTE: ICON: "1" → ICON pin enable;"0" → ICON pin disable

8. Selectable LCD driving bias level : 1/3,1/3.5,1/4,1/4.5,1/5,1/5.5,1/6,1/6.5,1/7,1/7.5,1/8 bias
9. Selectable LCD display clock frequency
10. Electronic contrast control functions (64 steps)
11. Built-in useful Instruction Set : Display data read/write, Display on/off, Inverse display, Page address set, Common address set, LCD display contrast control, Set Sleep mode, Standby mode….
12. Operating Voltage range :
    Supply voltage : 2.2 to 5.5 V
    LCD driving voltage : 4.0 to 15.0 V

APPLICATIONS

Organizer
Electronic Dictionary
Scientific calculator
Cellular phone
Graphic pager
Handy Terminals (PDA)
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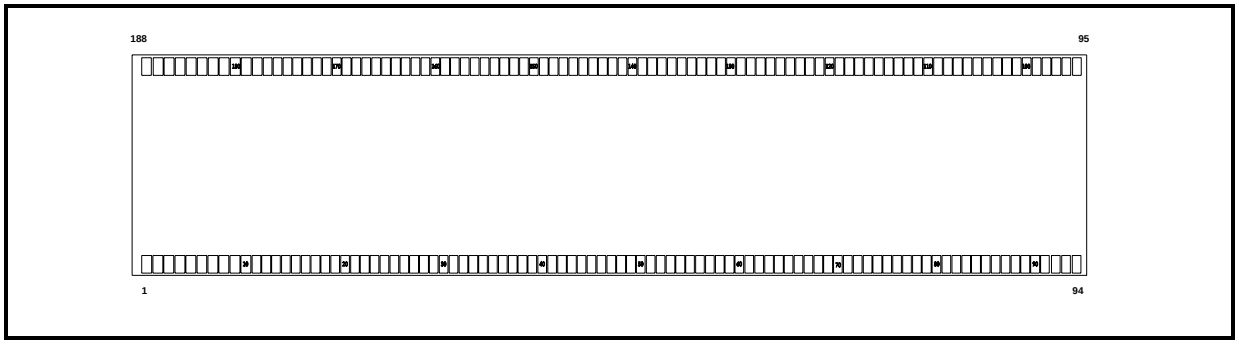
PIN ASSIGNMENT



PIN DIMENSIONS

Pad Size A : 85X150 μm^2 (Pad 1 to 15 and 80 to 94; Pad 95 to 109 and 174 to188)
Pad Size B : 75X150 (Pad 16 to 79; Pad 110 to 173)
Pad Pitch A: 95 μm
Pad Pitch B: 85 μm

Pad coordinates

PAD NO.	Symbol	X	Y
1	COM21	-4095.0	-742.5
2	COM22	-4000.0	-742.5
3	COM23	-3905.0	-742.5
4	COM24	-3810.0	-742.5
5	COM25	-3715.0	-742.5
6	COM26	-3620.0	-742.5
7	COM27	-3525.0	-742.5
8	COM28	-3430.0	-742.5
9	COM29	-3335.0	-742.5
10	COM30	-3240.0	-742.5
11	COM31	-3145.0	-742.5
12	COM32	-3050.0	-742.5
13	COM33	-2955.0	-742.5
14	COM34	-2860.0	-742.5
15	COM35	-2765.0	-742.5
16	COM36	-2675.0	-742.5
17	COM37	-2590.0	-742.5
18	COM38	-2505.0	-742.5
19	COM39	-2420.0	-742.5
20	COM40	-2335.0	-742.5
21	COM41	-2250.0	-742.5
22	COMI1	-2165.0	-742.5
23	VDD	-2080.0	-742.5
24	VDD	-1995.0	-742.5
25	C1+	-1910.0	-742.5
26	C1-	-1825.0	-742.5
27	C3	-1740.0	-742.5
28	C4	-1655.0	-742.5
29	C2-	-1570.0	-742.5
30	C2+	-1485.0	-742.5
31	VOUT	-1400.0	-742.5
32	V0	-1315.0	-742.5
33	V1	-1230.0	-742.5
34	V2	-1145.0	-742.5
35	V3	-1060.0	-742.5
36	V4	-975.0	-742.5
37	VR	-890.0	-742.5
38	GND	-805.0	-742.5
39	GND	-720.0	-742.5
40	MS	-635.0	-742.5
41	PS	-550.0	-742.5
42	FR	-465.0	-742.5
43	C86	-380.0	-742.5
44	/DOF	-295.0	-742.5
45	CLS	-210.0	-742.5
46	CL	-125.0	-742.5
47	OSC	-40.0	-742.5
48	FRS	45.0	-742.5
49	IRS	130.0	-742.5
50	/RES	215.0	-742.5

PAD NO.	Symbol	X	Y
51	D7	300.0	-742.5
52	D6	385.0	-742.5
53	D5	470.0	-742.5
54	D4	555.0	-742.5
55	D3	640.0	-742.5
56	D2	725.0	-742.5
57	D1	810.0	-742.5
58	D0	895.0	-742.5
59	CS2	980.0	-742.5
60	/CS1	1065.0	-742.5
61	A0	1150.0	-742.5
62	/WR	1235.0	-742.5
63	/RD	1320.0	-742.5
64	TEST	1405.0	-742.5
65	COM20	1490.0	-742.5
66	COM19	1575.0	-742.5
67	COM18	1660.0	-742.5
68	COM17	1745.0	-742.5
69	COM16	1830.0	-742.5
70	COM15	1915.0	-742.5
71	COM14	2000.0	-742.5
72	COM13	2085.0	-742.5
73	COM12	2170.0	-742.5
74	COM11	2255.0	-742.5
75	COM10	2340.0	-742.5
76	COM9	2425.0	-742.5
77	COM8	2510.0	-742.5
78	COM7	2595.0	-742.5
79	COM6	2680.0	-742.5
80	COM5	2770.0	-742.5
81	COM4	2865.0	-742.5
82	COM3	2960.0	-742.5
83	COM2	3055.0	-742.5
84	COM1	3150.0	-742.5
85	COM0	3245.0	-742.5
86	COMI2	3340.0	-742.5
87	SEG101	3435.0	-742.5
88	SEG100	3530.0	-742.5
89	SEG99	3625.0	-742.5
90	SEG98	3720.0	-742.5
91	SEG97	3815.0	-742.5
92	SEG96	3910.0	-742.5
93	SEG95	4005.0	-742.5
94	SEG94	4100.0	-742.5
95	SEG93	4100.0	742.5
96	SEG92	4005.0	742.5
97	SEG91	3910.0	742.5
98	SEG90	3815.0	742.5
99	SEG89	3720.0	742.5
100	SEG88	3625.0	742.5

PAD NO.	Symbol	X	Y
101	SEG87	3530.0	742.5
102	SEG86	3435.0	742.5
103	SEG85	3340.0	742.5
104	SEG84	3245.0	742.5
105	SEG83	3150.0	742.5
106	SEG82	3055.0	742.5
107	SEG81	2960.0	742.5
108	SEG80	2865.0	742.5
109	SEG79	2770.0	742.5
110	SEG78	2680.0	742.5
111	SEG77	2595.0	742.5
112	SEG76	2510.0	742.5
113	SEG75	2425.0	742.5
114	SEG74	2340.0	742.5
115	SEG73	2255.0	742.5
116	SEG72	2170.0	742.5
117	SEG71	2085.0	742.5
118	SEG70	2000.0	742.5
119	SEG69	1915.0	742.5
120	SEG68	1830.0	742.5
121	SEG67	1745.0	742.5
122	SEG66	1660.0	742.5
123	SEG65	1575.0	742.5
124	SEG64	1490.0	742.5
125	SEG63	1405.0	742.5
126	SEG62	1320.0	742.5
127	SEG61	1235.0	742.5
128	SEG60	1150.0	742.5
129	SEG59	1065.0	742.5
130	SEG58	980.0	742.5
131	SEG57	895.0	742.5
132	SEG56	810.0	742.5
133	SEG55	725.0	742.5
134	SEG54	640.0	742.5
135	SEG53	555.0	742.5
136	SEG52	470.0	742.5
137	SEG51	385.0	742.5
138	SEG50	300.0	742.5
139	SEG49	215.0	742.5
140	SEG48	130.0	742.5
141	SEG47	45.0	742.5
142	SEG46	-40.0	742.5
143	SEG45	-125.0	742.5
144	SEG44	-210.0	742.5
145	SEG43	-295.0	742.5
146	SEG42	-380.0	742.5
147	SEG41	-465.0	742.5
148	SEG40	-550.0	742.5
149	SEG39	-635.0	742.5
150	SEG38	-720.0	742.5

PAD NO.	Symbol	X	Y
151	SEG37	-805.0	742.5
152	SEG36	-890.0	742.5
153	SEG35	-975.0	742.5
154	SEG34	-1060.0	742.5
155	SEG33	-1145.0	742.5
156	SEG32	-1230.0	742.5
157	SEG31	-1315.0	742.5
158	SEG30	-1400.0	742.5
159	SEG29	-1485.0	742.5
160	SEG28	-1570.0	742.5
161	SEG27	-1655.0	742.5
162	SEG26	-1740.0	742.5
163	SEG25	-1825.0	742.5
164	SEG24	-1910.0	742.5
165	SEG23	-1995.0	742.5
166	SEG22	-2080.0	742.5
167	SEG21	-2165.0	742.5
168	SEG20	-2250.0	742.5
169	SEG19	-2335.0	742.5
170	SEG18	-2420.0	742.5
171	SEG17	-2505.0	742.5
172	SEG16	-2590.0	742.5
173	SEG15	-2675.0	742.5
174	SEG14	-2765.0	742.5
175	SEG13	-2860.0	742.5
176	SEG12	-2955.0	742.5
177	SEG11	-3050.0	742.5
178	SEG10	-3145.0	742.5
179	SEG9	-3240.0	742.5
180	SEG8	-3335.0	742.5
181	SEG7	-3430.0	742.5
182	SEG6	-3525.0	742.5
183	SEG5	-3620.0	742.5
184	SEG4	-3715.0	742.5
185	SEG3	-3810.0	742.5
186	SEG2	-3905.0	742.5
187	SEG1	-4000.0	742.5
188	SEG0	-4095.0	742.5

Note: For PCB layout, IC substrate must be connected to VSS or floating.

BLOCK DIAGRAM

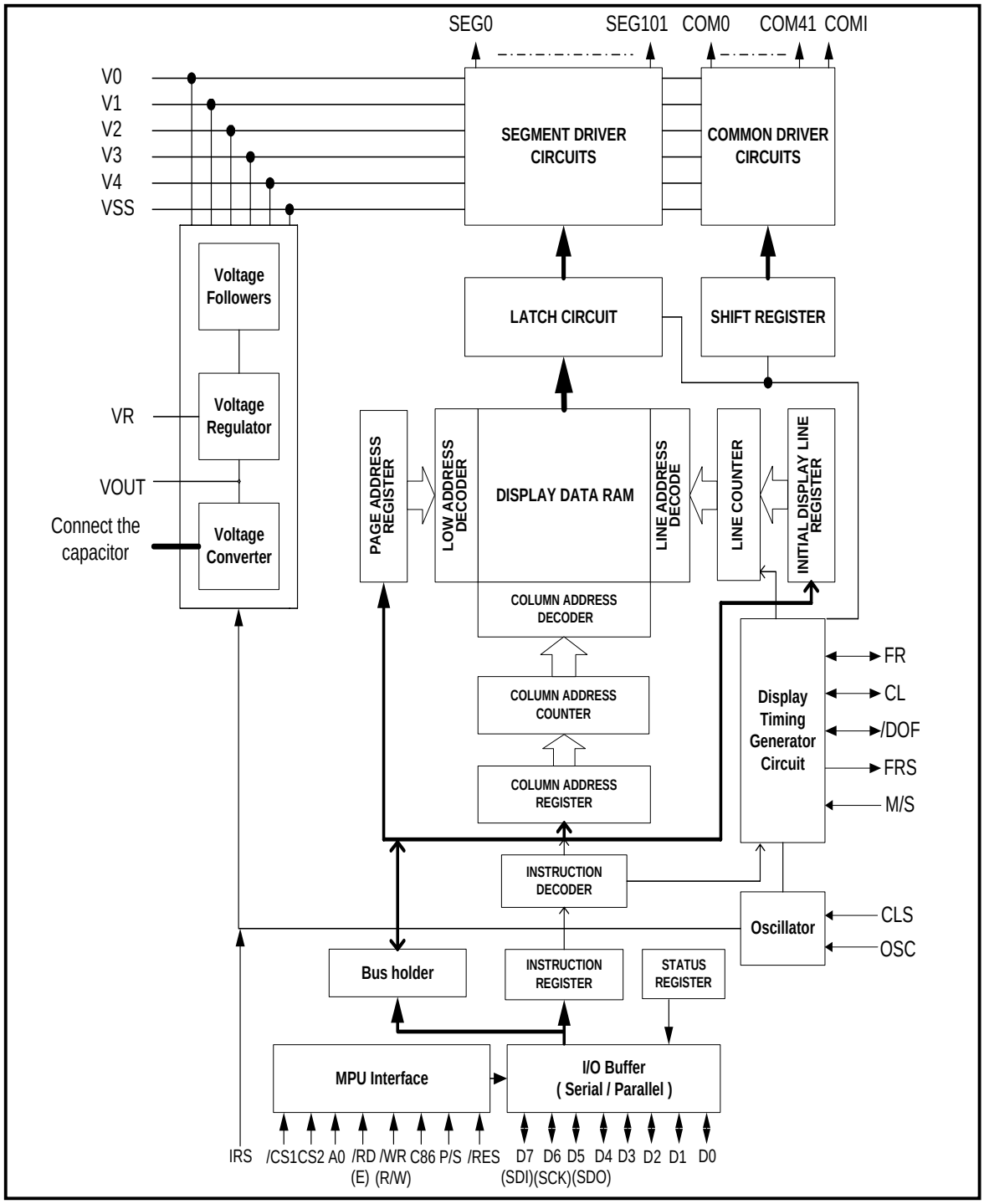


Figure 1

PIN DESCRIPTION

POWER SUPPLY

Name	I/O	Description
VDD	Power	VDD Power Supply
VSS	Power	0V (GND)
V0 V1 V2 V3 V4	Power	LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier (**OPA**) for application. Voltages have the following relationship: V0 ≧V1≧V2≧V3≧V4≧VSS When the internal power circuit is active, these voltages are generated according to the state of LCD bias, The selection of voltages is determined by the "LCD bias select" instruction, as shown in the table below.

LCD Bias	V1	V2	V3	V4
1/8 Bias	(7/8)XV0	(6/8)XV0	(2/8)XV0	(1/8)XV0
1/7.5 Bias	(6.5/7.5)XV0	(5.5/7.5)XV0	(2/7.5)XV0	(1/7.5)XV0
1/7 Bias	(6/7)XV0	(5/7)XV0	(2/7)XV0	(1/7)XV0
1/6.5 Bias	(5.5/6.5)XV0	(4.5/6.5)XV0	(2/6.5)XV0	(1/6.5)XV0
1/6 Bias	(5/6)XV0	(4/6)XV0	(2/6)XV0	(1/6)XV0
1/5.5 Bias	(4.5/5.5)XV0	(3.5/5.5)XV0	(2/5.5)XV0	(1/5.5)XV0
1/5 Bias	(4/5)XV0	(3/5)XV0	(2/5)XV0	(1/5)XV0
1/4.5 Bias	(3.5/4.5)XV0	(2.5/4.5)XV0	(2/4.5)XV0	(1/4.5)XV0
1/4 Bias	(3/4)XV0	(2/4)XV0	(2/4)XV0	(1/4)XV0
1/3.5 Bias	(2.5/3.5) XV0	(1.5/3.5)XV0	(2/3.5)XV0	(1/3.5)XV0
1/3 Bias	(2/3)XV0	(1/3)XV0	(2/3)XV0	(1/3)XV0

LCD DRIVER SUPPLY

Name	I/O	Description
C1+ C1-	O	Boosted capacitor connecting terminals used for voltage booster.
C2+ C2-	O	Boosted capacitor connecting terminals used for voltage booster.
C3 C4	O	Boosted capacitor connecting terminals used for voltage booster.
VOUT	I/O	Voltage converter output
VR	I	V0 voltage adjustment pin.

SYSTEM CONTROL

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>M/S</td><td>I</td><td>Master/slave operation select pin.
- MS = "H": Master operation
- MS = "L": Slave operation

<table>
<tr><th>M/S</th><th>CLS</th><th>OSC.</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>/DOF</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Available</td><td>Available</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>“L”</td><td>Unavailable</td><td>Available</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>“L”</td><td>*</td><td>Unavailable</td><td>Unavailable</td><td>I</td><td>I</td><td>Hi-Z</td><td>I</td></tr>
</table>
NOTE: * : Don't Care
O : Output
I : Input</td></tr>
<tr><td>P/S</td><td>I</td><td>Select Interface mode with the MPU.
When PS = "High": Parallel interface mode.
When PS = "Low": Serial interface mode.</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output pin.
When is used in master/slave mode (multi-chip), the FR pins must be connected each other.
- MS = “H”: Output
- MS = “L”: Input</td></tr>
<tr><td>C68</td><td>I</td><td>Select the kinds of the MPU to interface.
When C68 = "High": 68-series MPU interface mode
When C68 = "Low": 80-series MPU interface</td></tr>
<tr><td>/DOF</td><td>I/O</td><td>LCD Display blanking control pin. In multi-chip mode, the /DOF pin must be connected to each other.
M/S = ”H” (Master) : /DOF is output pin.
→Display “On” = “H”, Display “Off” = “L”
M/S = ”L” (Slave) : /DOF is input pin.
→Via external control. Refer to the following table.

<table>
<tr><th rowspan="2">Instruction</th><th colspan="2">/DOF</th></tr>
<tr><th>H</th><th>L</th></tr>
<tr><td>Display “On”</td><td>On</td><td>Off</td></tr>
<tr><td>Display “Off”</td><td>Off</td><td>Off</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Internal oscillator circuit enable / disable select pin.
CLS = “H”: Internal oscillator circuit is enable
CLS = “L”: Internal oscillator circuit is disable
(External display clock input to OSC pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
When the EPL43102 is used in master/slave mode (multi-chip), the CL pins must be connected each other.

<table>
<tr><th>M/S</th><th>CL</th></tr>
<tr><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
</table></td></tr>
</table>

OSC	I	When using an external oscillator, input the clock to OSC pin. When using an internal oscillator, leave this pin open.
FRS	O	Static driver output pin. This pin is used in combination with the FR pin.
IRS	I	Internal resistor select pin. This pin selects the resistors for adjusting V0 voltage level and is available only in master mode. - IRS = "H": The internal resistors are used. - IRS = "L": The external resistors are used. V0 voltage is controlled using the external divider resistor connect the VR pin.

MPU INTERFACE

Name	I/O	Description
/RES	I	Hardware reset input. The LSI is reset when this signal is pulled low. (Active low)
/CS1,CS2	I	These are the chip select signals. The Chip Select of the LSI becomes active when CS1 is "L" and also CS2 is "H" and allows the input/output of data or commands.
A0	I	Used as register selection input. When A0 = "High", Data register. When A0 = "Low", Instruction register.
/WR (R/W)	I	When C68 = "High"(68-series MPU interfacing), used as read (/WR = "High"),write (/WR = "Low") When C68 = "Low "(80-series MPU interfacing), used as write enable input (/WR).
/RD (E)	I	When C68 = "High"(68-series MPU interfacing), used as read/write enable input (E). When C68 = "Low "(80-series MPU interfacing), used as read enable input (/RD).
D0 to D7	I/O	When serial mode, D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin and the others are not used. When parallel mode, D0 to D7 are used as bi-directional data bus pin.

/CS1	CS2	Status
“L”	“L”	The device is not active. (D7~D0 is Hi-Z)
“L”	“H”	Data and instruction are available.
“H”	“L”	The device is not active. (D7~D0 is Hi-Z)
“H”	“H”	The device is not active. (D7~D0 is Hi-Z)

LCD DRIVER OUTPUT

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>COM0 to
COM41</td><td>O</td><td>The LCD common output pins.
<table>
<tr><th>Scan Data</th><th>FR</th><th>COMs Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Vss</td></tr>
<tr><td>L</td><td>V0</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COMI</td><td>O</td><td>These are two icon display pins. Both pins output the same signal.
Leave these pins open when they are not used.</td></tr>
<tr><td>SEG0 to
SEG101</td><td>O</td><td>The LCD segment output pins.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">FR</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power Save Mode</td><td colspan="2">Vss</td></tr>
</table></td></tr>
</table>

FUNCTION DESCRIPTION

SYSTEM INTERFACE

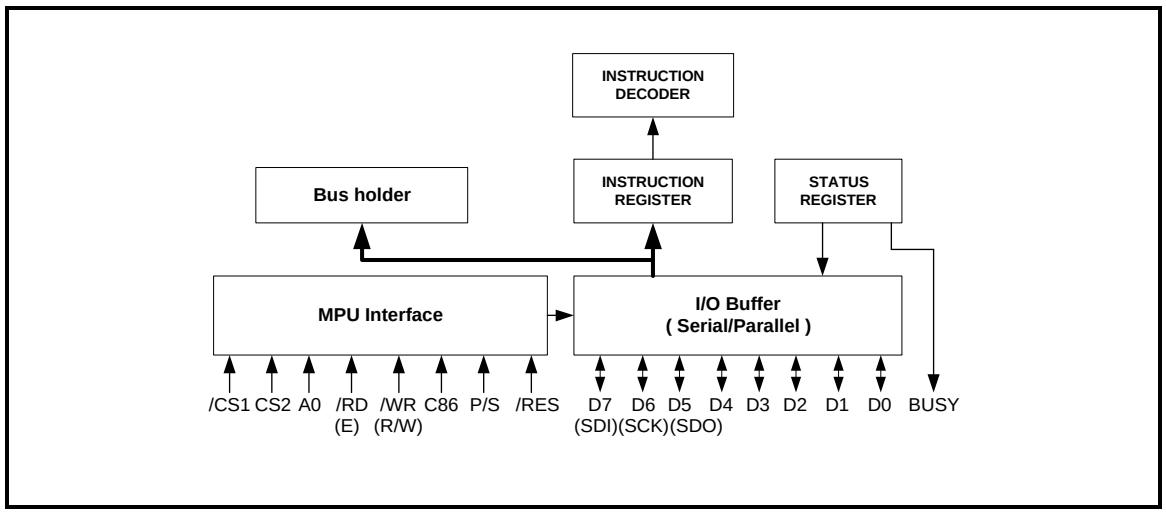


Figure 2

MPU interface

The EPL43102 has two chip select pin /CS1 and CS2. In case of /CS1="L" and CS2="H", the interface with MPU is available. When the chip select pin is inactive (Other /CS1 and CS2 condition), D7 to D0 are high impedance (invalid) and input of A0, /RD, or /WR inputs are not effective. If the serial interface has been selected, the shift register and counter are both reset.

However, the reset is always operated in any conditions of /CS1 and CS2.

P/S	C68	A0	/WR	/RD	D0~D4	D5	D6	D7
Serial Mode (L)	SPI interface (-)	A0	R/W	-	*	SDO	SCK	SDI
Parallel mode (H)	80-series (L)	A0	/WR	/RD	D0~D7			
	68-series (H)	A0	R/W	E	D0~D7			

NOTE: ***** : Don' t care ("High", "Low" or "Open")

- : Fixed " High" (VDD) or " Low" (VSS)

The EPL43102 can be operated with serial interface (SPI) and parallel interface (80-series or 68-series) is selected by P/S pin.

1. *Serial mode (SPI)*: When serial mode (PS = "L"), D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin. When the LSI is active (/CS1="L", CS2="H"), serial data input (D7), serial clock input (D6) inputs and serial data output (D5) are enabled. The 8-bit shift register and 3-bit counter are reset to the initial condition when the chip is not selected. The data input/output from SDI/SDO terminal is MSB first like as the order of D7, D6…D0, and is latched at the rising edge of the serial clock SCK. Serial input data is display data when A0="H" and instruction when is A0="L". The A0 input is read in and identified at the rising edge of the (8 x n) serial clock pulse. Since the clock signal (D6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

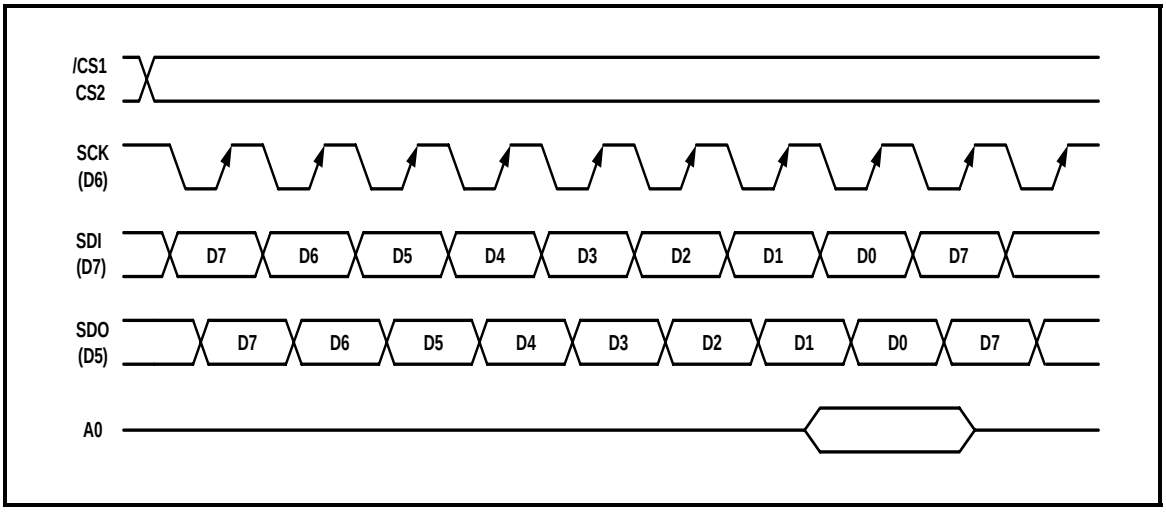


Figure 3

A0	/WR (R/W)	D7 (SDI)	D5 (SDO)
0	0	Instruction Write	Status Read
0	1	Invalid	Status Read
1	0	Display Data Write	Status Read
1	1	Invalid	Display Data Read

2. *Parallel mode (8-bit length)*: When the parallel input is selected (PS = ”H”), D0~D7 can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to high or low.

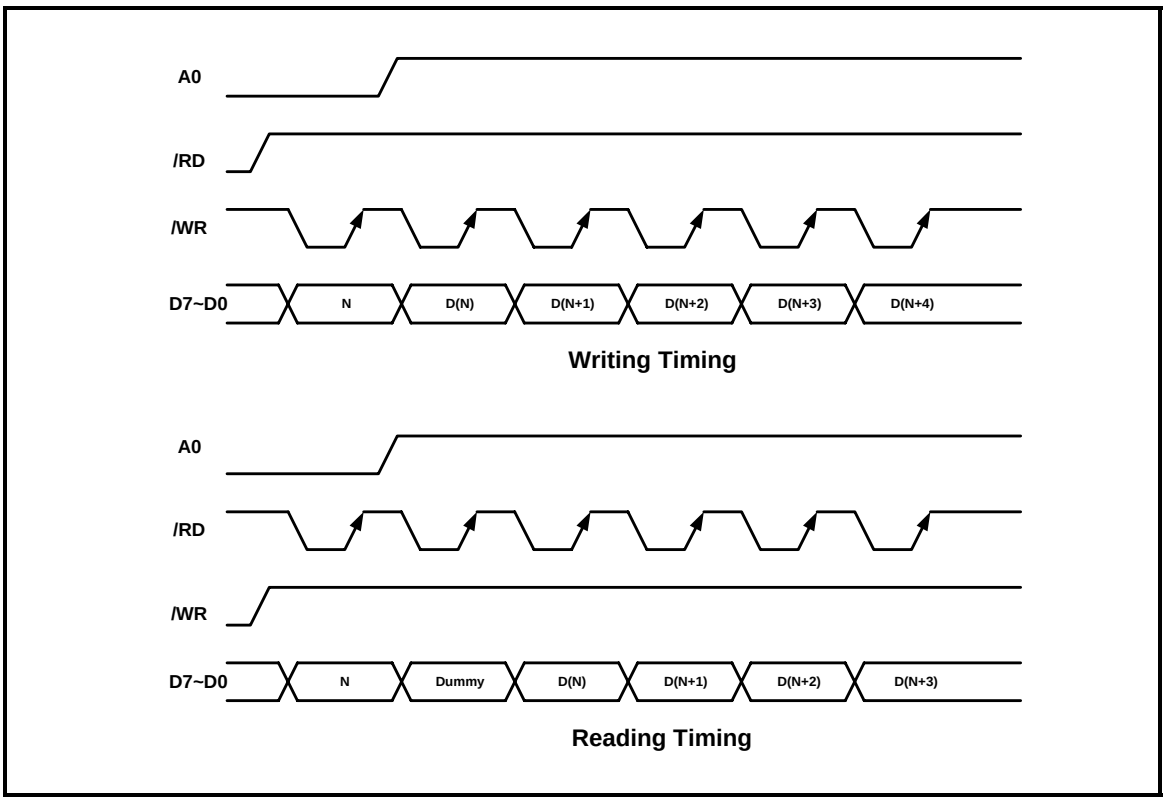


Figure 4

Common	80-series		68-series	Description
A0	/RD	/WR	R/W	
H	L	H	H	Display data read
H	H	L	L	Display data write
L	L	H	H	Register status read
L	H	L	L	Writes to Instruction register

DATA TRANSFER

The EPL43102 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to the DDRAM, data is automatically transferred from the bus holder to the DDRAM. When reading data from the DDRAM to MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and MPU reads this stored data from bus holder for the next data read cycle.

DISPLAY DATA RAM

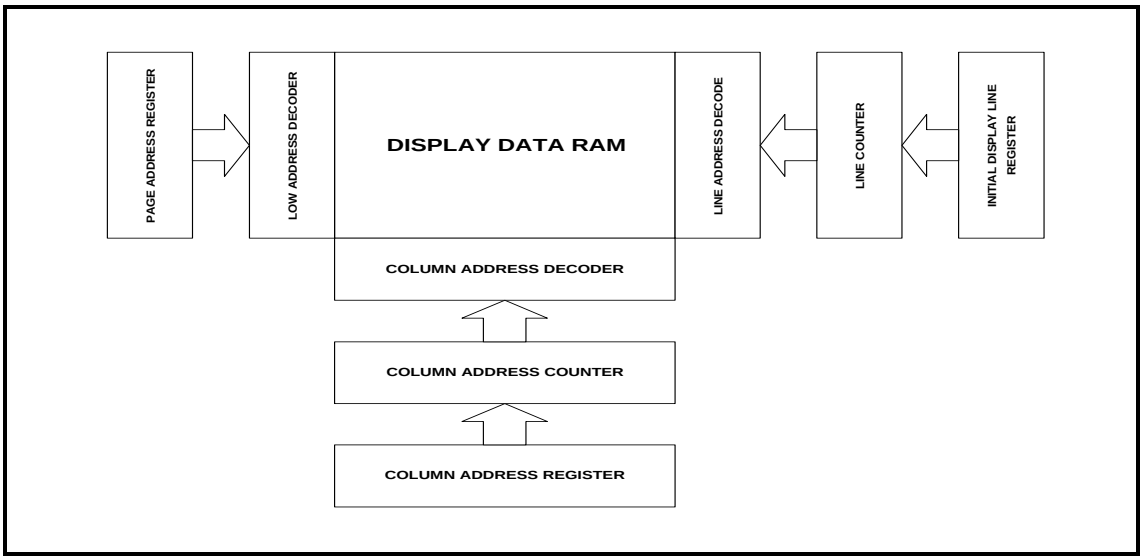


Figure 5

The display data RAM *(DDRAM)* stores pixel data for the LCD. It is a 43-row x 102-column addressable array. It is possible to access any required bit by specifying the page address and the column address. The 43 rows are divided into 5 pages of 8 lines, 1 page with 2 line (D0,D1) and the seventh page with a single line (D0 only).

The each bit in the Display Data RAM corresponds to the each pixel of the LCD each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

(Refer to “Inverse Display ON/OFF” instruction for more detail.)

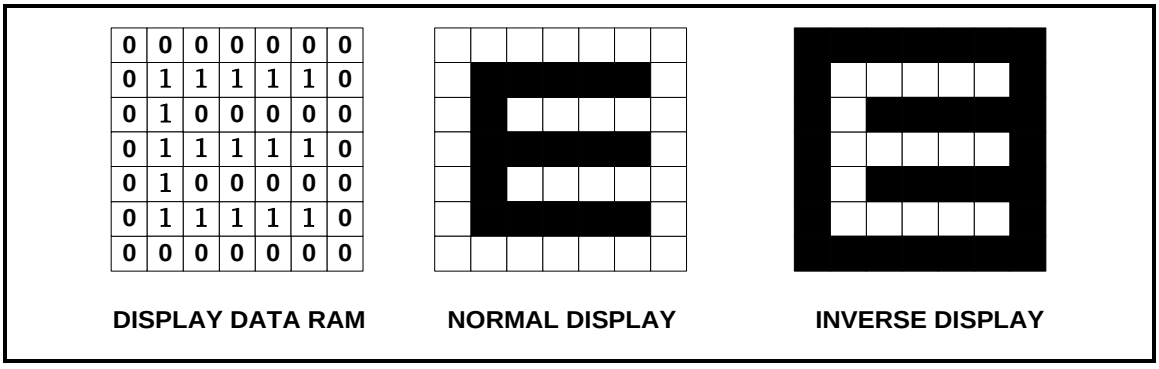


Figure 6

The microprocessor (MPU) can read from and write to RAM through the I/O buffer. Since the LCD controller operates *independently*, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address P3,P2,P1,P0				Data	Column Address								Line Address (HEX)	Common Output (1/42,1/43)	Common Output (1/36,1/37)	Common Output (1/32,1/33)	Common Output (1/16,1/17)
0	0	0	0	D0				PAGE0					00	COM36			
				D1									01	COM37			
				D2									02	COM38			
				D3									03	COM39			
				D4									04	COM40			
				D5									05	COM41			
				D6									06	COM0	COM0	COM0	COM0
				D7									07	COM1	COM1	COM1	COM1
0	0	0	1	D0				PAGE1					08	COM2	COM2	COM2	COM2
				D1									09	COM3	COM3	COM3	COM3
				D2									0A	COM4	COM4	COM4	COM4
				D3									0B	COM5	COM5	COM5	COM5
				D4									0C	COM6	COM6	COM6	COM6
				D5									0D	COM7	COM7	COM7	COM7
				D6									0E	COM8	COM8	COM8	COM8
				D7									0F	COM9	COM9	COM9	COM9
0	0	1	0	D0				PAGE2					10	COM10	COM10	COM10	COM10
				D1									11	COM11	COM11	COM11	COM11
				D2									12	COM12	COM12	COM12	COM12
				D3									13	COM13	COM13	COM13	COM13
				D4									14	COM14	COM14	COM14	COM14
				D5									15	COM15	COM15	COM15	COM15
				D6									16	COM16	COM16	COM16	
				D7									17	COM17	COM17	COM17	
0	0	1	1	D0				PAGE3					18	COM18	COM18	COM18	
				D1									19	COM19	COM19	COM19	
				D2									1A	COM20	COM20	COM20	
				D3									1B	COM21	COM21	COM21	
				D4									1C	COM22	COM22	COM22	
				D5									1D	COM23	COM23	COM23	
				D6									1E	COM24	COM24	COM24	
				D7									1F	COM25	COM25	COM25	
0	1	0	0	D0				PAGE4					20	COM26	COM26	COM26	
				D1									21	COM27	COM27	COM27	
				D2									22	COM28	COM28	COM28	
				D3									23	COM29	COM29	COM29	
				D4									24	COM30	COM30	COM30	
				D5									25	COM31	COM31	COM31	
				D6									26	COM32	COM32		
				D7									27	COM33	COM33		
0	1	0	1	D0				PAGE5					28	COM34	COM34		

				D1									29	COM35	COM35		
0	1	1	0	D0				PAGE6						COMI	COMI	COMI	COMI
Column Address(HEX)				ADC=0	00	01	02	- - - - - - - - -	62	63	64	65					
				ADC=1	65	64	63	- - - - - - - - -	03	02	01	00					
LCD Output					SEG0	SEG1	SEG2	- - - - - - - - -	SEG98	SEG99	SEG100	SEG101					

NOTE: For example the initial display line address is 06H.

Programmable Duty Ratio

The duty ratio is selected by “Set Duty Ratio” instruction.

The common output circuits have showed as following figure 7. They are separated into three shift registers and control by "duty ratio register".

The common output circuits have showed as following figure. They are separated into three shift registers and control by "duty ratio register".

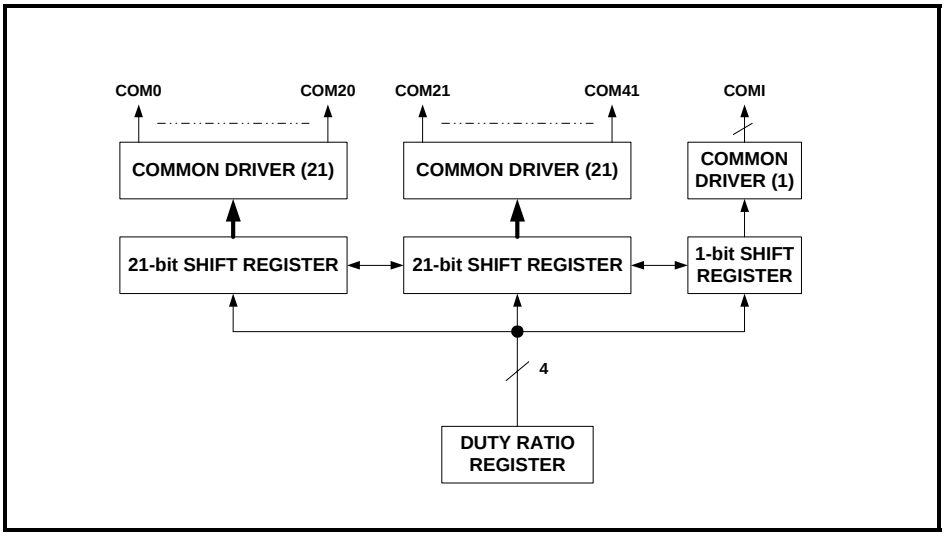


Figure 7

Duty	SHL	Common Output Pins												
		0	1	2	……					39	40	41	COMI
1/43	0	COM[0..41]												COMI
1/42	1	COM[41..0]												–
1/37	0	COM[0..17]							COM[18..35]					COMI
1/36	1	COM[35..18]							COM[17..0]					–
1/33	0	COM[0..15]							COM[16..31]					COMI
1/32	1	COM[31..16]							COM[15..0]					–
1/25	0	COM[0..11]							COM[12..23]					COMI
1/24	1	COM[23..12]							COM[11..0]					–
1/17	0	COM[0..7]							COM[8..15]					COMI
1/16	1	COM[15..8]							COM[7..0]					–
1/9	0	COM[0..3]							COM[4..7]					COMI
1/8	1	COM[7..4]							COM[3..0]					–

The Relationship between Duty Ratio and Common Output

Initial display line register

The initial display line register assigns a DDRAM line address which corresponds to COM0 by “Initial display line set” instruction. It is used for not only normal display but also vertical display scrolling and page switching without changing the contents of the DDRAM. However, the 43th address for icon display can’t be assigned for initial display line address.

Line counter

The line counter provides a DDRAM line address. It initializes its contents at the switching of frame reversal signal (FR), and also counts-up in synchronization with common timing signal.

Column address counter

The column address counter is an 8-bit preset counter which provides a DDRAM column address, and it is independent of below-mentioned page address register.
It will increment (+1) the column address whenever “display data read” or “display data write” instructions are issued. However, the incrementing of column address is stopped at column address of 65H. The count-lock will be able to be released by the “column address set” instruction again. The counter can invert the correspondence between the column address and segment driver direction by means of “ADC select” instruction.

Page address register

The page address register provides a DDRAM page address. The page address 6 is used for icon display, and only D0 is valid.

LCD DRIVER CIRCUITS

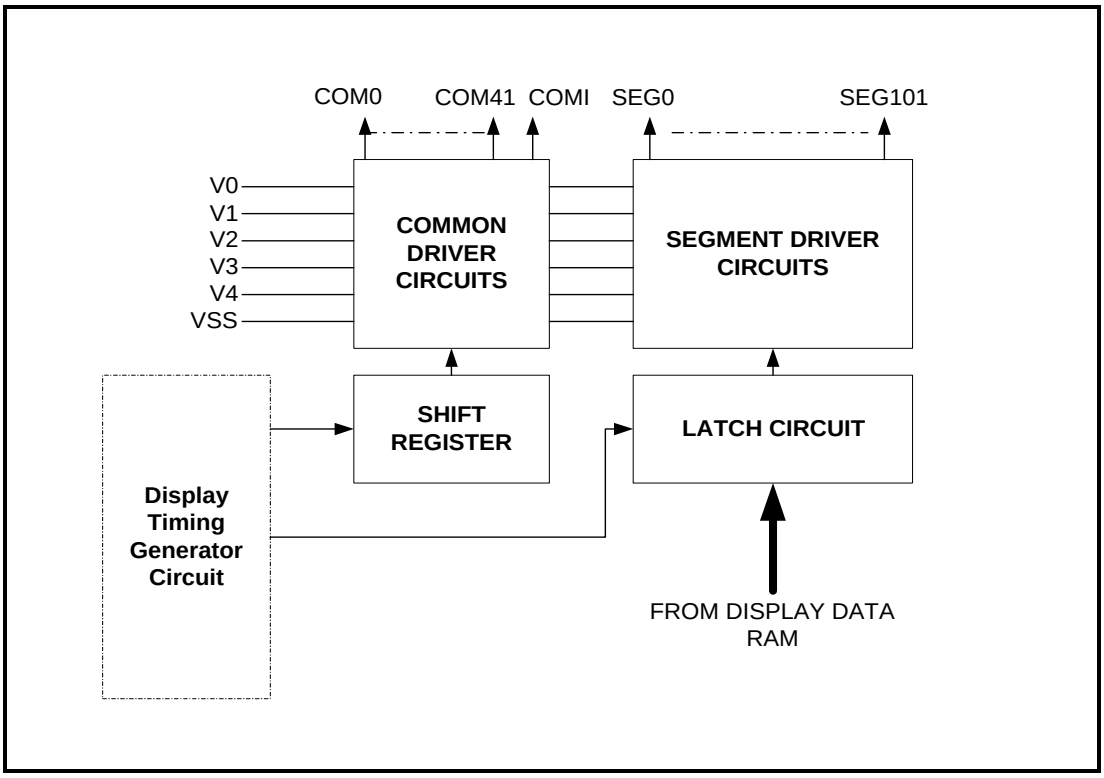


Figure 8

This driver circuit is configured by 42-common drivers, 102-segment drivers and 1-icon-common driver. This LCD panel driver voltage depends on the combination of display data and FR signal.

Display data latch circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
“Display on/off”, “Inverse display on/off” and “Entire display on/off” instructions control only the contents of this latch circuit, they can’t change the contents of the DDRAM.

Shift register circuit

The circuit contains a 42-bit shift register to shift the turn-on data required for the LCD drive common signals and 1-bit shift register used for icon. The clock of this shift register is generated by display clock CL.

Examples of 1/33 and 1/43 duty (ICON enable) driving waveform

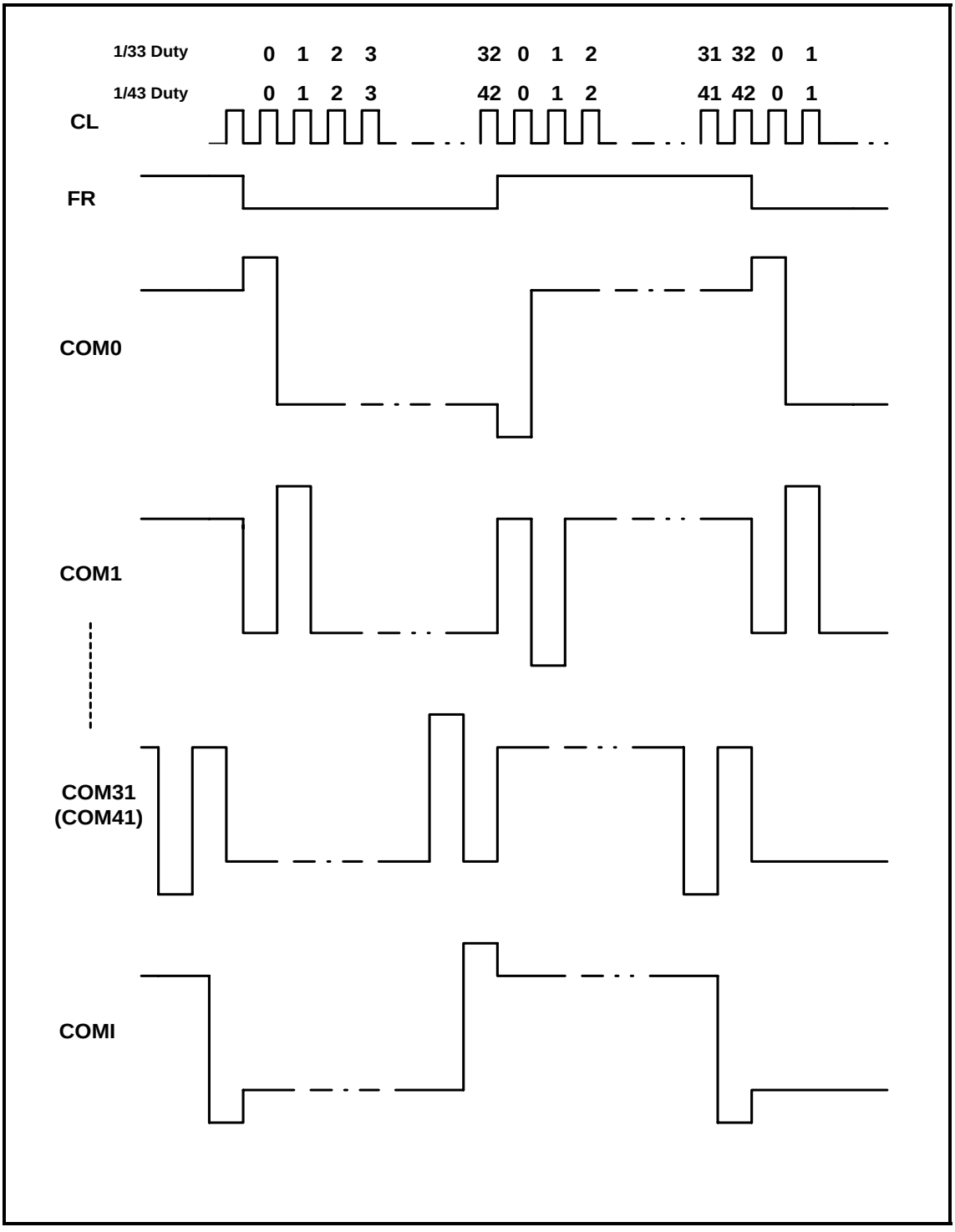


Figure 9

Examples of 1/32 and 1/42 duty (ICON disable) driving waveform

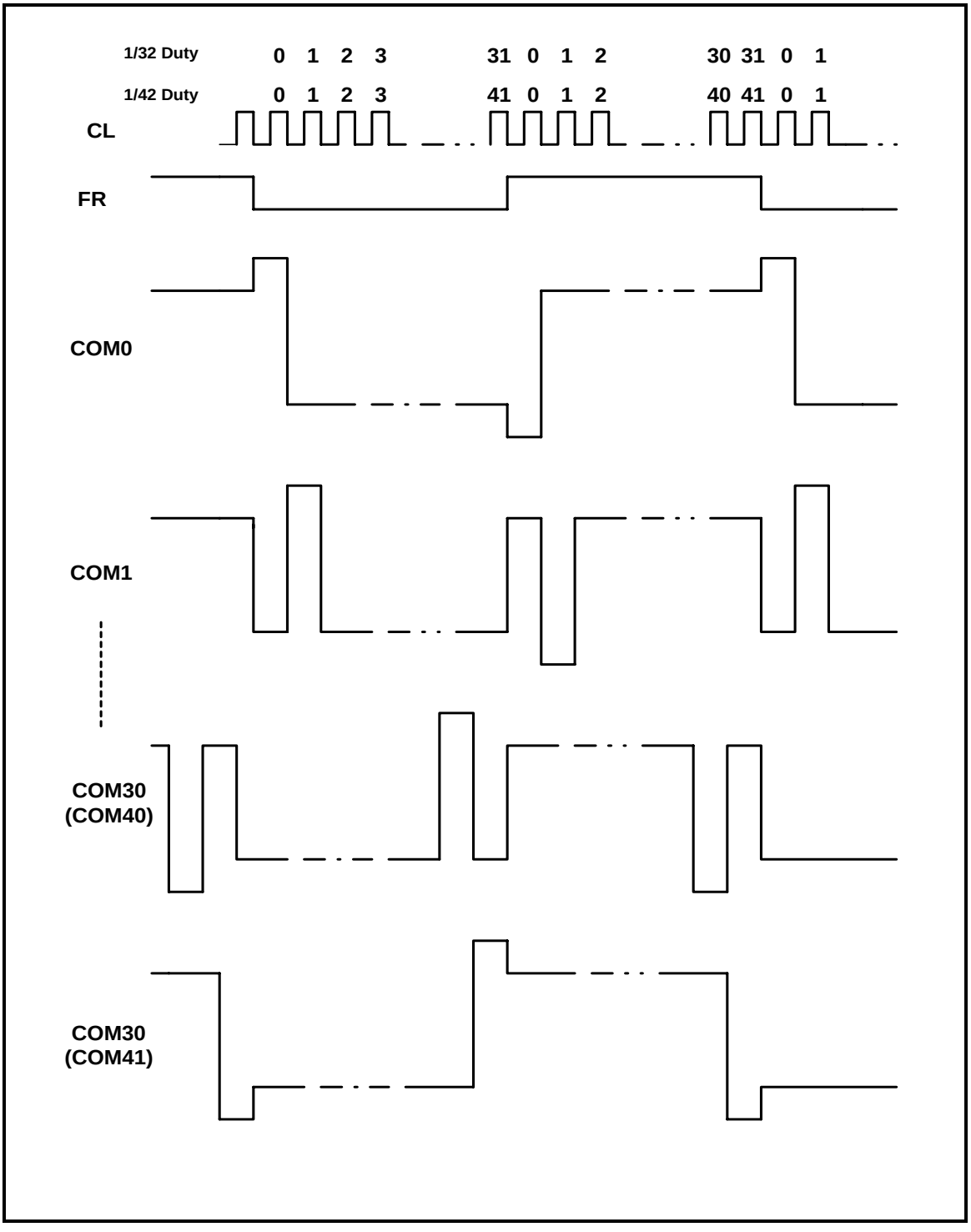
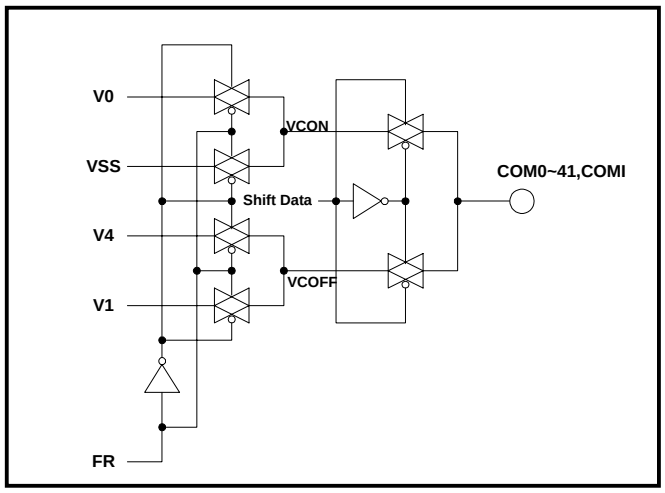


Figure 10

Common driver circuit

Common driver circuit consists of 43 drive circuits. One of the four LCD driving level is selected by the combination of FR and the data from the sift register.

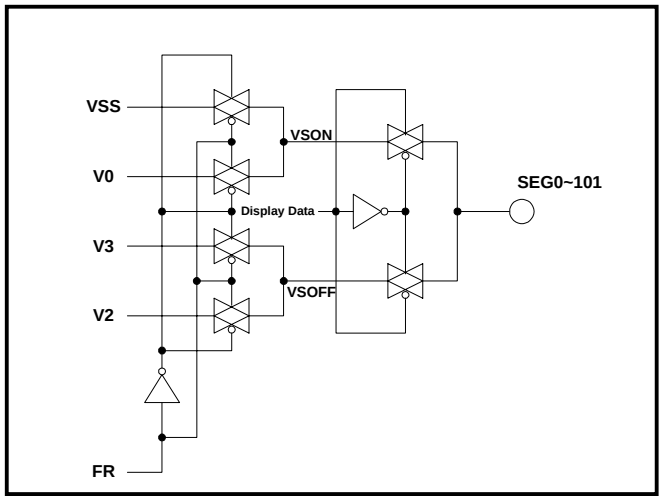


Scan Data	FR	COMs Output Voltage
H	H	VSS
	L	V0
L	H	V1
	L	V4
Power save mode		VSS

Figure 11

Segment driver circuit

Segment driver circuit consists of 102 driver circuits. One the four LCD driving level is selected by the combination of FR and the display data transferred from the latch circuit.



Display Data	FR	SEGs Output Voltage	
		Normal Display	Inverse Display
H	H	V0	V2
	L	VSS	V3
L	H	V2	V0
	L	V3	VSS
Power save mode		VSS	

Figure 12

LCD Driving Waveform

The following illustration is an example of how the common and segment drivers to a LCD panel.

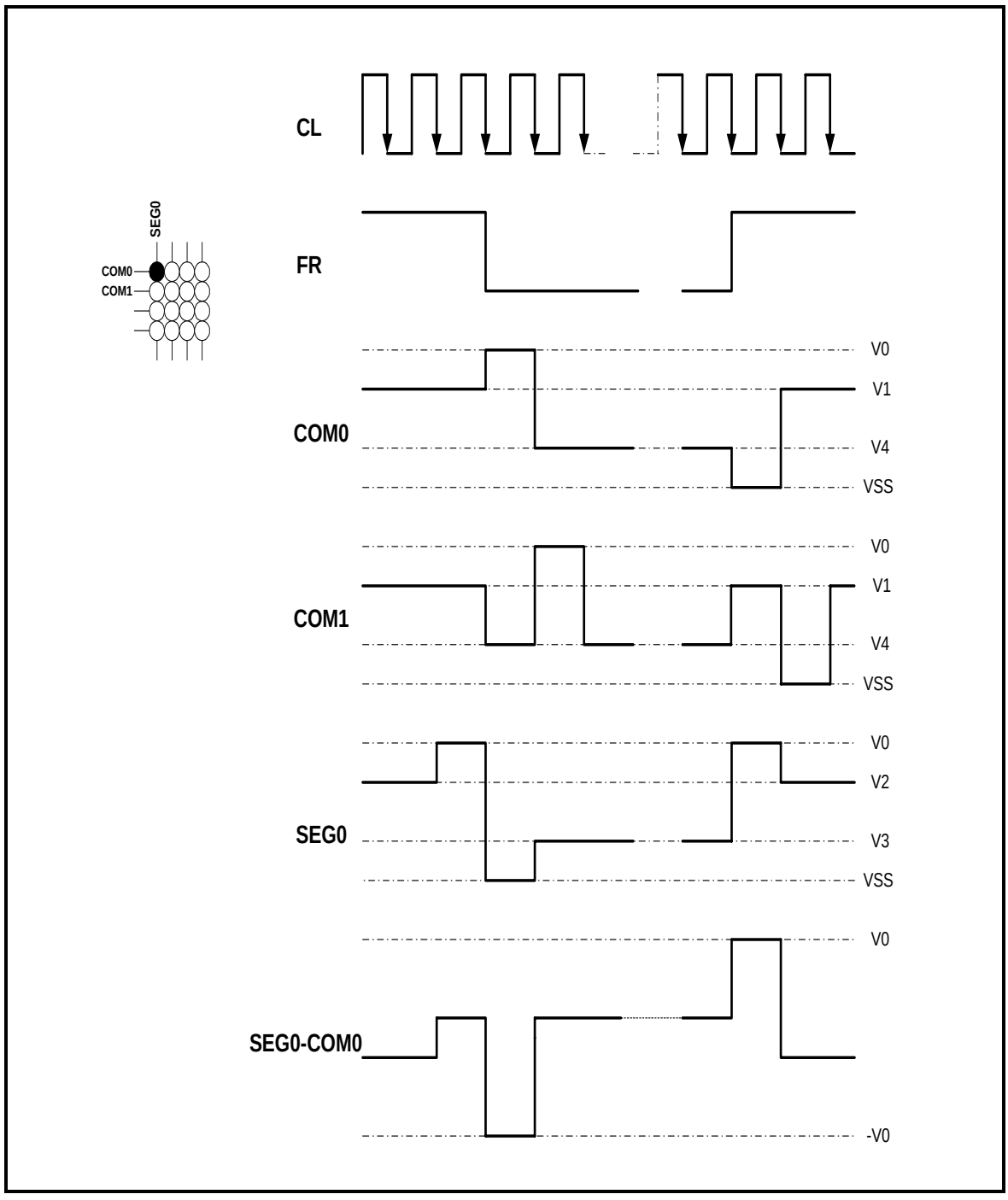


Figure 13

INTERNAL POWER CIRCUITS

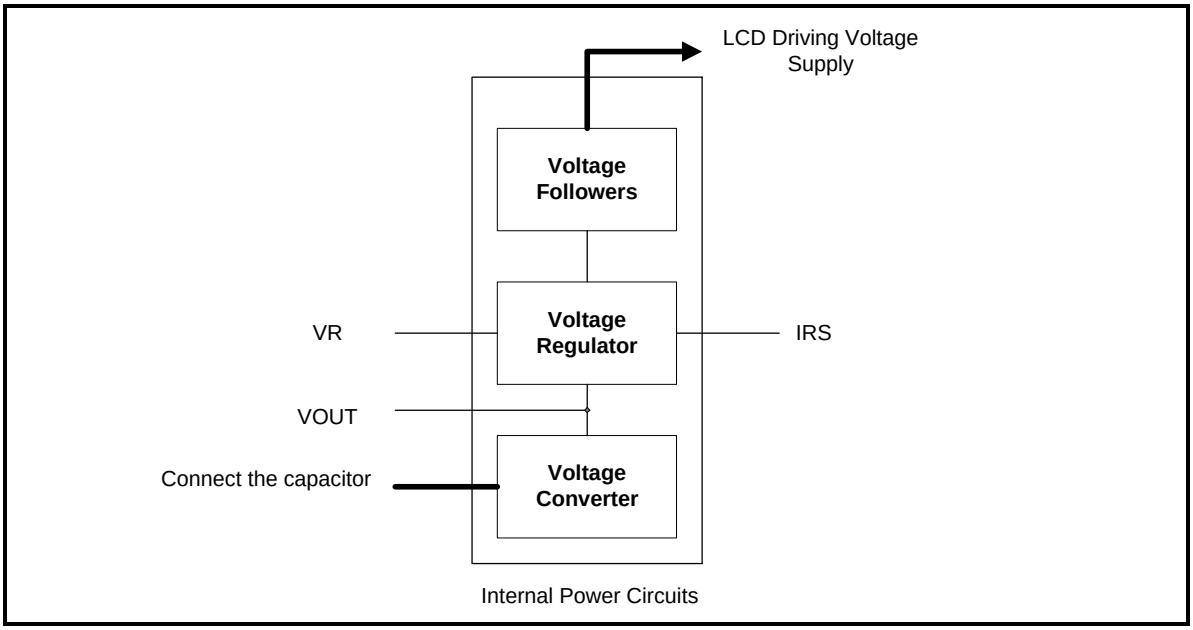


Figure 14

The internal power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter (V/C) circuits, voltage regulator (V/R) circuits, and voltage follower (V/F) circuits. They are valid only in **master** operation and controlled by “Power Control” instruction. For details, refers to "Instruction Description".

User Setup	Power control (VC VR VF)	V/C Circuits	V/R circuits	V/F Circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage Regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

Voltage converter circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3, 4, or 5 times toward positive side and boosted voltage is outputted from VOUT pin. The boosting magnitude of internal booster circuit is selected by the capacitor connection (Refer Figure 15). The internal oscillator is required to be operating when using this converter, because the divided signal provided from the oscillator is used for the internal timing of this circuit.

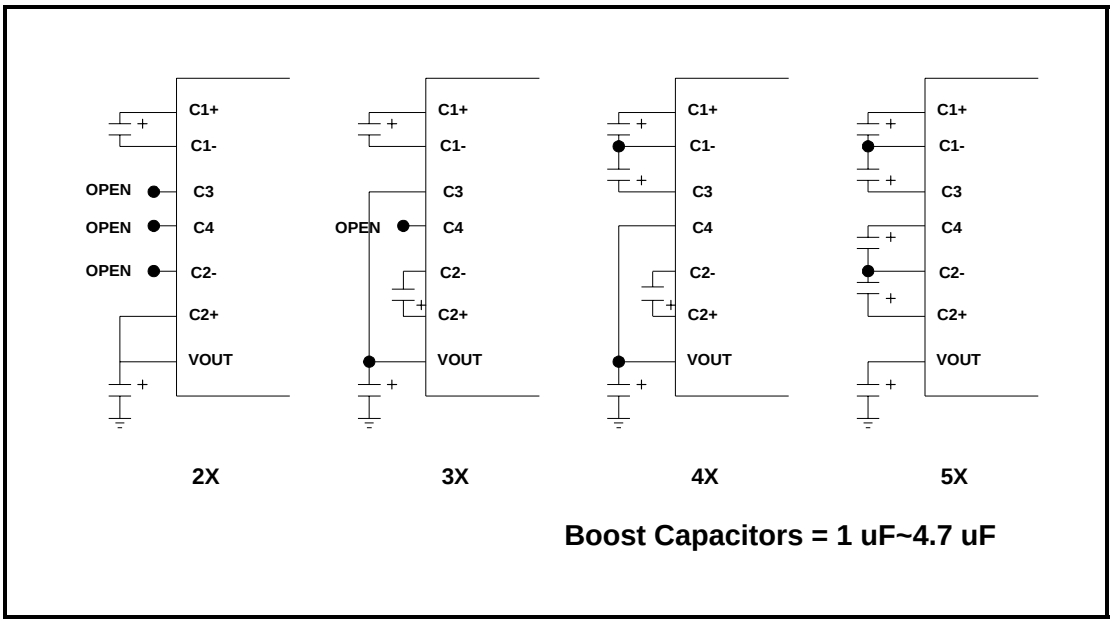


Figure 15

Voltage regulator circuits

The voltage regulator determines the LCD driving voltage V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits, it is necessary to be applied internally or externally. For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by IRS pin. And **VEV** called the voltage of *electronic volume* is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Contrast Control Mode", within the range 0 to 63.

VREF, a constant voltage source is 2 V at T_A=25^{o}C.

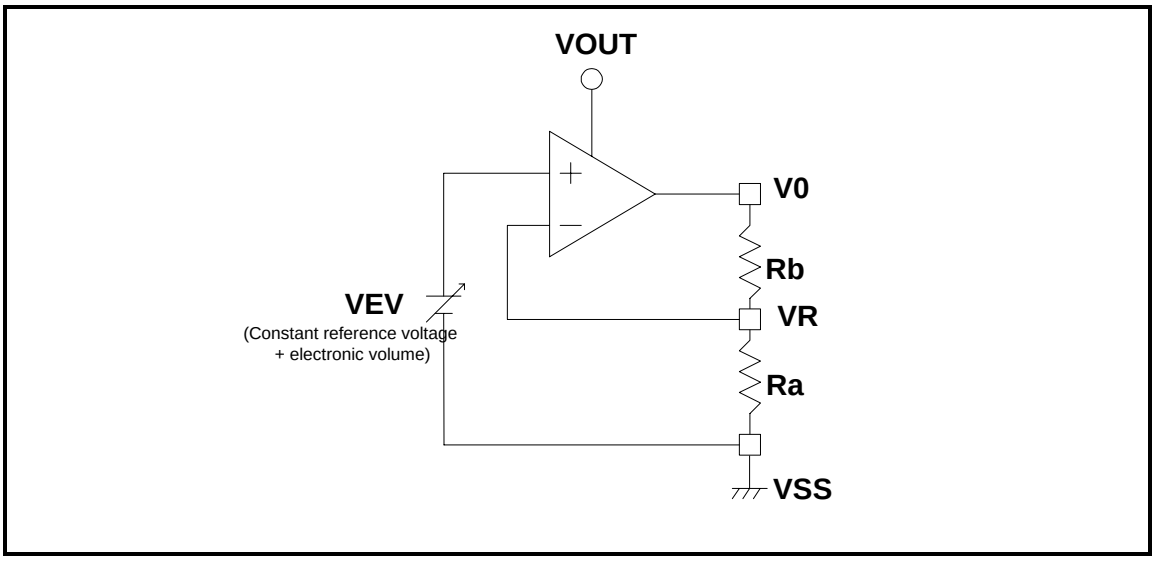


Figure 16

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV \quad \text{.....Eq.1}$$

$$VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF \quad \text{.....Eq.2}$$

Register value (R2 R1 R0)	1+(Rb/Ra)	Value
0 0 0	3.5	Small
0 0 1	4.0	.
0 1 0	4.5	.
0 1 1	5.0	.
1 0 0	5.5	.
1 0 1	6.0	.
1 1 0	6.5	.
1 1 1	7.0	Large

(Refer to “Regulator Resistor Select” instruction for detail.)

α	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
..	.	.	.	.	.	.
..	.	.	.	.	.	.
62	1	1	1	1	1	0
63	1	1	1	1	1	1

(Refer to “Set Contrast Control Mode” instruction for detail.)

In case of using internal resistors, Ra and Rb. (IRS = "H")

When IRS pin is " H" , resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

In case of using external resistors, Ra and Rb. (IRS = "L")

When IRS pin is " L" , it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

For a particular liquid, the optimum V_{LCD} can be calculated for a given multiplex rate. For duty ratio is 1/43, the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{43}}{\sqrt{2\times\left(1-\frac{1}{\sqrt{43}}\right)}}\times V_{th} = 5.805\times V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Voltage follower circuits

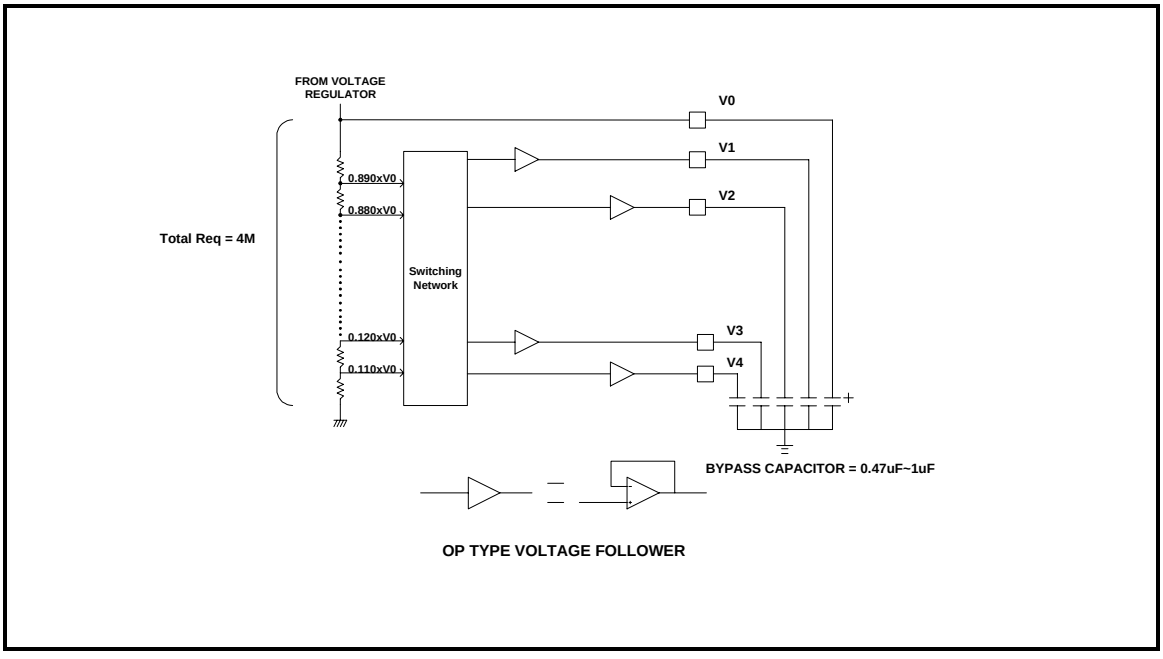


Figure 17

V_{LCD} voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower (**OPA**) for increasing drive capability. Total 6 levels LCD reference voltage (V0,V1,V2,V3,V4,VSS) is generated by the voltage follower circuits.

LCD Bias	V1	V2	V3	V4
1/8	0.875*V0	0.750*V0	0.250*V0	0.125*V0
1/7.5	0.865*V0	0.735*V0	0.265*V0	0.135*V0
1/7	0.855*V0	0.715*V0	0.285*V0	0.145*V0
1/6.5	0.845*V0	0.690*V0	0.310*V0	0.155*V0
1/6	0.835*V0	0.665*V0	0.335*V0	0.165*V0
1/5.5	0.820*V0	0.635*V0	0.365*V0	0.180*V0
1/5	0.800*V0	0.600*V0	0.400*V0	0.200*V0
1/4.5	0.780*V0	0.555*V0	0.445*V0	0.220*V0
1/4	0.750*V0	0.500*V0	0.500*V0	0.250*V0
1/3.5	0.715*V0	0.430*V0	0.570*V0	0.285*V0
1/3	0.665*V0	0.335*V0	0.665*V0	0.335*V0

Different duty radio requires different bias level. For optimum bias level, B_L can be calculated from:

$$B_L = \frac{1}{\sqrt{Duty\ ratio + 1}}$$

Changing the bias system from the optimum will have a consequence on the contrast and viewing angle.

The LCD Bias affects the display quality. But for reducing the current consumption, the unsuitable bias may be selected. Therefore, the LCD Bias could be selected by “Select LCD bias” instruction.

LCD DISPLAY CIRCUITS

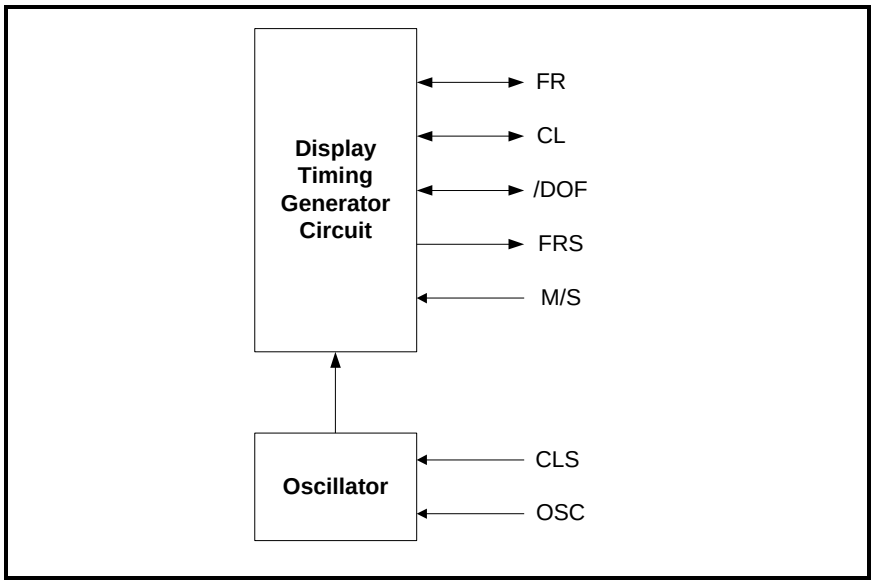


Figure 18

Oscillator

This is a completely on-chip oscillator and its frequency is nearly independent of VDD. This is the low power consumption RC type oscillator which provides the display clock and voltage converter timing clock.

When "**M/S="H" and "CLS"="H**", the oscillator circuit is enable. When CLS="L", the oscillator is stop, and the oscillator clock has to be input to the OSC pin.

The oscillator circuit is available in **master** mode only. The oscillator signal is divided and output as display clock at CL pin.

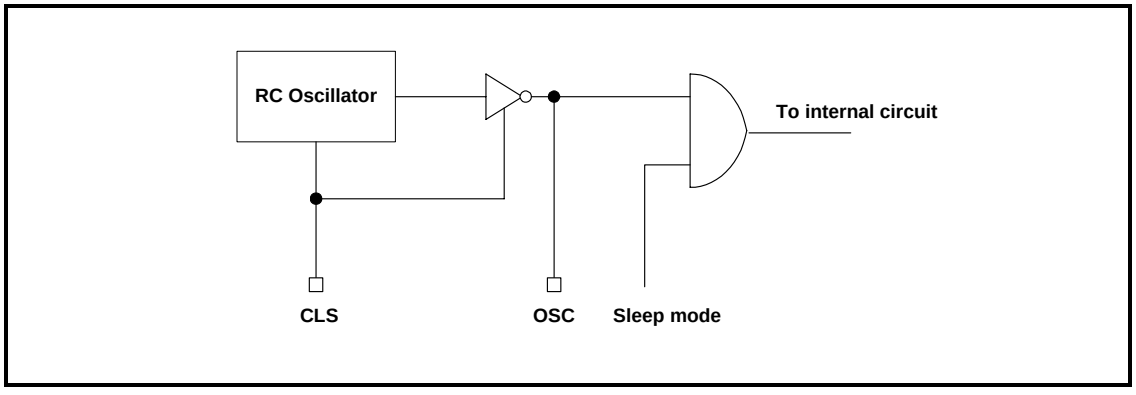


Figure 19

/DOF pin description

The pin is used to control blinking LCD display.

Instruction	M/S= "H"	M/S="L"	
	/DOF (Output)	/DOF (Input) ="H"	/DOF (Input) ="L"
Display "ON"	"H"	LCD On	LCD Off
Display "OFF"	"L"	LCD Off	LCD Off

When the "Power Save" Instruction is activating, the /DOF pin is set to low level.

Display timing generator circuit

This circuit generates some signals to be used to display LCD. When using in master/slave mode (multi-chip), some pins must be connected each other. That's due to synchronization output. The display clock (CL) generated by the oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL), and the 102-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor.
The display clock generates an LCD frame reversal signal (FR) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver.. When this EPL43102 is used for a multi-chip, the slave chip must receive the FR, CL, /DOF signals from the master.

Operation Mode		FR	CL	/DOF	FRS	OSC
Master (M/S="H")	Internal oscillator is enable(CLS="H")	Output	Output	Output	Output	Open
	Internal oscillator is disable (CLS="L")	Output	Output	Output	Output	Input
Slave (M/S="L")	Internal oscillator is disable (CLS ="L" or "H")	Input	Input	Input	Hi-Z	Open
		Input	Input	Input	Hi-Z	Open

Note: Open means "leave the pin open"

Oscillator frequency

The EPL43102 contains a RC oscillator. The frame frequency (f_{FM}) is derived from the RC circuit's oscillation frequency (f_{OSC}) by driving it an appropriate value. The relationship between the oscillation frequency (f_{OSC}), display clock frequency (f_{CL}) and the frame frequency (f_{FM}) is shown below.

The f_{OSC} could be selected internal or external oscillator via CLS pin, f_{CL} could be selected via “Set display clock CL frequency” instruction, and frame frequency could be calculated via following equation.

f_{CL} = (Duty ratio) x (Frame frequency)

THE RESET CIRCUIT

When the /RES input comes to the “L” level, these LSI return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC select instruction D0 = “L”)
4. SHL select: Normal (SHL select instruction D3 = “L”)
5. Power control register: (D2, D1, D0) = (0, 0, 0)
6. Serial interface internal register data clear
7. Duty ratio = 1/43
8. CL frequency Register (D4, D3, D2, D1,D0) = (0, 0, 0, 0, 1, 1)
9. LCD power supply bias level = (1/8)
10. Entire display OFF (Entire display instruction D0 = “L”)
11. Power saving clear
12. Modify-Read OFF
13. Static indicator OFF
    Static indicator register : (D1, D2) = (0, 0)
14. Display initial line set to first line : 0
15. Column address set to Address : 0
16. Page address set to Page : 0
17. V0 voltage regulator internal resistor ratio set mode clear: (R2, R1, R0) = (0, 0, 0)
18. Contrast control set mode clear
    Contrast control register : (D5, D4, D3, D2, D1,D0) = (1, 0, 0, 0, 0, 0)

INSTRUCTION DESCRIPTION

Instruction	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Description
Read Display Data	1	0	1	Read Data								Read data from DDRAM
Write Display Data	1	1	0	Write Data								Write data into DDRAM
Read Status	0	0	1	Status				0	0	0	0	Read the internal status
Set Duty Ratio Mode	0	1	0	1	0	0	0	0	1	0	0	Set duty ratio Mode
Duty Ratio Register	0	1	0	*	*	*	*	ICON	D2	D1	D0	Select the duty ratio
Set CL frequency Mode	0	1	0	1	0	0	0	0	0	1	0	Set CL frequency Mode
CL frequency Register	0	1	0	*	*	*	D4	D3	D2	D1	D0	Set CL frequency Register
Set LCD Bias select Mode	0	1	0	1	0	0	0	0	1	0	1	Set LCD Bias select Mode
LCD Bias select Register	0	1	0	*	*	*	*	D3	D2	D1	D0	Select the LCD Bias
Display On/Off	0	1	0	1	0	1	0	1	1	1	Don	Turn on/off LCD panel When DON=0: display off When DON=1: display on
Initial Display Line	0	1	0	0	1	D5	D4	D3	D2	D1	D0	Specify DDRAM line for COM0
Set Contrast Control Mode	0	1	0	1	0	0	0	0	0	0	1	Set Contrast Control Mode
Set Contrast Control Register	0	1	0	*	*	D5	D4	D3	D2	D1	D0	Set Contrast Control Register
Set Page Address	0	1	0	1	0	1	1	Page Address				Set page address
Set Column Address MSB	0	1	0	0	0	0	1	Higher order Column Add.				DDRAM column address of Higher 4-bits
Set Column Address LSB	0	1	0	0	0	0	0	Lower order column Add.				DDRAM column address of lower 4-bits
ADC Select	0	1	0	1	0	1	0	0	0	0	ADC	Select segment direction When ADC=0: normal direction (SEG0 →SEG101) When ADC=1: reverse direction (SEG101→SEG0)
Inverse Display ON/OFF	0	1	0	1	0	1	0	0	1	1	REV	Select normal/inverse display 0 : Normal display 1 : Inverse display on
Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON=0: normal display. When EON=1: entire display ON
Set Modify-read	0	1	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset Modify-read	0	1	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL Select	0	1	0	1	1	0	0	SHL	*	*	*	Select COM output direction When SHL=0: normal direction (COM0 -> OM41) When SHL=1: reverse direction (COM41 -> COM0)
Power Control	0	1	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator Resistor Select	0	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set Static Indicator Mode	0	1	0	1	0	1	0	1	1	0	SM	Set static indicator mode When SM = 0: off When SM = 1: on
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	S1	S0	Set static indicator register
Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON

Note: * : Don't care

Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. After writing the display data, the column address is automatically incremented so that the microprocessor can continuously write data to the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

Read Status

This instruction reads out the internal status regarding “ADC select”, “Display on/off” and “Reset”.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	-	ADC	On/Off	RESET	0	0	0	0

Flag	Description
ADC	It shows the correspondence between the column address and segment drivers. ADC =0 : Reverse direction (SEG101 → SEG0) =1 : Normal direction (SEG0 → SEG101)
On/Off	This bit indicates the ON/OFF state of the display. 0: Display ON 1: Display OFF
RESET	Indicates the initialization is in progress by RESETB signal. RESET =0 : Normal display operation state =1 : Internal reset operation state with reset command.

Set Duty Ratio *(Two-Byte instruction)*

Consists of 2-byte instruction. The first instruction sets duty ratio mode, the second one updates the contents of duty ratio register. After second instruction, set duty mode is released. The LSI can’t accept any instructions except the “Set duty ratio register” during the sets duty ratio mode

Set Duty Ratio mode (First instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	0

Set Duty Ratio Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Duty ratio
0	1	0	*	*	*	*	ICON	0	0	0	8 (+ICON)
								0	0	1	16(+ICON)
								0	1	0	24(+ICON)
								0	1	1	32(+ICON)
								1	0	0	36(+ICON)
								1	0	1	42(+ICON)

ICON: “1” Enable COMI (icon display) pin

: ”0” Disable COMI (icon display) pin

Set display clock CL frequency *(Two-Byte instruction)*

The display clock CL affects the current consumption and the frame frequency affects the flicker, so the fine adjustment is required for the display clock CL and the frame frequency.

Set CL frequency select mode (First instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	1	0

Set CL frequency select Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	CL frquency
0	1	0	*	*	*	0	0	0	0	0	f_{OSC}
						0	0	0	0	1	f_{OSC} / 2
						0	0	0	1	0	f_{OSC} / 3
						0	0	0	1	1	f_{OSC} / 4
						0	0	1	0	0	f_{OSC} / 5
						0	0	1	0	1	f_{OSC} / 6
						0	0	1	1	0	f_{OSC} / 7
						0	0	1	1	1	f_{OSC} / 8
						0	1	0	0	0	f_{OSC} / 9
						0	1	0	0	1	f_{OSC} / 10
						0	1	0	1	0	f_{OSC} / 11
						0	1	0	1	1	f_{OSC} / 12
						0	1	1	0	0	f_{OSC} / 13
						0	1	1	0	1	f_{OSC} / 14
						0	1	1	1	0	f_{OSC} / 15
						0	1	1	1	1	f_{OSC} / 16
						1	*	*	*	*	f_{OSC} / 32

Select LCD Bias *(Two-Byte instruction)*

Selects LCD bias ratio of the voltage required for driving the LCD.

Set LCD Bias select mode (First instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	1

Set LCD Bias select Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	LCD Bias
0	1	0	*	*	*	*	0	0	0	0	1/3
							0	0	0	1	1/3.5
							0	0	1	0	1/4
							0	0	1	1	1/4.5
							0	1	0	0	1/5
							0	1	0	1	1/5.5
							0	1	1	0	1/6
							0	1	1	1	1/6.5
							1	0	0	0	1/7
							1	0	0	1	1/7.5
							1	0	1	0	1/8

Display ON/OFF

This is the instruction for controlling the turning on or off the LCD panel regardless of the contents of the DDRAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display On or Off
1	1	0	1	0	1	0	1	1	1	0	0 :Off
										1	1 :On

Initial Display Line

Sets the line address of display RAM to determine the initial display line. The initial display line corresponds to COM0.The display area read from the display data RAM corresponds to the number of the lines set by the Duty select command.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address for COM0
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	0	1	0	0	0	40
					1	0	1	0	0	1	41

Electronic Contrast Control Set *(Two-Byte instruction)*

Consists of 2-byte instruction. The first instruction sets contrast control mode, the second one updates the contents of contrast control register. After second instruction, contrast control mode is released. The LSI can't accept any instructions except the "Set Contrast Control Register" during the Contrast Control Mode.

Sets Contrast Control Mode (First instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Set Contrast Control Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Electronic volume value (α)
0	1	0	*	*	0	0	0	0	0	0	0 Minimum
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Set Page Address

Sets the page address of display data RAM from the microprocessor into the page address register. It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Along with the column address, the page address defines the address of the display RAM to write or read display data. Changing the page address doesn't effect to the display status. Page 6 is assigned to the icon display. D0 only is valid.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							.	.	.	.	.
							.	.	.	.	.
							0	1	1	0	6

Set Column Address

Sets the column address of display RAM from the microprocessor into the column address register. When accessing the display data RAM from the MPU, the column address is incremented. The incrementing of the column address is stopped at the address 65H.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Column address setting
0	1	0	0	0	0	1	A7	A6	A5	A4	Upper 4-bit
						0	A3	A2	A1	A0	Lower 4-bit

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	0	0	1	0	0	100
0	1	1	0	0	1	0	1	101

ADC Select

This instruction selects segment driver direction. Normal or reverse can be selected for the correlation between the column address of the display data RAM and the segment output terminal.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Segment driver direction
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

D0 = 0 Normal Column addresses 00H to 65H correspond to segment outputs 0 to 101.

= 1 Reverse Column addresses 00H to 65H correspond to segment outputs 101 to 0.

Inverse Display ON/OFF

The instruction is used to invert the display status on LCD panel without rewriting the contents of the display data RAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display status
0	1	0	1	0	1	0	0	1	1	0	Normal
										1	Inverse

D0 = 0 Normal Display data “1” makes the LCD on.
= 1 Inverse Display data “0” makes the LCD on.

Entire Display ON/OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM will be retained. This instruction has priority over the Reverse Display On/Off instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Entire display on/off
0	1	0	1	0	1	0	0	1	0	0	Normal
										1	Entire display on

Set Modify-read

This instruction stops the automatic increment of the column address by the Read Display Data instruction, but the column address is still increased by the Write Display Data instruction. This instruction can reduce the load of MPU, during the display data in specific DDRAM area is repeatedly changed for cursor blink or others. This mode is canceled by the Reset Modify-read instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Reset Modify-read

This instruction cancels the Modify-read mode. The column address of the display data RAM returns to the address before Read Modify Write is executed.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the /RES pin.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Reset status by “Reset” instruction:

1. Read modify write off
2. Static indicator off and static indicator register: (S1,S0)=(0,0)
3. Initial display line address : (00)H
4. Column address : (00)H
5. Page address : (0) page
6. SHL select : Normal mode (D3=0)
7. Regulator resistor select register: (R2,R1,R0)=(0,0,0)
8. Sets contrast control set mode off and contrast control register : (20)H

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Common driver direction
0	1	0	1	1	0	0	0 1	*	*	*	Normal Reverse

D3 =0 Normal Normal direction (COM0 → COM 41)

=1 Reverse Reverse direction (COM41 → COM 0)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	VC	VR	VF

VC: Voltage converter

VR: Voltage regulator

VF: Voltage follower

0: Off 1: ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See

voltage regulator section in power supply circuit for more details.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb/Ra] Ratio
0	0	0	Small
0	0	1	…
..	..	..	..
1	1	0	..
1	1	1	Large

Set Static Indicator status *(Two-Byte instruction)*

Consists of two bytes instruction. The first byte instruction (Set Static Indicator Mode) enables the second byte instruction (Set Static Indicator Register) to be valid. The first byte sets the static indicator on/off. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

Set Static Indicator Mode (First instruction)

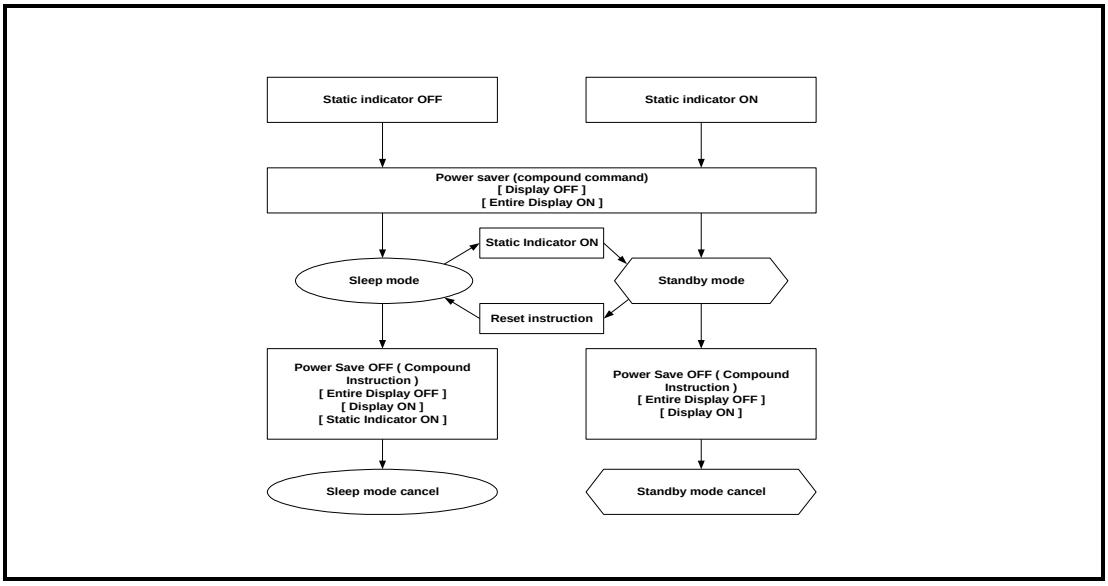
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	Off
										1	On

Set Static Indicator Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Status
0	1	0	*	*	*	*	*	*	0	0	Off
									0	1	On（Blink at 4 frame intervals ）
									1	0	On（Blink at 2 frame intervals ）
									1	1	On（Turn on at all time ）

Power Save *(compound instruction)*

The current consumption can be greatly reduced by entering the power save status by inputting the “Entire Display ON” instruction while the display is in OFF mode. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When Static Indicator mode is ON, *standby mode* is issued, when OFF, *sleep mode* is issued. Power Save mode is released by the “Display ON” & “Entire Display OFF” instruction.



Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

1. The oscillator circuit and the LCD power supply circuit are stopped.
2. All liquid crystal drive circuits are stopped, and the segment and common driver output VSS level.

When a “static indicator on” instruction is issued in the *sleep mode*, the LSI goes into the *standby mode*.

Standby Mode

All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:

1. The power supply circuit for LCD drive is stopped. The oscillator circuit will be operating.
2. The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the VSS level. The static display section will be operating.

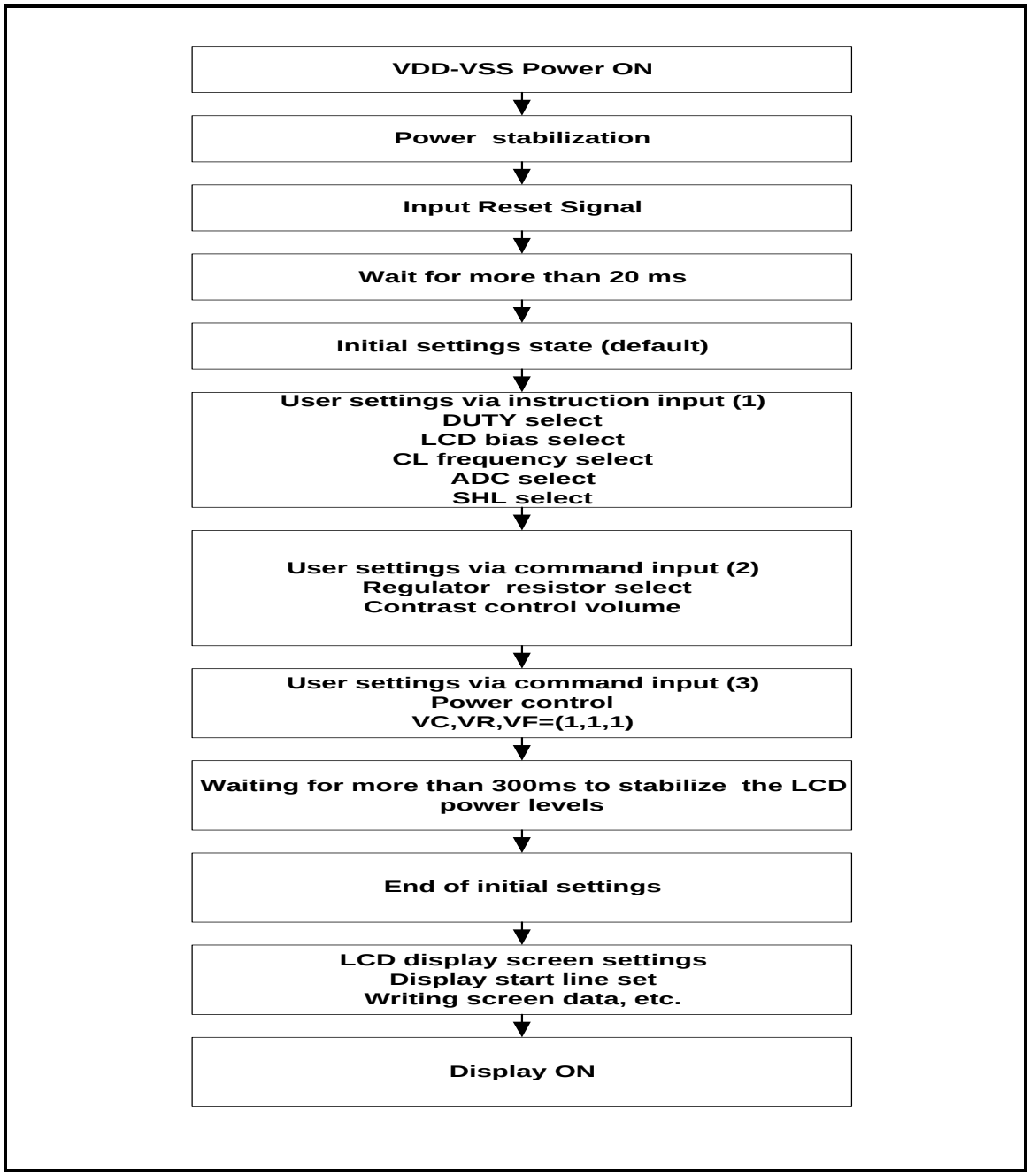
When a reset instruction is issued in the *standby mode*, the LSI goes into the *sleep mode*.

APPLICATION INFORMATION

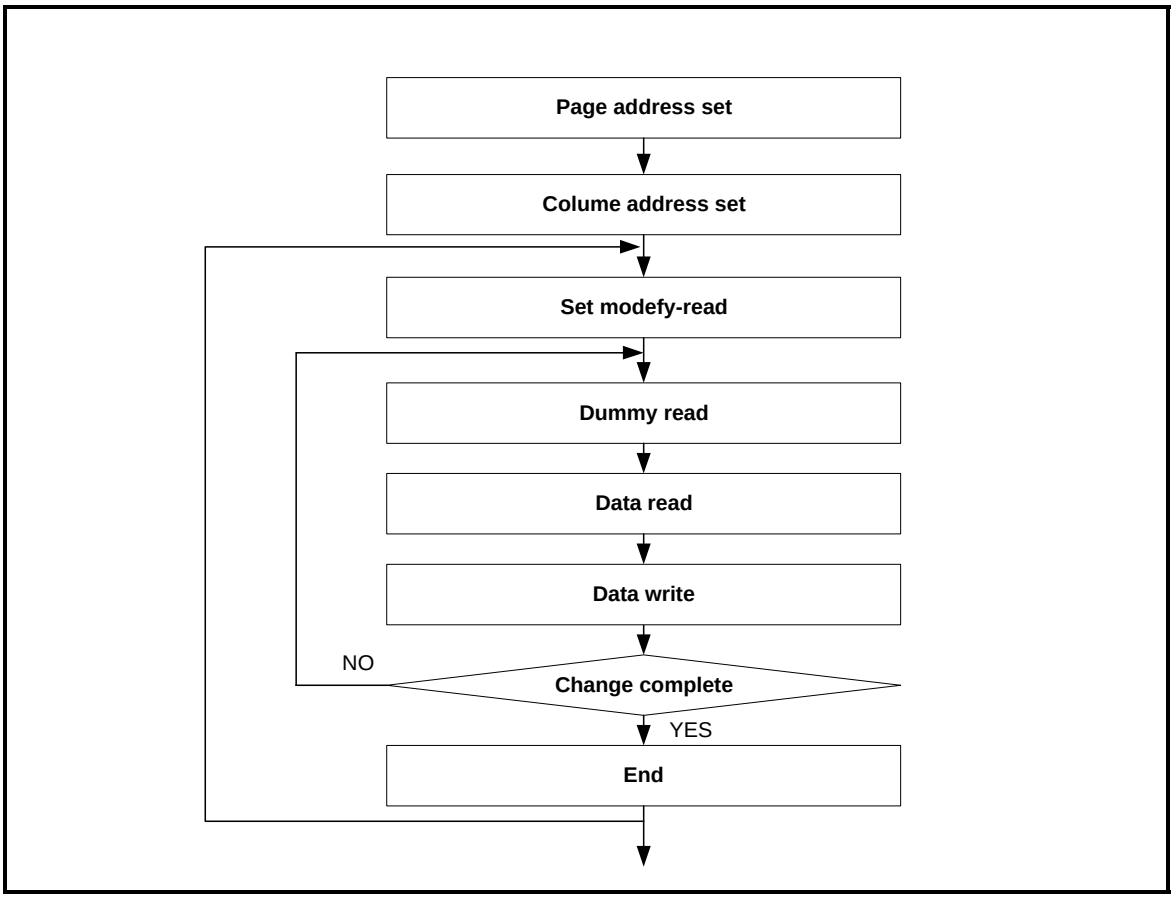
INSTRUCTION PROCEDURE EXAMPLES

Initial setup

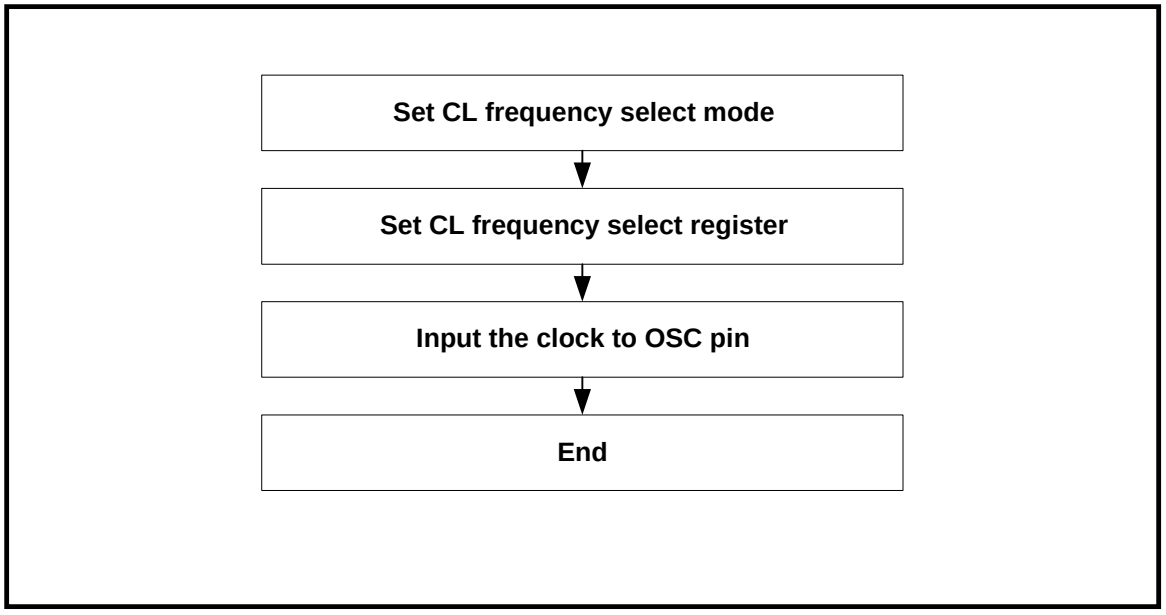
(From power application to display ON using internal power supply circuits)



The sequence of “Modify-read”



The sequence of “External oscillator input”



PROGRAM EXAMPLES

Use Elan Risc II MCU assembly

```
;*****************************************************************************
;       INITIALIZATION SETTING EXAMPLE OF EPL43102
;*****************************************************************************
INI_DRIVER_IC:
        MOV     A,#LCD_COM_RESET            ;INITIAL SETTINGS STATE (DEFAULT)
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_COM_DUTY             ;SET DUTY 1ST INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,#DUTY_SET                 ;SET DUTY 2ND INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_COM_BIAS             ;SET LCD BIAS 1ST INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,BIAS_SET                  ;SET BIAS 2ND INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_COM_FREQ              ;SET LCD CL FREQUENCY 1ST INSTRUCTION
```

```
        CALL    WRITE_LCD_1BYTE
        MOV     A,#CL_FREQ                      ;SET CL FREQUENCE 2ND INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_ADC_SET                  ;SET ADC FUNCTION SELECT
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_SHL_SET                  ;SET SHL FUNCTION SELECT
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_REGULATOR_RES_SET    ;SET REGULATOR RESISTOR 1+(Rb/Ra)
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_COM_CONTRAST         ;SET CONTRAST 1ST INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,#CONTRAST_SET             ;SET CONTRAST 2ND INSTRUCTION
        CALL    WRITE_LCD_1BYTE
        MOV     A,#LCD_POWER_CONTROL_SET    ;SET POWER CONTROL (INTERNAL OR EXTERNAL)
        CALL    WRITE_LCD_1BYTE
        BS      REG_CPUCON,F_CKS            ;ADD CLOCK BY OSC PIN (CLOCK FROM CPU)
        MOV     A,#150                      ;WAITING FOR STABILIZING THE LCD POWER
        CALL    WAIT_A_MS
        CALL    LCD_DISPLAY_ON              ;TURN ON LCD
        MOV     A,#LCD_DISPLAY_INI_LINE     ;SET INITIAL DISPLAY LINE
        CALL    WRITE_LCD_1BYTE
        CALL    LCD_DATA_WRITE              ;WRITING SCREEN DATA
        RET

********************************************************************************
;       WRITE DISPLAY_PICTURE DATA INTO DISPLAY DATA RAM OF EPL43102
;********************************************************************************
DATA_WRITE:
        TBPTL   #DISPLAY_PICTURE*2          ;DEFINE DISPLAY PICTURE DATA INDEX
        TBPTM   #DISPLAY_PICTURE/0x80
        TBPTH   #DISPLAY_PICTURE/0x8000
DATA_WRITE_43102:
        MOV     A,#LINE_Y_MAX               ;MAX PAGES OF DDRAM
        MOV     REG_LCDARH,A
```

```
DATA_W1:
        MOV     A,#LINE_X_MAX                   ;SET MAX SEGMENTS OF DDRAM
        MOV     REG_LCDARL,A
        BC      REG_PORTB,F_LCD_A0              ;SET LCD /A0 = 0 INSTRUCTION OUTPUT
        MOV     A,#LCD_COM_PAGE
        ADD     A,REG_LCDARH
        CALL    WRITE_LCD_1BYTE
        MOV     A,#0b00000000                   ;SET LOWER ORDER COLUMN ADDRESS=0000
        CALL    WRITE_LCD_1BYTE
        MOV     A,#0b00010000                   ;SET HIGHER ORDER COLUMN ADDRESS=0000
        CALL    WRITE_LCD_1BYTE
        BS      REG_PORTB,F_LCD_A0              ;SET LCD /A0 = 1 DATA OUTPUT
DATA_W2:
        TBRD    01,REG_ACC                      ;ACCESS THE DATA OF DISPLAY_PICTURE
        CALL    WRITE_LCD_1BYTE
        DEC     REG_LCDARL
        JBS     REG_STATUS,F_C,DATA_W2          ;IDENTIFY RES_STATUS CARRY BIT SET OR NOT
        DEC     REG_LCDARH
        JBS     REG_STATUS,F_C,DATA_W1
        BC      REG_PORTB,F_LCD_A0              ;LCD /A0 = 0 FOR INSTRUCTION OUTPUT
        RET
;*********************************************************************************
;       WRITE ONE BYTE DATA INTO DDRAM (PARALLEL MODE 80 SERIES)
;*********************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION WRITE
WRITE_LCD_1BYTE:
        JBS     REG_DCRG,F_LAHEN,WRITE_LCD_1BYTE_1      ;CHECK REG_DCRG LAHEN BIT=1 OR NOT
        BC      REG_PORTC,F_LCD_WR                      ;SET /WR=0 ENABLE WRITE
        MOV     REG_DATA,A                              ;MOVE A==> PORT_G
        NOP                                             ;Write low pulse( Wait 2 instruction cycles)
        NOP
        BS      REG_PORTC,F_LCD_WR                      ;SET /WR=1 DISABLE WRITE
        NOP
        NOP
```

```
        NOP
        NOP
        RET
WRITE_LCD_1BYTE_1:
        MOV     REG_DATA,A                          ;MOVE A==> PORT_G
        RET

;*************************************************************************
;
;       READ ONE BYTE DATA INTO DDRAM (PARALLEL MODE 80 SERIES)
;
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION READ
READ_LCD_1BYTE:
        BC      REG_PORTB,F_LCD_RD                  ;SET /RD=0 ENABLE READ
        NOP
        NOP
        MOV     A,REG_DATA                          ;MOVE PORT_G ==> A
        NOP
        BS      REG_PORTB,F_LCD_RD                  ;SET /RD=1 DISABLE READ
        NOP
        RET
```

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Applicable pins	Symbol	Condition	Rate value	Unit
Power supply voltage	VDD	V_{DD}	—	-0.3 to +7	V
Driver supply voltage	VOUT	V_{LCD}	—	-0.3 to +17	
Input voltage	ALL INPUT	V_{IN}	—	-0.3 to VDD+0.3	
Operating temperature range	—	T_A	—	-30 to +80	^{O}C
Storage temperature range	—		—	-55 to +125	

Recommended Operating Conditions

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min.	Typ.	Max.	
Power supply Voltage	VDD	V_{DD}	—	2.2	—	5.5	V
Voltage converter output voltage	VOUT	V_{OUT}	—	4.0	—	15	
V0 output voltage	V0	V_0	—	3.0	—	12	
Output voltage		V_{OH}	—	0.7VDD	—	VDD	
		V_{OL}	—	VSS	—	0.3VDD	
Input voltage		V_{IH}	—	0.7VDD	—	VDD	
		V_{IL}	—	VSS	—	0.3VDD	
Operating temperature range	—	T_A	—	0		40	^{O}C

DC Characteristics

(VSS=0V, VDD=2.6 to 3.3V, T_A= -30~80 °C)

Parameter	Applicable Pins	Symbol	Condition	Rated value			Unit
				Min.	Typ.	Max.	V
Power supply voltage	VDD	V_{DD}		2.2	—	5.5	
Voltage converter input voltage	VDD	V_{DD2}	2 x boost	2.2	—	5.5	
	VDD	V_{DD3}	3 x boost	2.2	—	5.0	
	VDD	V_{DD4}	4 x boost	2.2	—	3.75	
	VDD	V_{DD5}	5 x boost	2.2	—	3.0	
Reference voltage	—	V_{REF0}	T_A=0 °C	2.07	2.16	2.25	
		V_{REF20}	T_A=20 °C	1.96	2.05	2.14	
		V_{REF40}	T_A=40 °C	1.86	1.94	2.02	
Regulated voltage	V0 (*1)	V_0	T_A=0~40 °C	V0-4%	V0	V0+4%	
OP Amp voltage output of LCD power supply	V0	V_{OUT0}	No load (*2) (*3)		V0		mV
	V1	V_{OUT1}			V1		
	V2	V_{OUT2}			V2		
	V3	V_{OUT3}			V3		
	V4	V_{OUT4}			V4		
Voltage converter output voltage	VOUT	V_{OUT}	x2/x3/x4/x5 no-load	95	99	100	%
LCD driver ON resistance	COMn SEGn	R_{ON}	Current load I_{load}= 50 μA	—	2	5	kΩ
Reset resistor	/RES	R_{RESET}	VDD=3V, Vin=0V	400	800	1200	
			VDD=3V, Vin=1.7V	25	50	75	
Output current (Source and Drain)	(*5)	I_{OH}	VDD=3V, V_{OH}=2.4V	-3	-4	-5	mA
		I_{OL}	VDD=3V, V_{OL}=0.2V	1.2	2.2	3.2	
Input leakage current	All Input (*4)	I_{IL}	V_{IN}= VDD or 0V	—	—	±1	μA
Output Tri-state	(*5)					± 3	
Dynamic current consumption (1/43 duty)		I_{DDD1}	VDD=3V, five boosting, T_A=25 °C, internal OSC. f_{OSC}=22kHz ,1/43 duty ratio, all display pattern off, no load	—	70	100	
Dynamic current consumption (1/32 duty)		I_{DDD2}	VDD=3V, double boosting, T_A=25 °C, external OSC,. f_{OSC}=22kHz,1/32 duty ratio, all display pattern off, no load	—	40	55	
V1 sink ability	V1	Isv1	V0=3.6V, V1=2.4V (No load) VOH=2.8V	0.75	1	—	
V4 source ability	V4	Isv4	V0=3.6V, V4=1.2V (No load) VOL=0.8V	-0.75	-1	—	
Current consumption		I_{DDs1}	Standby mode	—	5	10	

Current consumption		I_{DDS2}	Sleep mode	—	1	2	
Frame frequency		f_{FM}		—	85	—	Hz
Internal Oscillator frequency	—	f_{OSC}	T_A=25 °C	17	22	27	kHz
External input Oscillator	OSC	f_{OSC}	T_A=25 °C	—	22	—	

Note1: $V0 = (1 + \frac{Rb}{Ra}) \times VEV$; $VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF$

Note2:

LCD Bias	V0	V1	V2	V3	V4
1/8 Bias		(7/8)XV0	(6/8)XV0	(2/8)XV0	(1/8)XV0
1/7.5 Bias		(6.5/7.5)XV0	(5.5/7.5)XV0	(2/7.5)XV0	(1/7.5)XV0
1/7 Bias		(6/7)XV0	(5/7)XV0	(2/7)XV0	(1/7)XV0
1/6.5 Bias		(5.5/6.5)XV0	(4.5/6.5)XV0	(2/6.5)XV0	(1/6.5)XV0
1/6 Bias		(5/6)XV0	(4/6)XV0	(2/6)XV0	(1/6)XV0
1/5.5 Bias		(4.5/5.5)XV0	(3.5/5.5)XV0	(2/5.5)XV0	(1/5.5)XV0
1/5 Bias		(4/5)XV0	(3/5)XV0	(2/5)XV0	(1/5)XV0
1/4.5 Bias		(3.5/4.5)XV0	(2.5/4.5)XV0	(2/4.5)XV0	(1/4.5)XV0
1/4 Bias		(3/4)XV0	(2/4)XV0	(2/4)XV0	(1/4)XV0
1/3.5 Bias		(2.5/3.5) XV0	(1.5/3.5)XV0	(2/3.5)XV0	(1/3.5)XV0
1/3 Bias		(2/3)XV0	(1/3)XV0	(2/3)XV0	(1/3)XV0

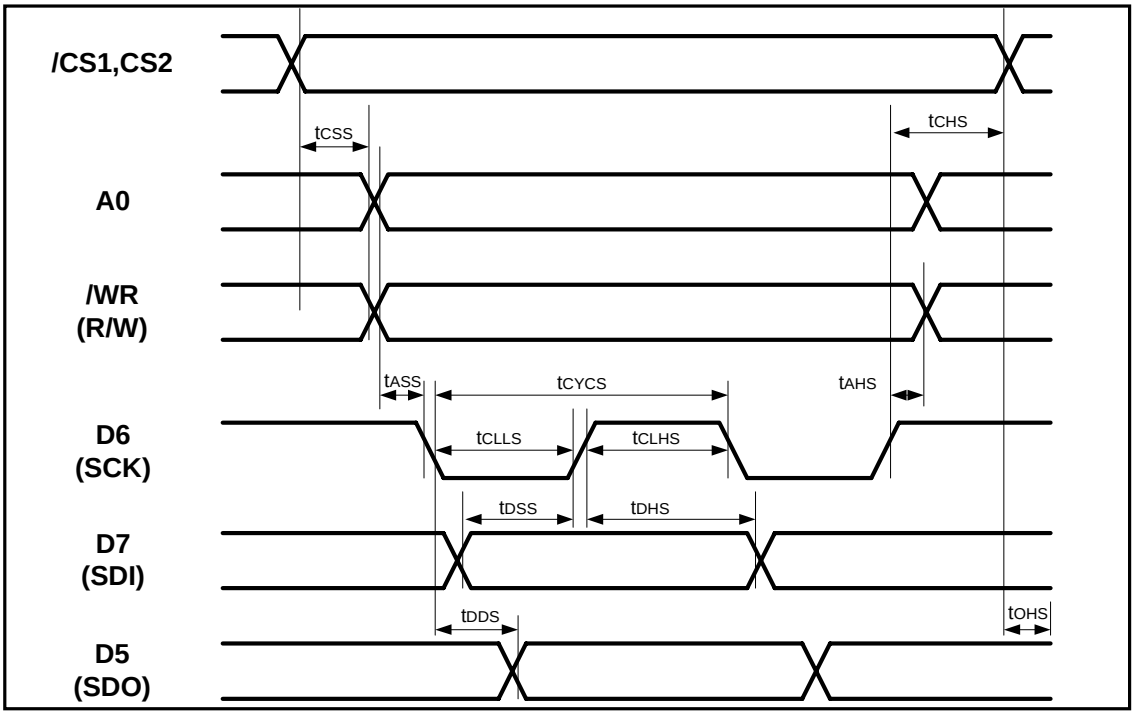
Note3: The target value of V0~V4 is Theoretical Value +/- 50mV

Note4: Input pin D0~D7、A0、/RD、/WR、/CS1、CS2、CLS、M/S、C86、P/S、IRS

Note5: Output pin D0~D7、FR、FRS、/DOF、CL

AC Characteristics

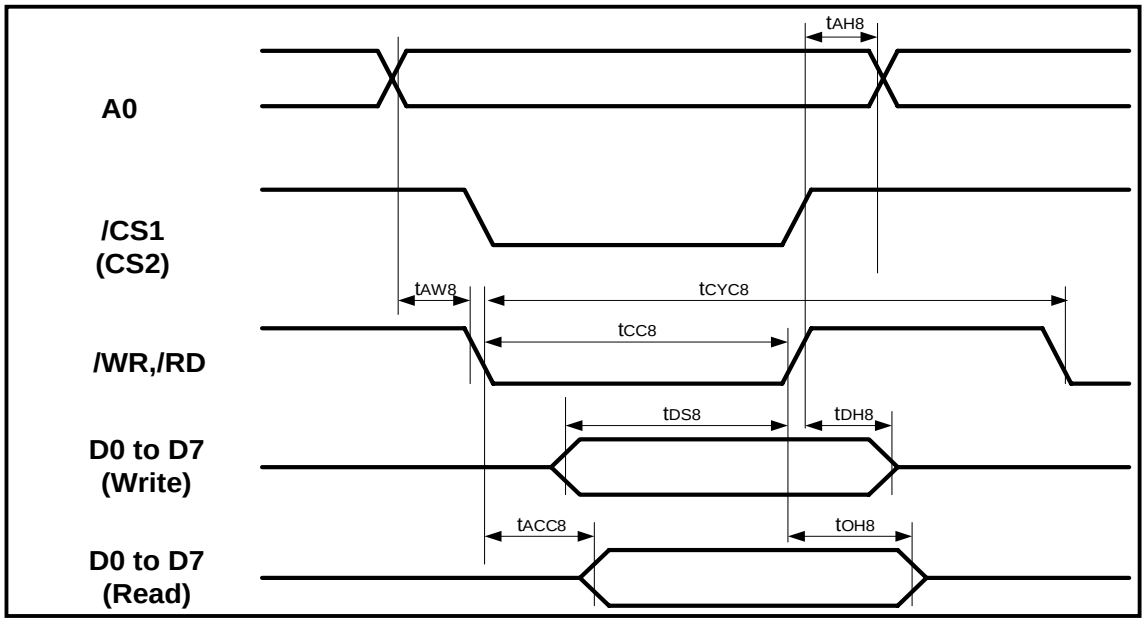
Serial Interface Timing Characteristics



Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	ns
Chip Select Setup Time Chip Select Hold Time	/CS1 CS2	t_{CSS} t_{CHS}		100 100	—	
Address Setup time Address Hold time	A0 R/W	t_{ASS} t_{AHS}		100 100	—	
Data Setup Time Data Hold Time	D7 (SDI)	t_{DSS} t_{DHS}	DATA→SCK↑ SCK↑→DATA	80 80	—	
Clock Cycle Time Clock L Time Clock H Time	D6 (SCK)	t_{CYCS} t_{CLLS} t_{CLHS}		300 100 100	—	
Data Delay Time Data Disable Time	D5 (SDO)	t_{DDS} t_{OHS}	C_L= 100 pF	 10	80 50	

(VSS= 0V,VDD= 2.6~3.3 V, T_A=0~40°C)

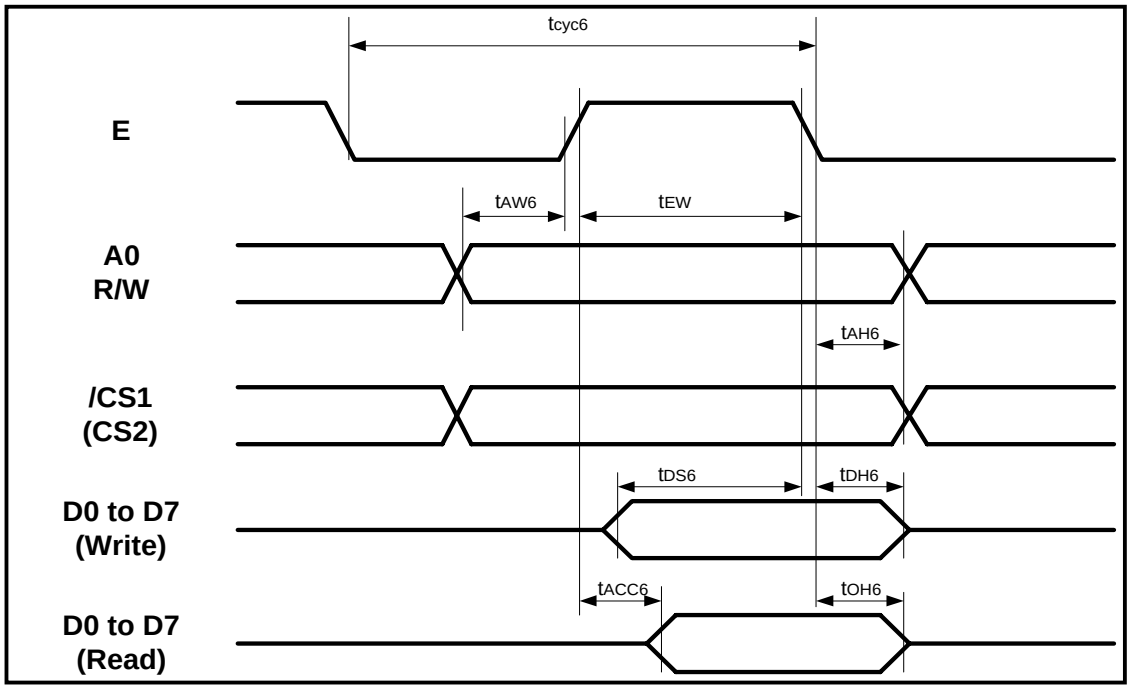
80-Family MPU Read/Write Timing Characteristics



Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	ns
Address Setup Time	A0	t_{AW8}		0	—	
Address Hold Time		t_{AH8}		0		
System Cycle Time	A0	t_{CYC8}		500	—	
Pulse Width(/WR)	/WR	t_{CC8}		160	—	
Pulse Width(/RD)	/RD			200		
Data Setup Time	D0~D7	t_{DS8}		20	—	
Data Hold Time		t_{DH8}		10		
Read Access Time		t_{ACC8}	C_L=100pF	—	60	
Output Disable Time		t_{OH8}		10	40	

(VSS= 0V,VDD= 2.6~3.3 V, T_A=0~40^{o}C)

68-Family MPU Read/Write Timing Characteristics

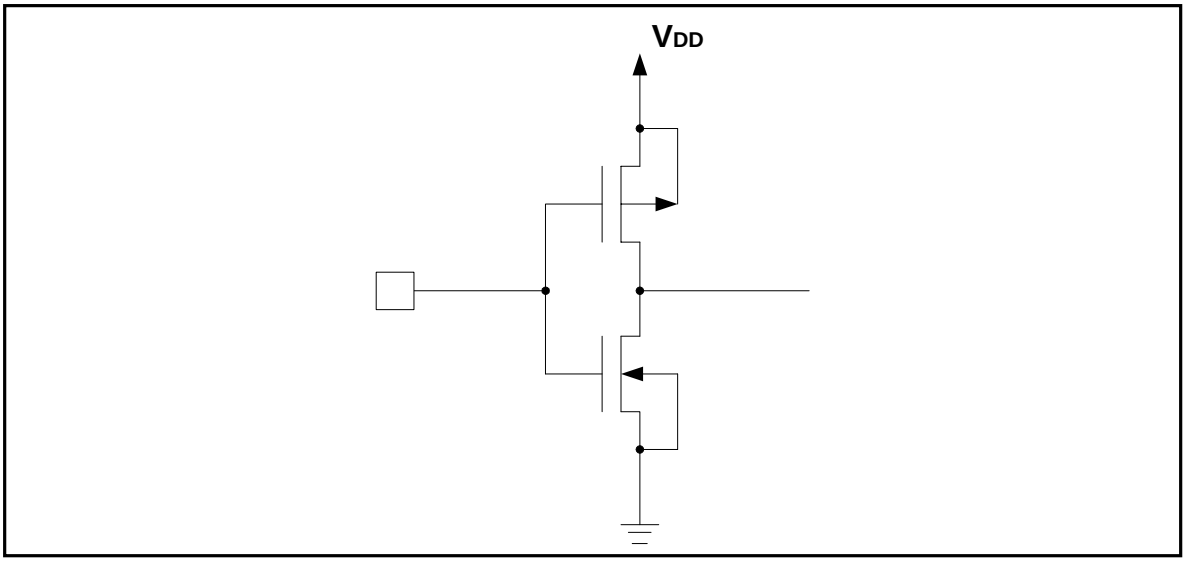


Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	ns
Address Setup Time Address Hold Time	A0 R/W	t_{AW6} t_{AH6}		0 0	—	
System Cycle Time	A0	t_{CYC6}		500	—	
Pulse Width(/WR) Pulse Width(/RD)	E	t_{EW}		160 200	—	
Data Setup Time Data Hold Time	D0~D7	t_{DS6} t_{DH6}		20 10	—	
Read Access Time Output Disable Time		t_{ACC6} t_{OH6}	C_L=100pF	— 10	60 40	

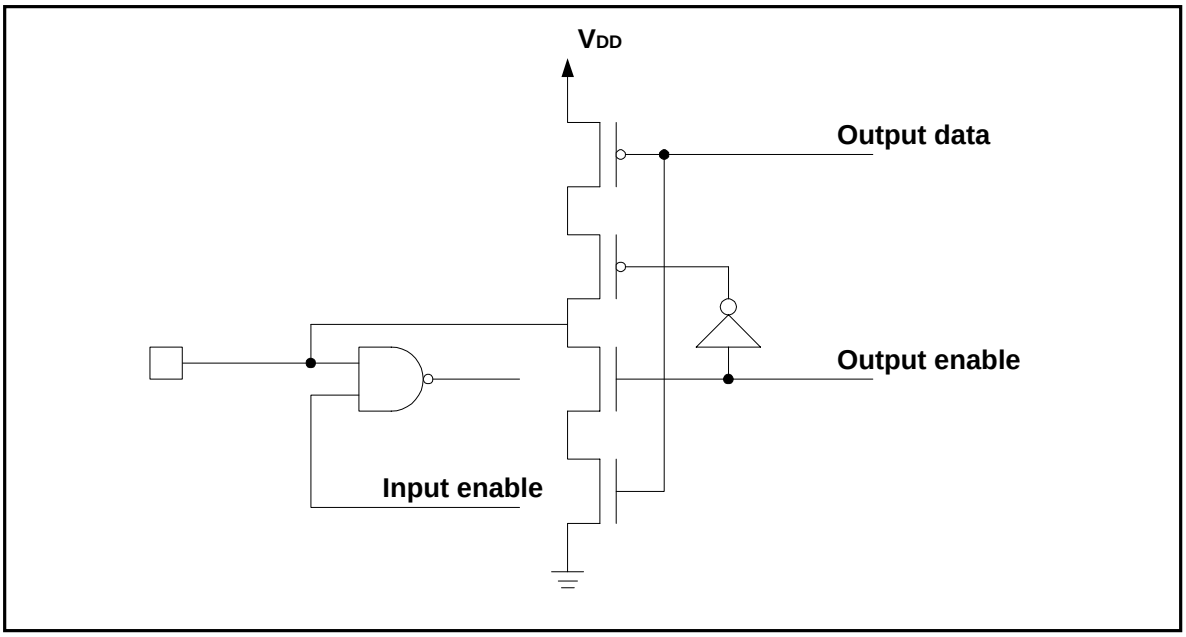
(VSS= 0V,VDD= 2.6~3.3 V, T_A=0~40^{o}C)

PIN CONFIGURATION

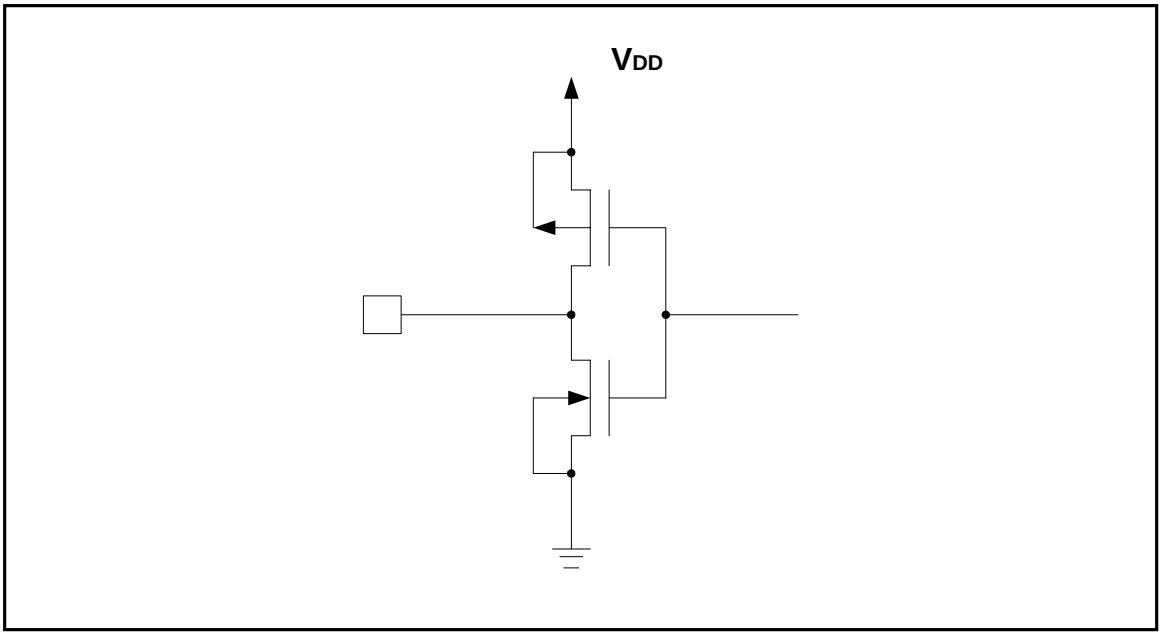
INPUT PIN CONFIGURATION



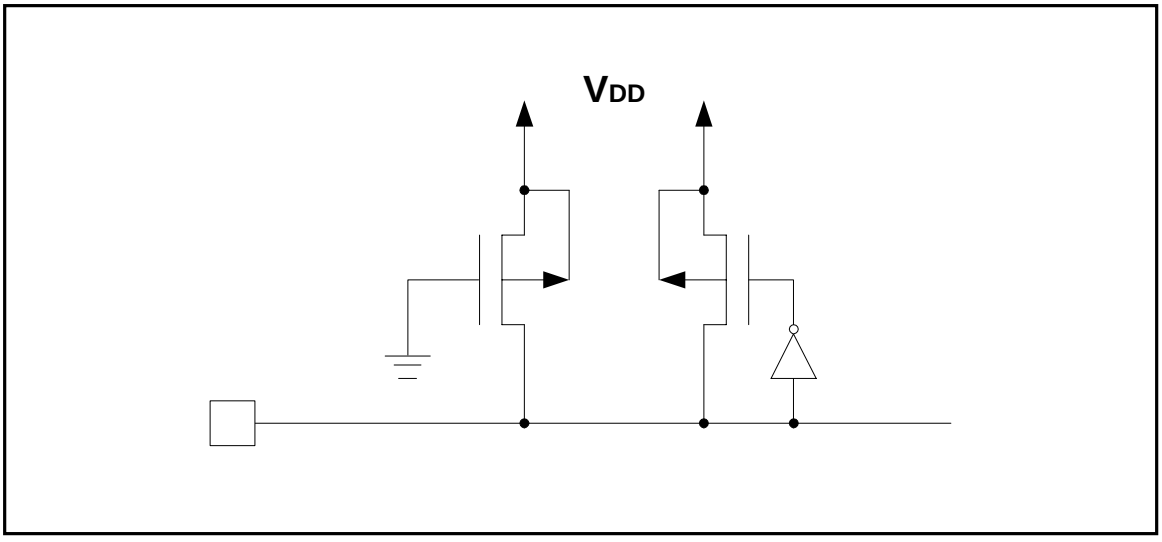
INPUT/OUTPUT PIN CONFIGURATION



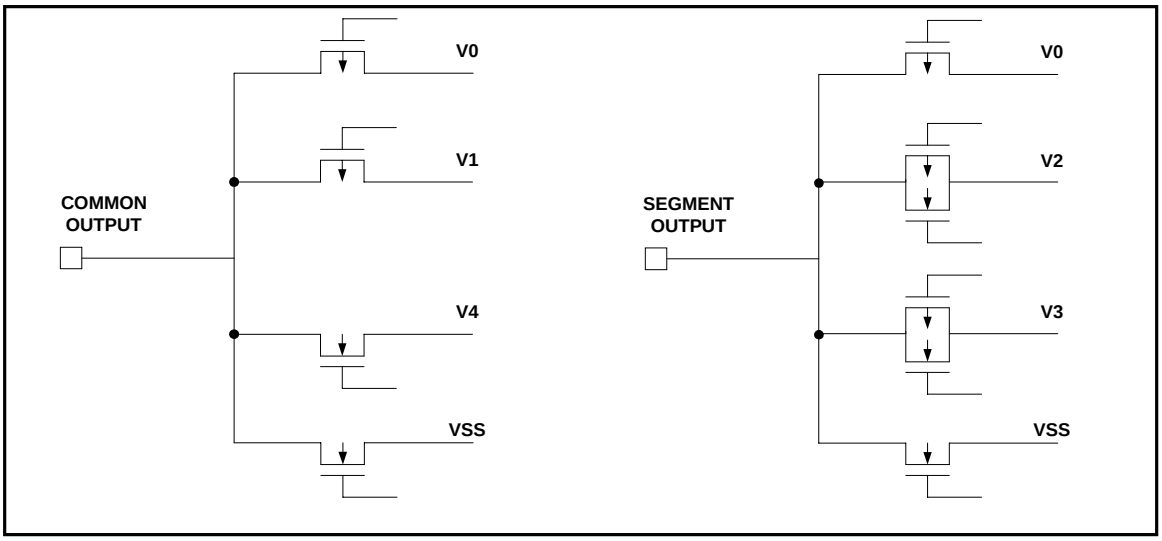
OUTPUT PIN CONFIGURATION



RESET INPUT PIN CONFIGURATION

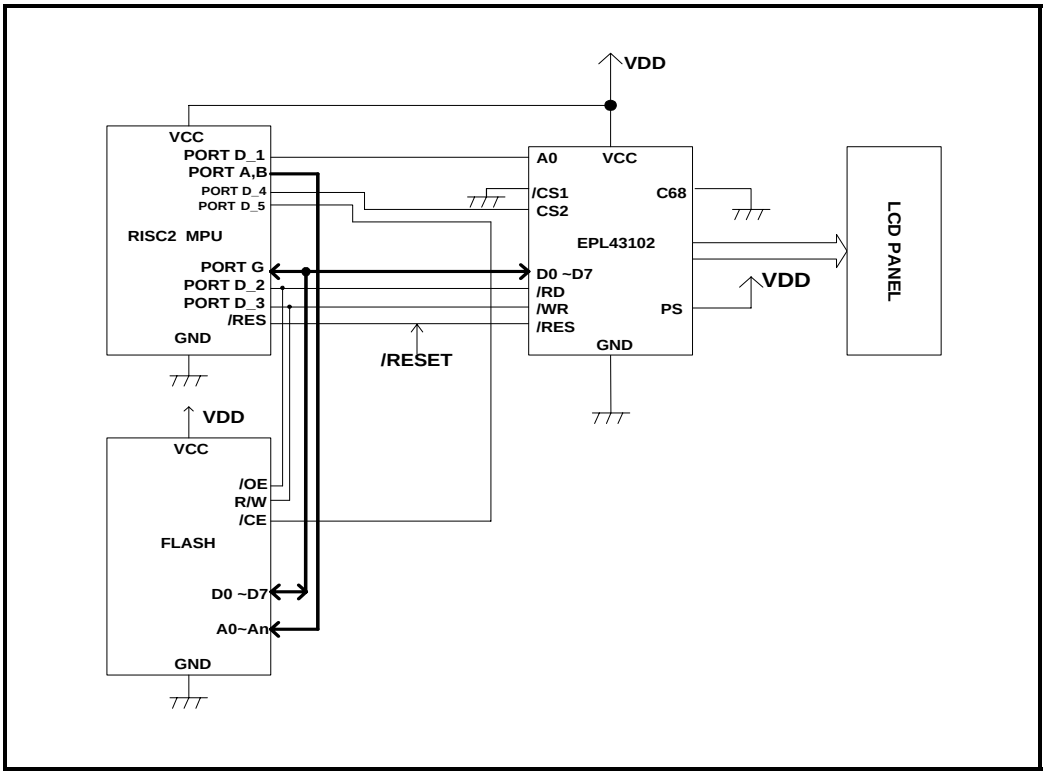


LCD OUTPUT PIN CONFIGURATION

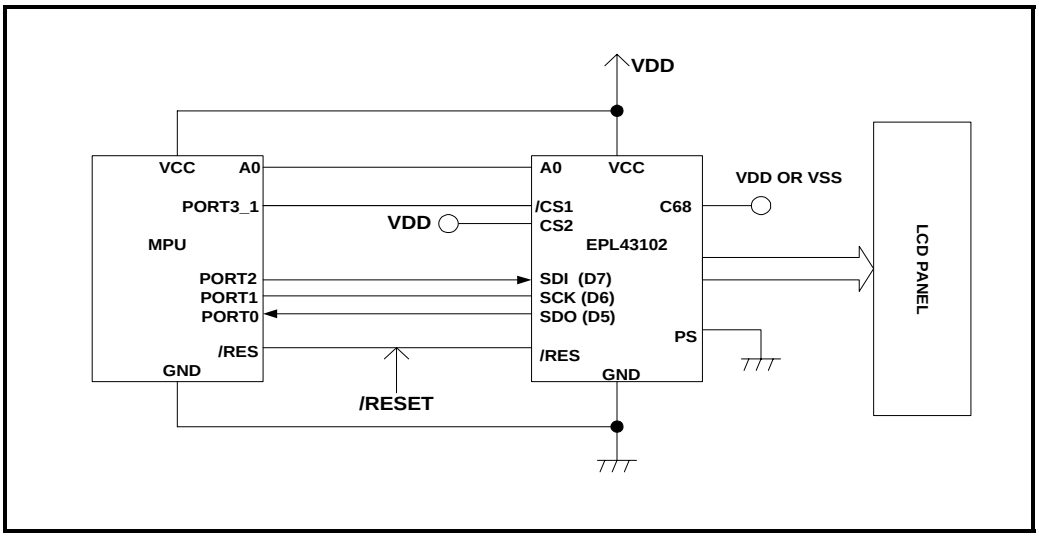


MPU INTERFACE

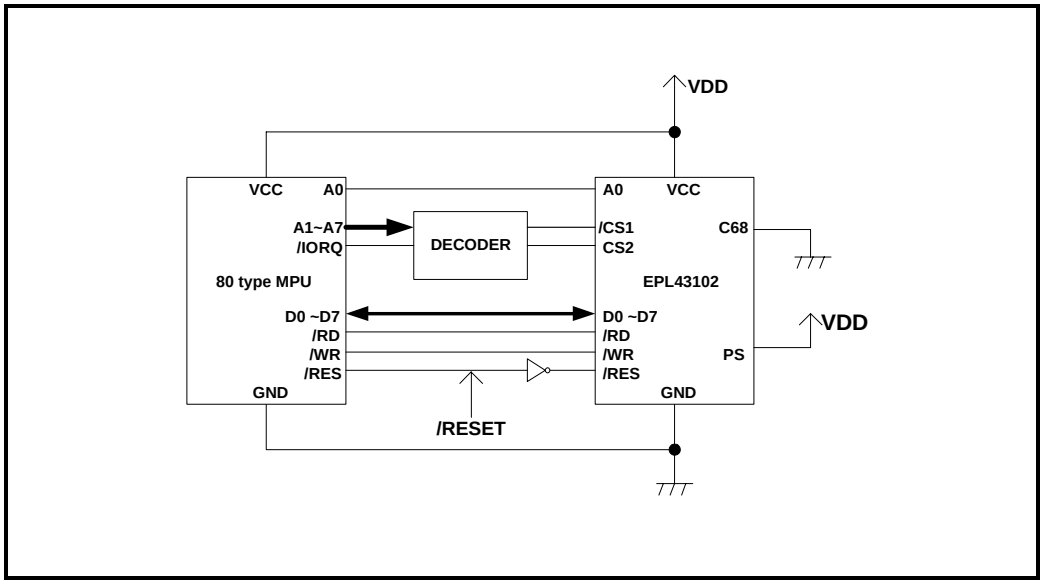
Elan 8-bit MPU (with an external memory)



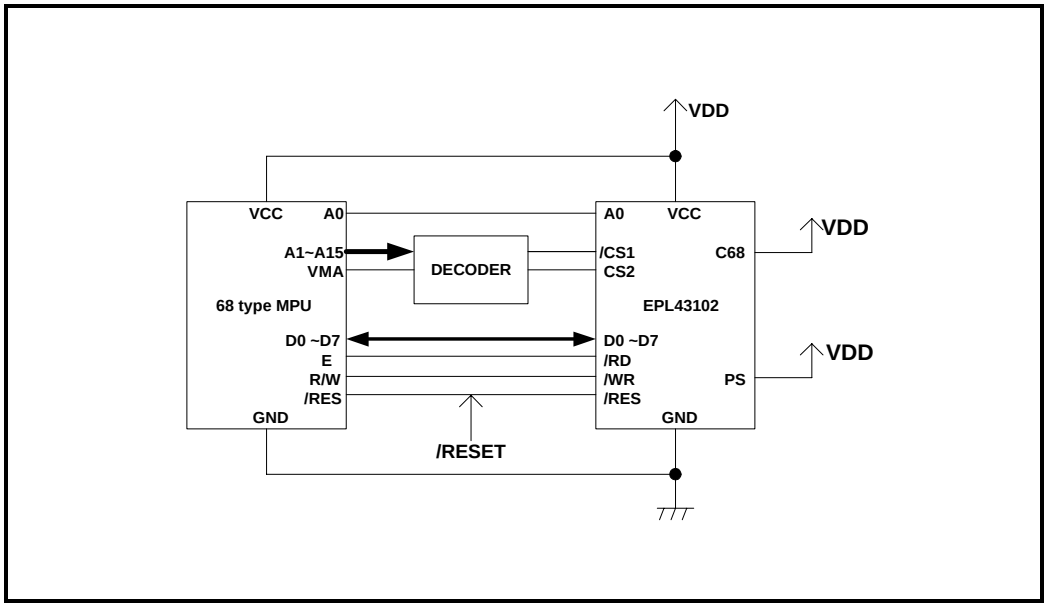
Serial Interface (SPI)



80-Family MPU



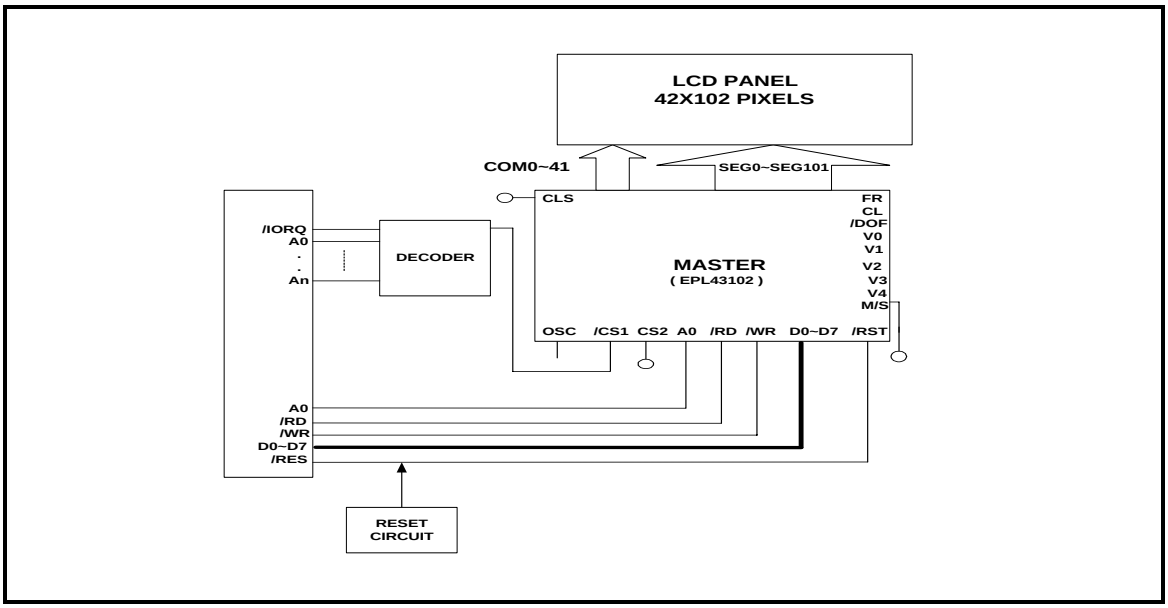
68-Family MPU



APPLICATION CIRCUITS

Example 1:

42x102 pixels driving application circuits (“Single-chip” using internal oscillator)



Example 2:

43x204 pixels driving application circuits (“Multi-chip” using external oscillator)