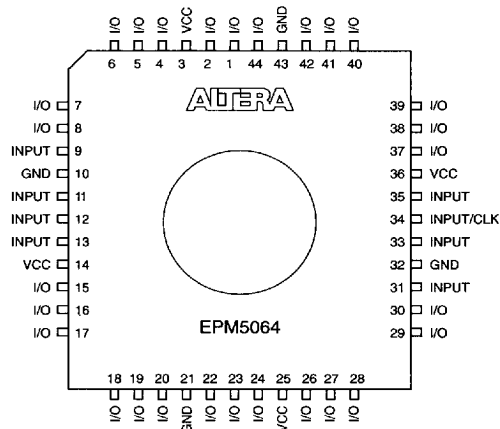


Features

- High-density, 64-macrocell, general-purpose MAX 5000 EPLD
- High-speed multi-LAB architecture
 - t_{PD} as fast as 15 ns
 - Counter frequencies up to 83.3 MHz
 - Pipelined data rates up to 100 MHz
- 128 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 36 inputs or 28 outputs
- Available in 44-pin windowed ceramic and one-time-programmable (OTP) J-lead chip carrier (JLCC and PLCC) packages, see Figure 11
- Easy integration of 10 standard PALs in 1/2-square-inch of board space
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 11. EPM5064 Package Pin-Out Diagram

Package outline not drawn to scale. Windows in ceramic packages only.



44-Pin J-Lead

General Description

Altera EPM5064 EPLDs are user-configurable, high-performance MAX 5000 EPLDs that serve as high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. In addition, these devices can integrate multiple 20- and 24-pin low-density PLDs. For example, the EPM5064 can integrate the logic contained in over 10 standard 20-pin PALs.

The EPM5064 consists of 64 macrocells equally divided into 4 Logic Array Blocks (LABs) with 16 macrocells. Each LAB also contains 32 expander product terms. They each have 8 dedicated input pins, one of which can be used as a global system Clock that provides enhanced Clock-to-output delays. The device has 28 I/O pins that can be configured for input, output, or bidirectional operation. All I/O pins feature dual-feedback for maximum pin flexibility. Two of the LABs have 8 I/O pins, ensuring high speed for 8-bit bus functions; the other two LABs have 6 I/O pins. See Figure 12.

Figure 12. EPM5064 Block Diagram

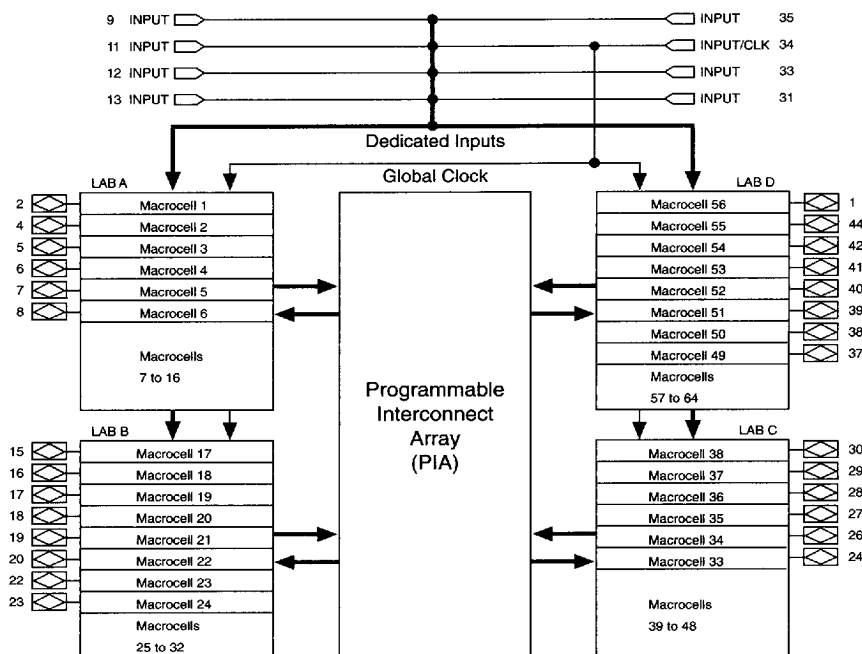
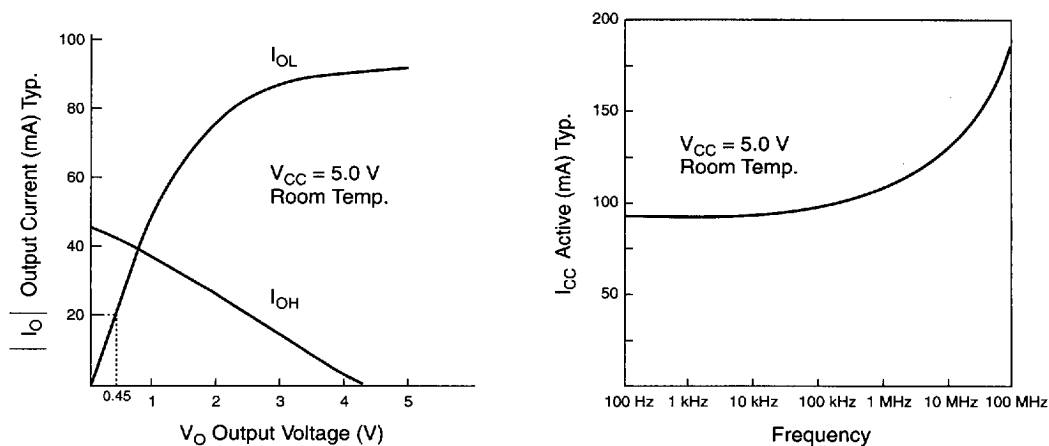


Figure 13 shows the output drive characteristics of EPM5064 I/O pins and typical supply current (I_{CC}) versus frequency. The high integration density of this device can greatly reduce system power requirements.

Figure 13. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-2.0	7.0	V
V_I	DC input voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		-25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	Notes (2),(3)	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	-40	85	°C
T_C	Case temperature	For military use	-55	125	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions Notes (4), (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level TTL output voltage	$I_{OH} = -4$ mA DC	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	-10		10	μA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	-40		40	μA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, Notes (2), (6)		90	125 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, no load, $f = 1.0$ MHz, Notes (2), (6)		95	135 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
C_{IO}	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		20	pF

AC Operating Conditions Note (5)

External Timing Parameters			EPM5064A-15		EPM5064A-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	$C1 = 35 \text{ pF}$		15		20	ns
t_{PD2}	I/O input to non-registered output	$C1 = 35 \text{ pF}$		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_H	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	$C1 = 35 \text{ pF}$		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	$C1 = 35 \text{ pF}$		15		20	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	Note (6)	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	Note (6)	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	Note (8)	100.0		71.4		MHz

Internal Timing Parameters Note (9)			EPM5064A-15		EPM5064A-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	$C1 = 35 \text{ pF}$		3		3	ns
t_{ZX}	Output buffer enable delay	$C1 = 35 \text{ pF}$		5		5	ns
t_{XZ}	Output buffer disable delay	$C1 = 5 \text{ pF}$		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_H	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Programmable Interconnect Array delay			10		13	ns

AC Operating Conditions Note (5)

External Timing Parameters			EPM5064-1		EPM5064-2		EPM5064		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	$C1 = 35 \text{ pF}$		25		30		35	ns
t_{PD2}	I/O input to non-registered output	$C1 = 35 \text{ pF}$		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_H	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	$C1 = 35 \text{ pF}$		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	$C1 = 35 \text{ pF}$		25		30		35	ns
t_{ACH}	Array clock high time	Note (7)	11		14		16		ns
t_{ACL}	Array clock low time	Note (7)	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	Note (6)	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	Note (6)	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	Note (8)	62.5		50		40		MHz

Internal Timing Parameters Note (9)			EPM5064-1		EPM5064-2		EPM5064		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	$C1 = 35 \text{ pF}$		5		5		6	ns
t_{ZX}	Output buffer enable delay	$C1 = 35 \text{ pF}$		10		11		13	ns
t_{XZ}	Output buffer disable delay	$C1 = 5 \text{ pF}$		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_H	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

- (1) Minimum DC input is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- (2) Numbers in parentheses are for military- and industrial-temperature-range versions.
- (3) Maximum V_{CC} rise time for the EPM5064/EPM5064A is 200 ms.
- (4) Typical values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{ V}$.
- (5) Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C for commercial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C for industrial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_C = -55^\circ\text{C}$ to 125°C for military use.
- (6) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0°C .
- (7) This parameter is measured with a positive-edge-triggered Clock at the register.
 For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
- (8) The f_{MAX} values represent the highest frequency for pipelined data.
- (9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.