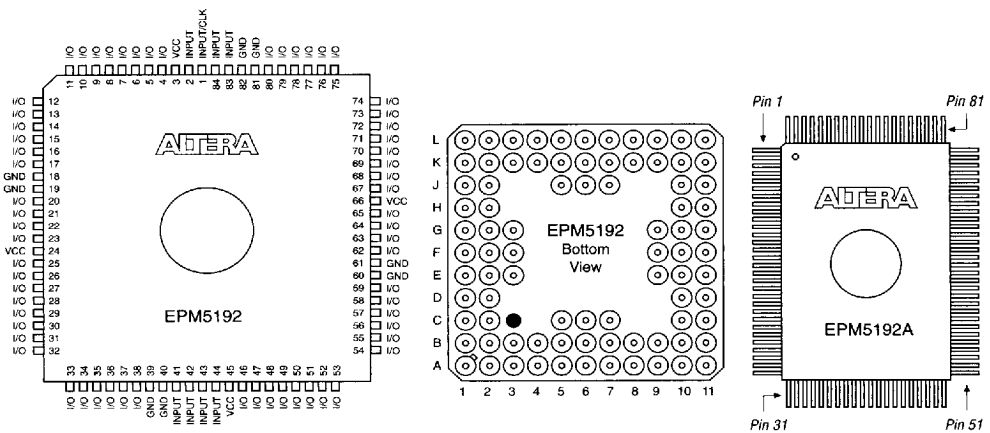
Features

- High-density, 192 macrocell, general-purpose MAX 5000 EPLD, easily integrating complete logic boards into a single package
- High-speed multi-LAB architecture
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 83.3 MHz
  - Pipelined data rates up to 100 MHz
- 384 shareable expander product terms ("expanders") offering flexibility for register and combinatorial logic expansion
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs, and I/O tri-state buffers that facilitate connections to system buses
- Available in 84-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 20):
  - 84-pin J-lead chip carrier (JLCC and PLCC)
  - 84-pin ceramic pin-grid array
  - 100-pin plastic quad flat pack (EPM5192A only)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 20. EPM5192 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 8 and 9 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead | 84-Pin PGA | 100-Pin QFP

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General Description

Altera EPM5192 EPLDs are user-configurable, high-performance MAX 5000 EPLDs that provide high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. They can replace over 100 TTL SSI and MSI components and integrate the logic of over 20 22V10 devices. The EPM5192 consists of 192 macrocells equally divided into 12 Logic Array Blocks (LABs), each with 16 macrocells and 32 expanders. These compact LABs maintain high performance and efficient use of device resources. Each of these devices have 8 dedicated input pins, one of which can be used as a global Clock. They can mix global and array clocking, facilitating easy integration of multiple subsystems. The EPM5192 contains 64 I/O pins that can be configured for input, output, or bidirectional operation, providing an interface for high-speed, bus-oriented applications. See Figure 21.

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Figure 21. EPM5192 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages. Numbers in brackets are for EPM5192A QFP packages.

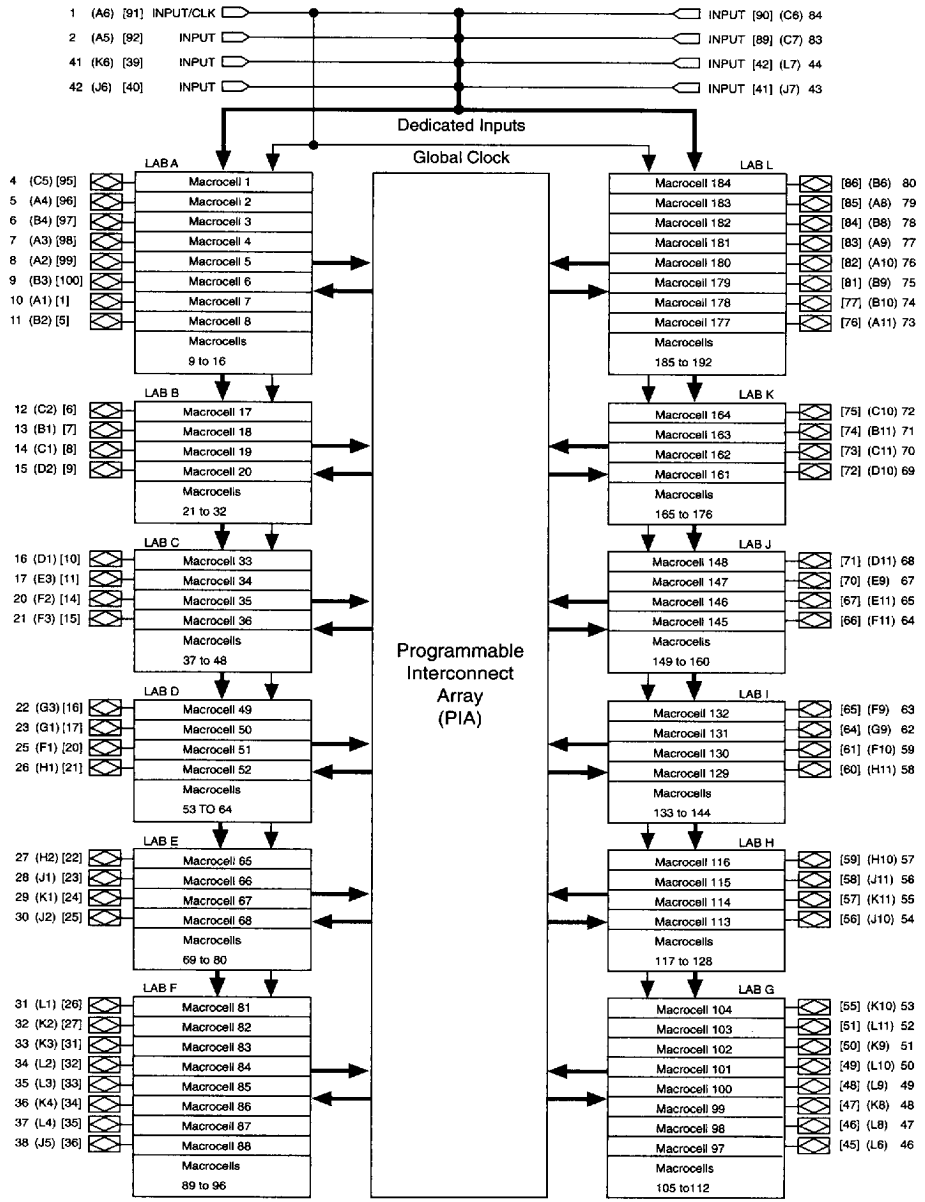

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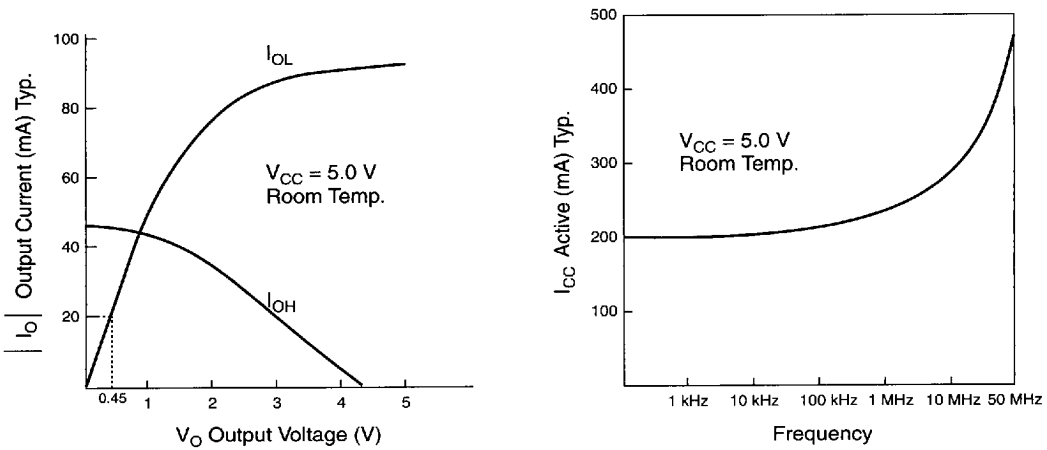
Figure 22 shows the output drive characteristics of EPM5192 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 22. Typical Output Drive Characteristics & I_{CC} vs. Frequency



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Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (7)*		250	360 (435)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, no load, f = 1.0 MHz, *Notes (3), (7)*		270	380 (480)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

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AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5192A-15		EPM5192A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	100.0		71.4		MHz

Internal Timing Parameters *Note (10)*			EPM5192A-15		EPM5192A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Prog. Interconnect Array delay			10		13	ns

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AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (8)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (8)*	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	62.5		50		40		MHz

Internal Timing Parameters *Note (10)*			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

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Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Maximum V_{CC} rise time for the EPM5192/EPM5192A is 200 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(6) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(7) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Pin-Out Information

Tables 8 and 9 provide pin-out information for the EPM5192.

Table 8. EPM5192 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
INPUT/CLK	1	A6	91
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6	39, 40, 41, 42
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5	2, 3, 4, 12, 13, 28, 29, 30, 37, 38, 52, 53, 54, 62, 63, 78, 79, 80, 87, 88
VCC	3, 24, 45, 66	B5, E10, G2, K7	18, 44, 68, 69, 93, 94

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Table 9. EPM5192 I/O Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
1	A	4	C5	95	17	B	12	C2	6
2	A	5	A4	96	18	B	13	B1	7
3	A	6	B4	97	19	B	14	C1	8
4	A	7	A3	98	20	B	15	D2	9
5	A	8	A2	99	21	B	–	–	–
6	A	9	B3	100	22	B	–	–	–
7	A	10	A1	1	23	B	–	–	–
8	A	11	B2	5	24	B	–	–	–
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	16	D1	10	49	D	22	G3	16
34	C	17	E3	11	50	D	23	G1	17
35	C	20	F2	14	51	D	25	F1	20
36	C	21	F3	15	52	D	26	H1	21
37	C	–	–	–	53	D	–	–	–
38	C	–	–	–	54	D	–	–	–
39	C	–	–	–	55	D	–	–	–
40	C	–	–	–	56	D	–	–	–
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

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Table 9. EPM5192 I/O Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
65	E	27	H2	22	81	F	31	L1	26
66	E	28	J1	23	82	F	32	K2	27
67	E	29	K1	24	83	F	33	K3	31
68	E	30	J2	25	84	F	34	L2	32
69	E	–	–	–	85	F	35	L3	33
70	E	–	–	–	86	F	36	K4	34
71	E	–	–	–	87	F	37	L4	35
72	E	–	–	–	88	F	38	J5	36
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	46	L6	45	113	H	54	J10	56
98	G	47	L8	46	114	H	55	K11	57
99	G	48	K8	47	115	H	56	J11	58
100	G	49	L9	48	116	H	57	H10	59
101	G	50	L10	49	117	H	–	–	–
102	G	51	K9	50	118	H	–	–	–
103	G	52	L11	51	119	H	–	–	–
104	G	53	K10	55	120	H	–	–	–
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

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Table 9. EPM5192 I/O Pin-Outs (Part 3 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
129	I	58	H11	60	145	J	64	F11	66
130	I	59	F10	61	146	J	65	E11	67
131	I	62	G9	64	147	J	67	E9	70
132	I	63	F9	65	148	J	68	D11	71
133	I	–	–	–	149	J	–	–	–
134	I	–	–	–	150	J	–	–	–
135	I	–	–	–	151	J	–	–	–
136	I	–	–	–	152	J	–	–	–
137	I	–	–	–	153	J	–	–	–
138	I	–	–	–	154	J	–	–	–
139	I	–	–	–	155	J	–	–	–
140	I	–	–	–	156	J	–	–	–
141	I	–	–	–	157	J	–	–	–
142	I	–	–	–	158	J	–	–	–
143	I	–	–	–	159	J	–	–	–
144	I	–	–	–	160	J	–	–	–
161	K	69	D10	72	177	L	73	A11	76
162	K	70	C11	73	178	L	74	B10	77
163	K	71	B11	74	179	L	75	B9	81
164	K	72	C10	75	180	L	76	A10	82
165	K	–	–	–	181	L	77	A9	83
166	K	–	–	–	182	L	78	B8	84
167	K	–	–	–	183	L	79	A8	85
168	K	–	–	–	184	L	80	B6	86
169	K	–	–	–	185	L	–	–	–
170	K	–	–	–	186	L	–	–	–
171	K	–	–	–	187	L	–	–	–
172	K	–	–	–	188	L	–	–	–
173	K	–	–	–	189	L	–	–	–
174	K	–	–	–	190	L	–	–	–
175	K	–	–	–	191	L	–	–	–
176	K	–	–	–	192	L	–	–	–

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