Includes MAX 7000AE

MAX 7000A

Programmable Logic Device Family

January 1999, ver. 1.3 — Data Sheet

Features...

Preliminary Information

- Formerly known as Michelangelo devices
- High-performance CMOS EEPROM-based programmable logic devices (PLDs) built on second-generation Multiple Array MatriX (MAX®) architecture (see Table 1)
- 3.3-V in-system programmability (ISP) through the built-in Joint Test Action Group (JTAG) interface with advanced pin-locking capability
- Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- Enhanced ISP features
  - Enhanced ISP algorithm for faster programming (excluding EPM7128A and EPM7256A devices)
  - ISP_Done bit to ensure complete programming (excluding EPM7128A and EPM7256A devices)
  - Pull-up resistor on I/O pins during in-system programming
- Pin-compatible with the popular 5.0-V MAX 7000S devices
- High-density PLDs ranging from 600 to 10,000 usable gates
- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 192.3 MHz
- MultiVolt™ I/O interface enabling device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), space-saving FineLine BGA™, and plastic J-lead chip carrier (PLCC) packages

Table 1. MAX 7000A Device Features

Feature	EPM7032AE	EPM7064AE	EPM7128A	EPM7256A	EPM7384AE	EPM7512AE
Usable gates	600	1,250	2,500	5,000	7,500	10,000
Macrocells	32	64	128	256	384	512
Logic array blocks	2	4	8	16	24	32
Maximum user I/O pins	36	68	100	164	212	212
t_{PD} (ns)	4.5	4.5	6	7.5	7.5	7.5
t_{SU} (ns)	3	3	4	4.9	4.9	4.9
t_{FSU} (ns)	2.5	2.5	2.5	3	3	3
t_{CO1} (ns)	2.8	2.8	3.5	4.5	4.5	4.5
f_{CNT} (MHz)	192.3	192.3	147.1	119.0	119.0	119.0

A-DS-M7000A-1.3

...and More Features

- Supports hot-socketing
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- Peripheral component interconnect (PCI) compatible
- Bus friendly architecture including programmable slew-rate control
- Open-drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - 6 to 10 pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system on Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™- or Serial Vector Format File (**.svf**)-capable in-circuit tester

General Description

MAX 7000A (including MAX 7000AE) devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 178.6 MHz. MAX 7000A devices in the -5, -6, -7, and -10 speed grades are compatible with the characteristics of the peripheral component interconnect Special Interest Group (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1***. See Table 2.

Table 2. MAX 7000A Speed Grades Note (1)						
Device	Speed Grade					
	-4	-5	-6	-7	-10	-12
EPM7032AE	✓	✓		✓	✓	
EPM7064AE	✓	✓		✓	✓	
EPM7128A			✓	✓	✓	✓
EPM7256A				✓	✓	✓
EPM7384AE				✓	✓	✓
EPM7512AE				✓	✓	✓

Note:
(1) This information is preliminary.

The MAX 7000A architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and field-programmable gate array (FPGA) devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000A devices are also ideal for gate-array prototyping.
MAX 7000A devices are available in a wide range of packages, including PLCC, FineLine BGA, PQFP, and TQFP packages. See Table 3.

Table 3. MAX 7000A Maximum User I/O Pins Notes (1), (2)								
Device	44-Pin PLCC	44-Pin TQFP	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine βGA	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA
EPM7032AE	36	36						
EPM7064AE	36	36	68	68	68			
EPM7128A			68	84	84	100		100
EPM7256A				84		120	164	164
EPM7384AE						120	176	212
EPM7512AE						120	176	212

Notes:
(1) Contact Altera for up-to-date information on available device package options.
(2) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000A devices contain from 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V and all input pins are 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in the ***1999 Data Book***.

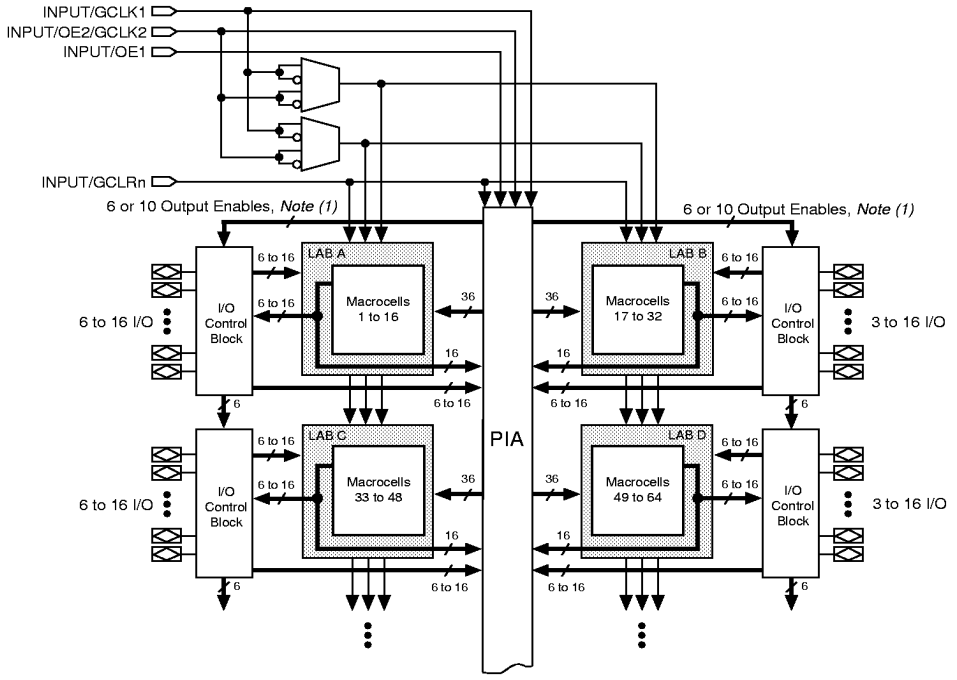
Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

Figure 1. MAX 7000A Device Block Diagram



Note:

(1) EPM7032AE, EPM7064AE, EPM7128A, and EPM7256A devices have 6 output enables. EPM7384AE and EPM7512AE devices have 10 output enables.

Logic Array βlocks

The MAX 7000A device architecture is based on the linking of high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

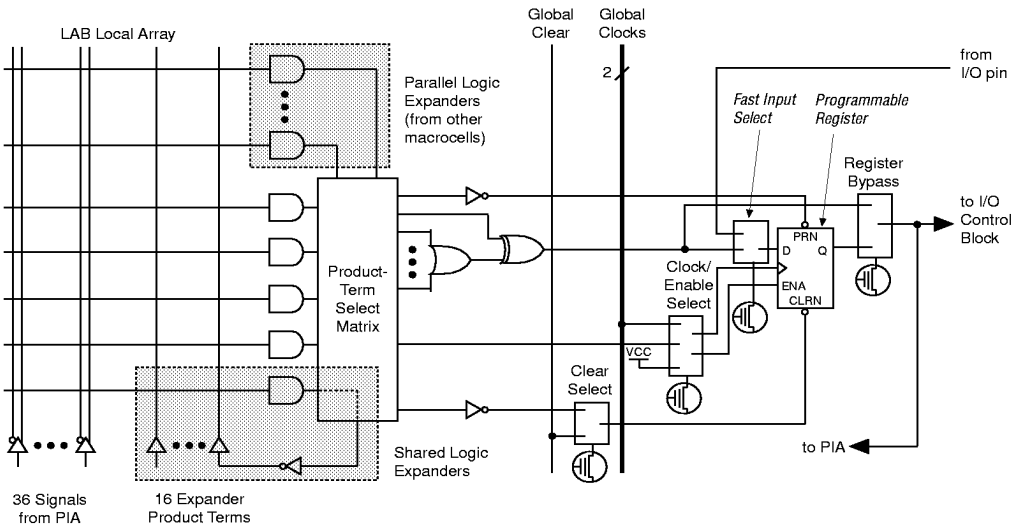
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

The MAX 7000A macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000A macrocell.

Figure 2. MAX 7000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. Clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (up to 2.5 ns) input setup time.

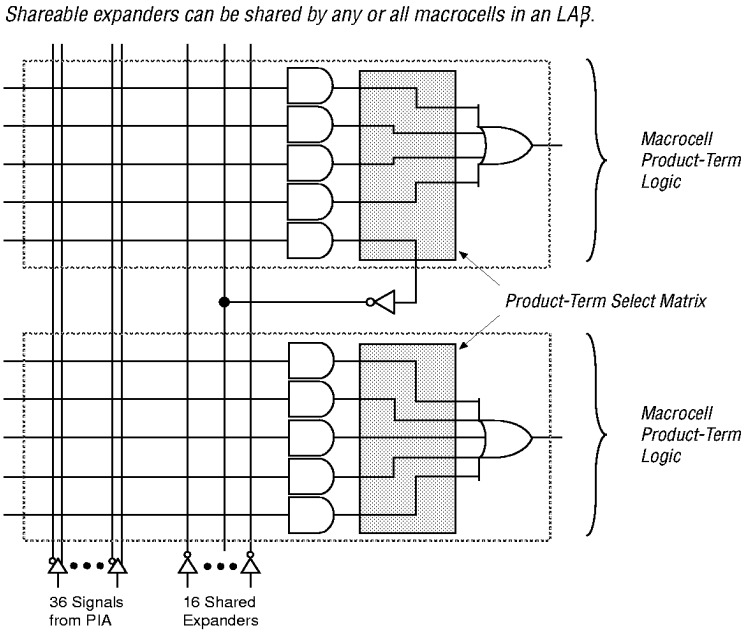
Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000A architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000A Shareable Expanders



Parallel Expanders

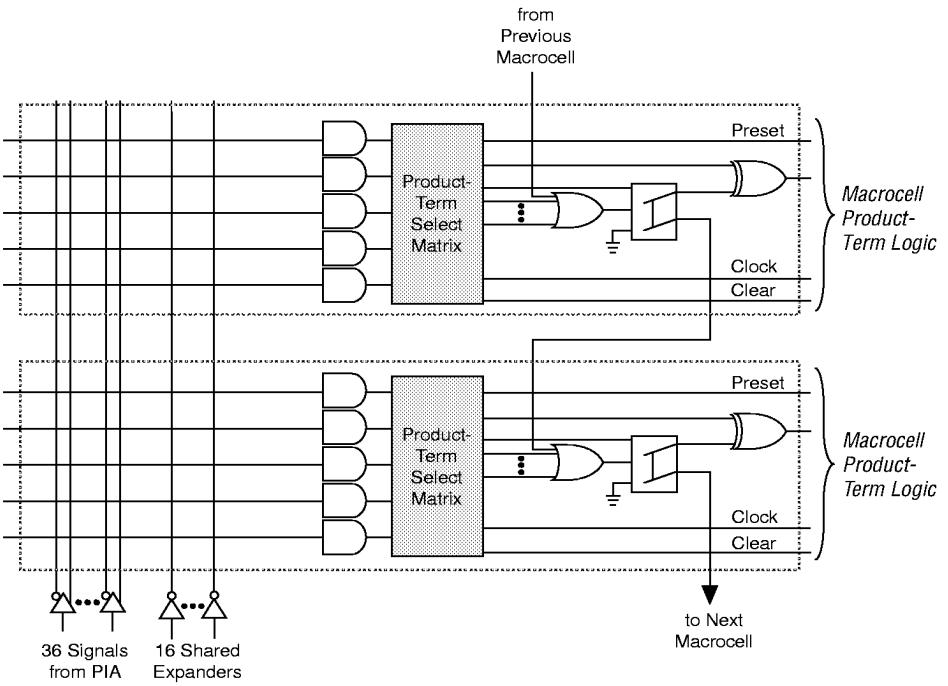
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically allocate up to 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of 5 parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000A Parallel Expanders

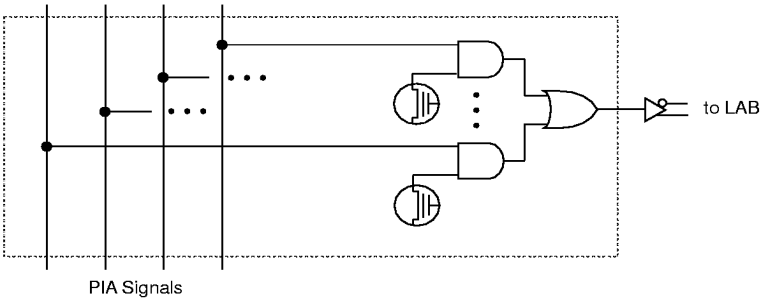
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000A PIA Routing

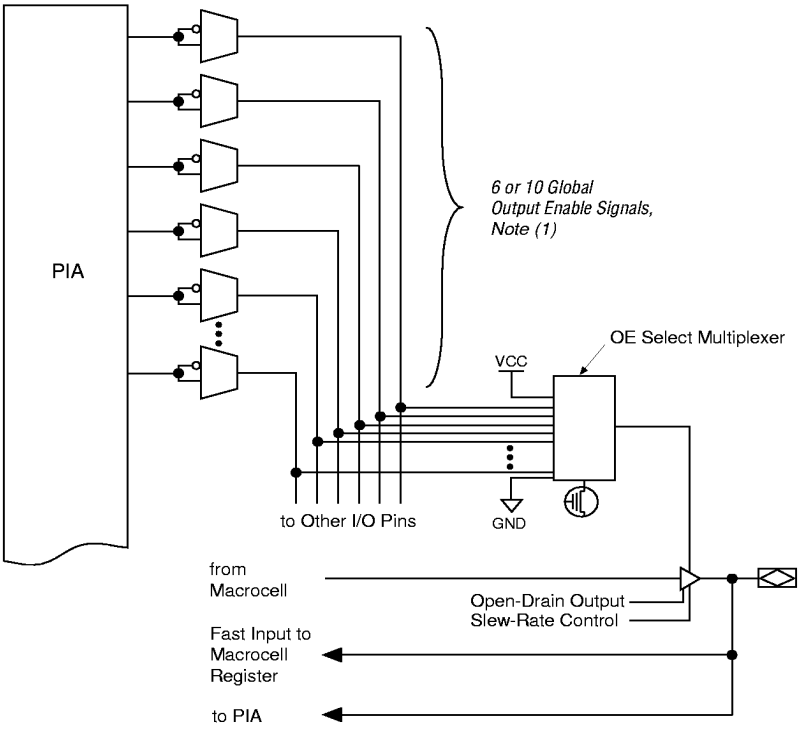


While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control βlock of MAX 7000A Devices



Note:
(1) EPM7032AE, EPM7064AE, EPM7128A, and EPM7256A devices have 6 output enable signals. EPM7384AE and EPM7512AE devices have 10 output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1-1990 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts.

MAX 7000AE devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is available in EPM7032AE, EPM7064AE, EPM7384AE, and EPM7512AE devices only.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera BitBlaster serial download cable, and the ByteBlaster and ByteBlasterMV parallel port download cables. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit tester platforms cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm contain an "F" suffix in the ordering code and are marked with an "F" in the bottom right-hand corner of the device.

Programming with External Hardware

MAX 7000A devices can be programmed on Pentium-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see the *Altera Programming Hardware Data Sheet* in the ***1999 Data Book***.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers* in the ***1999 Data Book***.

IEEE 1149.1 (JTAG) Boundary-Scan Support

MAX 7000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1-1990. Table 4 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables starting on page 32 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 4. MAX 7000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. Not available in the EPM7128A and EPM7256A devices.
UESCODE	These instructions select the user electronic signature (UESCODE) and allow the UESCODE to be serially shifted out of TDO. UESCODE instructions are available for EPM7128A and EPM7256A devices only.
ISP	These instructions are used when programming MAX 7000A devices via the JTAG ports with the BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or using a Jam File or SVF file via an embedded processor or test equipment.

Go to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 7 shows the timing information for the JTAG signals.

Figure 7. MAX 7000A JTAG Waveforms

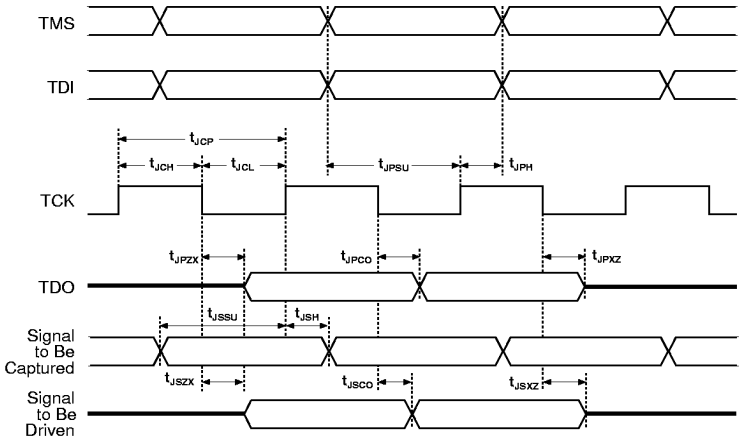


Table 5 shows the JTAG timing parameters and values for MAX 7000A devices.

Table 5. JTAG Timing Parameters & Values for MAX 7000A Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to connect to systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 6 describes the MAX 7000A MultiVolt I/O support.

Table 6. MAX 7000A MultiVolt I/O Support

V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓		✓	✓

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Design Security

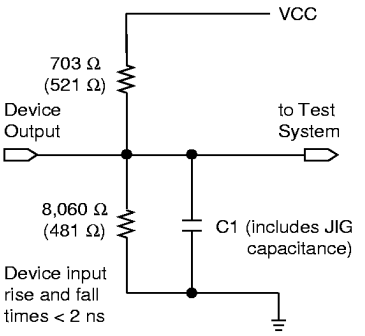
All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 8. Test patterns can be used and then erased during early stages of the production flow.

Figure 8. MAX 7000A AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 2.5-V operation.



Operating Conditions

The following tables provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

MAX 7000A Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground, *Note (2)*	–2.0	4.6	V
V_I	DC input voltage		–2.0	5.7	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	FineLine BGA, PQFP, and TQFP packages, under bias		135	° C

MAX 7000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Note (3)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation	*Note (3)*	3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation	*Note (3)*	2.3	2.7	V
V_{CCISP}	Supply voltage during ISP		3.0	3.6	V
V_I	Input voltage	*Note (4)*	0	5.3	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 7000A Device DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		1.7	5.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (6)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V, *Note (6)*	V_{CCIO} – 0.2		V
	2.5-V high-level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V, *Note (6)*	2.1		V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V, *Note (6)*	2.0		V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V, *Note (6)*	1.7		V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 4 mA DC, V_{CCIO} = 3.00 V, *Note (7)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V, *Note (7)*		0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V, *Note (7)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V, *Note (7)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V, *Note (7)*		0.7	V
I_I	Input leakage current	V_I = V_{CCINT} or ground	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CCINT} or ground	–10	10	µA
R_{ISP}	Value of I/O pin pull-up resistor when programming in-system or during power-up	V_{CCIO} = 3.0 to 3.6 V, *Note (8)*	20	50	kΩ
		V_{CCIO} = 2.3 to 2.7 V, *Note (8)*	30	80	kΩ
		V_{CCIO} = 2.3 to 3.6 V, *Note (9)*	20	74	kΩ

MAX 7000A Device Capacitance *Note (10)*

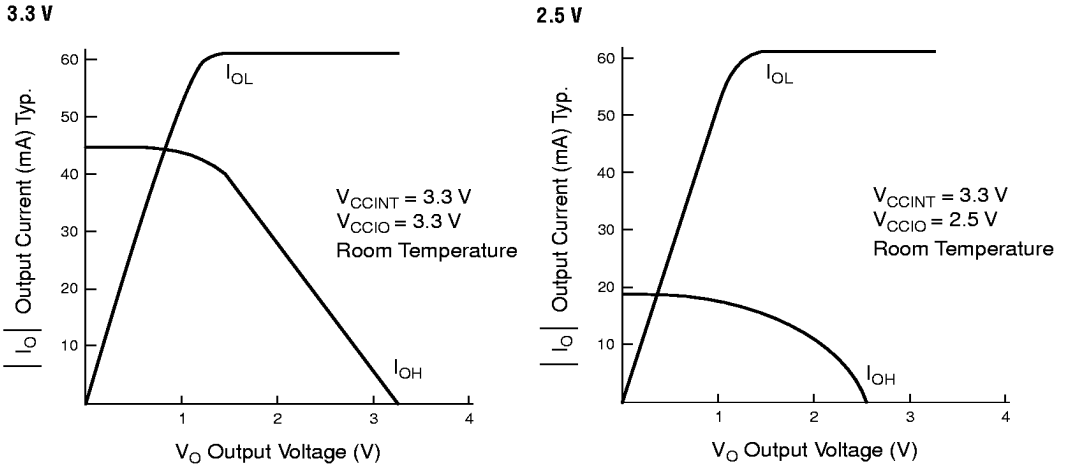
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in the ***1999 Data Book***.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(5) These values are specified under the "MAX 7000A Device Recommended Operating Conditions" on page 19.
(6) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(7) The I_{OL} parameter refers to low-level TTL or CMOS output current.
(8) For MAX 7000A devices, this pull-up exists while a device is programmed in-system.
(9) For MAX 7000AE devices, this pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
(10) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

Figure 9 shows the typical output drive characteristics of MAX 7000A devices.

Figure 9. Output Drive Characteristics of MAX 7000A Devices



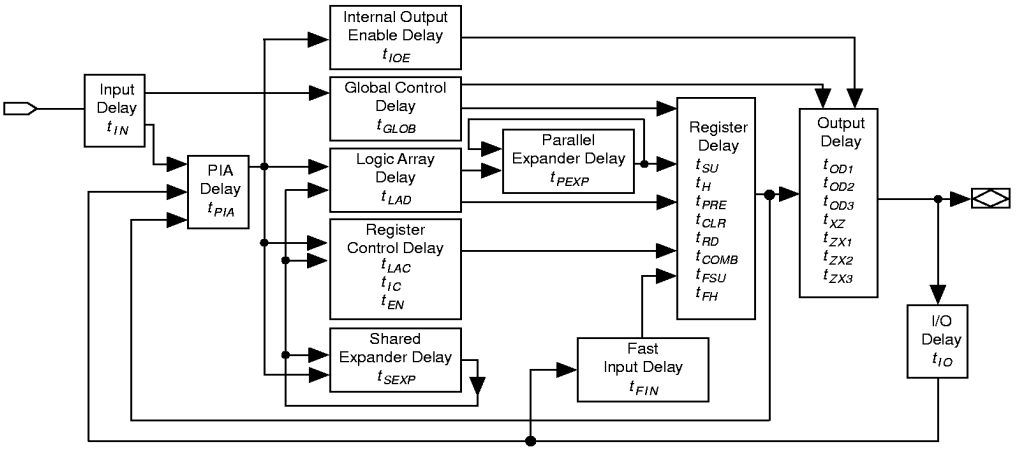
Hot-Socketing

Signals can be driven into MAX 7000AE devices before and during power up without damaging the device. Additionally, MAX 7000AE devices do not drive out during power up. Once operating conditions are reached, MAX 7000AE devices operate as specified by the user.

Timing Model

MAX 7000A device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 7000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 10. MAX 7000A Timing Model

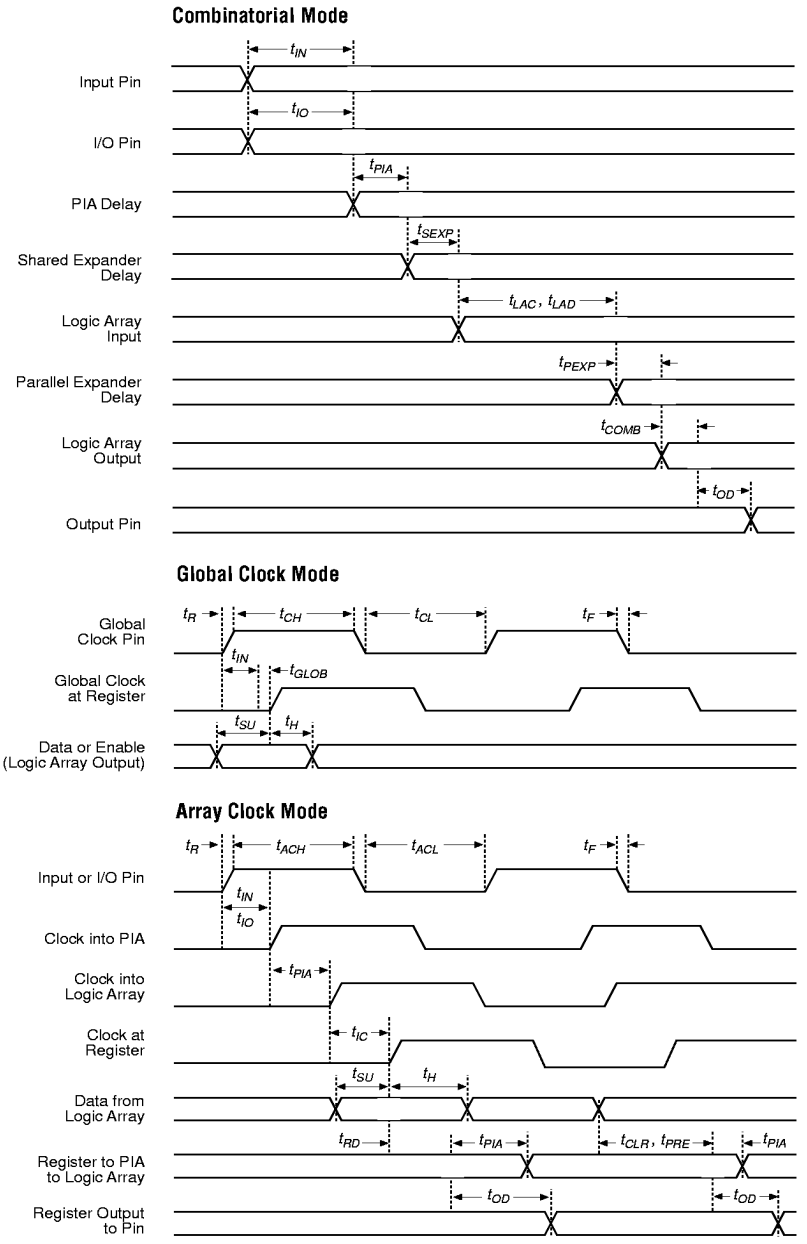


The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

Go to *Application Note 94 (Understanding MAX 7000 Timing)* in the ***1999 Data Book*** for more information.

Figure 11. MAX 7000A Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



EPM7128A AC Operating Conditions *Note (1)*

EPM7128A External Timing Parameters			Speed Grade								
			-6		-7		-10		-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF, *Note (2)*		6		7.5		10		12	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF, *Note (2)*		6		7.5		10		12	ns
t_{SU}	Global clock setup time	*Note (2)*	4.2		5.3		7		8.5		ns
t_{H}	Global clock hold time	*Note (2)*	–0.8		–0.7		–0.6		–0.4		ns
t_{FSU}	Global clock setup time of fast input		2.5		3		3		3		ns
t_{FH}	Global clock hold time of fast input		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1	3.7	1	4.6	1	6.1	1	7.3	ns
t_{CH}	Global clock high time		3		3		4		5		ns
t_{CL}	Global clock low time		3		3		4		5		ns
t_{ASU}	Array clock setup time	*Note (2)*	1.9		2.4		3.1		3.8		ns
t_{AH}	Array clock hold time	*Note (2)*	1.5		2.2		3.3		4.3		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF, *Note (2)*		6		7.5		10		12	ns
t_{ACH}	Array clock high time		3		3		4		5		ns
t_{ACL}	Array clock low time		3		3		4		5		ns
t_{CNT}	Minimum global clock period	*Note (2)*		6.9		8.6		11.5		13.8	ns
f_{CNT}	Maximum internal global clock frequency	*Notes (2), (4)*	144.9		116.3		87		72.5		MHz
t_{ACNT}	Minimum array clock period	*Note (2)*		6.9		8.6		11.5		13.8	ns
f_{ACNT}	Maximum internal array clock frequency	*Notes (2), (4)*	144.9		116.3		87		72.5		MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	166.7		166.7		125.0		100.0		MHz

EPM7128A Internal Timing Parameters			Speed Grade								
			-6		-7		-10		-12		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7		0.9		1.1	ns
t_{FIN}	Fast input delay			2.7		3.1		3.6		3.9	ns
t_{SEXP}	Shared expander delay			2.5		3.2		4.3		5.1	ns
t_{PEXP}	Parallel expander delay			0.7		0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			2.4		3		4.1		4.9	ns
t_{LAC}	Logic control array delay			2.4		3		4.1		4.9	ns
t_{IOE}	Internal output enable delay			0		0		0		0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		0.4		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (6)*		0.9		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 3.3 V or 2.5 V	C1 = 35 pF		5.4		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		4		4		5		5	ns
t_{ZX2}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		9		9		10		10	ns
t_{XZ}	Output buffer enable delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (6)*		4		4		5		5	ns
t_{SU}	Register setup time		1.9		2.4		3.1		3.8		ns
t_{H}	Register hold time		1.5		2.2		3.3		4.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.7		1.9		1.9		1.9		ns
t_{RD}	Register delay			1.7		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.7		2.1		2.8		3.3	ns
t_{IC}	Array clock delay			2.4		3		4.1		4.9	ns
t_{EN}	Register enable time			2.4		3		4.1		4.9	ns
t_{GLOB}	Global control delay			1		1.2		1.7		2	ns
t_{PRE}	Register preset time			3.1		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.1		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	*Note (2)*		0.9		1.1		1.5		1.8	ns
t_{LPA}	Low-power adder	*Note (7)*		11		10		10		10	ns

EPM7256A AC Operating Conditions *Note (1)*

EPM7256A External Timing Parameters			Speed Grade						
			-7		-10		-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF, *Note (2)*		7.5		10		12	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF, *Note (2)*		7.5		10		12	ns
t_{SU}	Global clock setup time	*Note (2)*	4.9		6.6		7.8		ns
t_{H}	Global clock hold time	*Note (2)*	0		0		0		ns
t_{FSU}	Global clock setup time of fast input		3		3		3		ns
t_{FH}	Global clock hold time of fast input		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1	4.5	1	5.9	1	7.1	ns
t_{CH}	Global clock high time		3		4		5		ns
t_{CL}	Global clock low time		3		4		5		ns
t_{ASU}	Array clock setup time	*Note (2)*	1.6		2.1		2.4		ns
t_{AH}	Array clock hold time	*Note (2)*	2.1		3.4		4.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF, *Note (2)*		7.8		10.4		12.5	ns
t_{ACH}	Array clock high time		3		4		5		ns
t_{ACL}	Array clock low time		3		4		5		ns
t_{CNT}	Minimum global clock period	*Note (2)*		8.4		11.2		13.3	ns
f_{CNT}	Maximum internal global clock frequency	*Notes (2), (4)*	119.0		89.3		75.2		MHz
t_{ACNT}	Minimum array clock period	*Note (2)*		8.4		11.2		13.3	ns
f_{ACNT}	Maximum internal array clock frequency	*Notes (2), (4)*	119.0		89.3		75.2		MHz
f_{MAX}	Maximum clock frequency	*Notes (2), (5)*	166.7		125.0		100.0		MHz

EPM7256A Internal Timing Parameters			Speed Grade						
			-7		-10		-12		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.4		0.6		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.6		0.7	ns
t_{FIN}	Fast input delay			3.3		3.7		4.1	ns
t_{SEXP}	Shared expander delay			3.6		4.9		5.9	ns
t_{PEXP}	Parallel expander delay			0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			3.7		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.4		4.6		5.6	ns
t_{IOE}	Internal output enable delay			0		0		0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (6)*		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		4		5		5	ns
t_{ZX2}	Output buffer enable delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (6)*		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9		10		10	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		5		5	ns
t_{SU}	Register setup time		1.3		1.7		2		ns
t_{H}	Register hold time		2.4		3.8		4.8		ns
t_{FSU}	Register setup time of fast input		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.9		1.9		1.9		ns
t_{RD}	Register delay			2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.5		2		2.4	ns
t_{IC}	Array clock delay			3.4		4.6		5.6	ns
t_{EN}	Register enable time			3.4		4.6		5.6	ns
t_{GLOB}	Global control delay			1.4		1.8		2.2	ns
t_{PRE}	Register preset time			3.9		5.2		6.2	ns
t_{CLR}	Register clear time			3.9		5.2		6.2	ns
t_{PIA}	PIA delay	*Note (2)*		1.3		1.7		2	ns
t_{LPA}	Low-power adder	*Note (7)*		10		10		10	ns

MAX 7000AE AC Operating Conditions *Note (1)*

MAX 7000AE External Timing Parameters			Speed Grade										
			-4		-5		-7		-10		-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF, *Note (2)*		4.5		5		7.5		10		12	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF, *Note (2)*		4.5		5		7.5		10		12	ns
t_{SU}	Global clock setup time	*Note (2)*	3		3.2		4.9		6.6		7.8		ns
t_{H}	Global clock hold time	*Note (2)*	0		0		0		0		0		ns
t_{FSU}	Global clock setup time of fast input		2.5		2.5		3		3		3		ns
t_{FH}	Global clock hold time of fast input		0		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1	2.8	1	3	1	4.5	1	5.9	1	7.1	ns
t_{CH}	Global clock high time		2		2		3		4		5		ns
t_{CL}	Global clock low time		2		2		3		4		5		ns
t_{ASU}	Array clock setup time	*Note (2)*	1.4		1		1.6		2.1		2.4		ns
t_{AH}	Array clock hold time	*Note (2)*	0.8		0.8		2.1		3.4		4.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF, *Note (2)*		4.4		5.2		7.8		10.4		12.5	ns
t_{ACH}	Array clock high time		2		2		3		4		5		ns
t_{ACL}	Array clock low time		2		2		3		4		5		ns
t_{CNT}	Minimum global clock period	*Note (2)*		5.2		5.5		8.4		11.2		13.3	ns
f_{CNT}	Maximum internal global clock frequency	*Notes (2), (4)*	192.3		181.8		119.0		89.3		75.2		MHz
t_{ACNT}	Minimum array clock period	*Note (2)*		5.2		5.5		8.4		11.2		13.3	ns
f_{ACNT}	Maximum internal array clock frequency	*Notes (2), (4)*	192.3		181.8		119.0		89.3		75.2		MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	250.0		250.0		166.7		125.0		100.0		MHz

MAX 7000AE Internal Timing Parameters			Speed Grade										
			-4		-5		-7		-10		-12		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.3		0.3		0.4		0.6		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.3		0.4		0.6		0.7	ns
t_{FIN}	Fast input delay			2.6		2.6		3.3		3.7		4.1	ns
t_{SEXP}	Shared expander delay			1.9		2.4		3.6		4.9		5.9	ns
t_{PEXP}	Parallel expander delay			0.5		0.6		0.8		1.1		1.3	ns
t_{LAD}	Logic array delay			1.9		2.5		3.7		5.0		6.0	ns
t_{LAC}	Logic control array delay			1.8		2.3		3.4		4.6		5.6	ns
t_{IOE}	Internal output enable delay			0		0		0		0		0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		0.3		0.4		0.6		0.7		0.9	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (6)*		0.8		0.9		1.1		1.2		1.4	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.3		5.4		5.6		5.7		5.9	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		4		4		4		5		5	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (1)*		4.5		4.5		4.5		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF *Note (1)*		9		9		9		10		10	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF *Note (6)*		4		4		4		5		5	ns
t_{SU}	Register setup time		1.4		0.8		1.3		1.7		2		ns
t_{H}	Register hold time		0.8		1		2.4		3.8		4.8		ns
t_{FSU}	Register setup time of fast input		0.9		0.8		1.1		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.6		1.7		1.9		1.9		1.9		ns
t_{RD}	Register delay			1.2		1.4		2.1		2.8		3.3	ns
t_{COMB}	Combinatorial delay			1.3		1		1.5		2		2.4	ns
t_{IC}	Array clock delay			1.9		2.3		3.4		4.6		5.6	ns
t_{EN}	Register enable time			1.8		2.3		3.4		4.6		5.6	ns
t_{GLOB}	Global control delay			1		0.9		1.4		1.8		2.2	ns
t_{PRE}	Register preset time			2.3		2.6		3.9		5.2		6.2	ns
t_{CLR}	Register clear time			2.3		2.6		3.9		5.2		6.2	ns
t_{PIA}	PIA delay	*Note (2)*		0.7		0.8		1.3		1.7		2	ns
t_{LPA}	Low-power adder	*Note (7)*		12.0		12.0		10.0		10.0		10.0	ns

Notes to tables:

(1) These values are specified under the "MAX 7000A Device Recommended Operating Conditions" on page 19.
(2) For certain devices (EPM7032AE-5, EPM7064AE-5, EPM7128A-6, EPM7128A-7, EPM7256A-6, EPM7384AE-7, EPM7384AE-10, EPM7384AE-12, EPM7512AE-7, EPM7512AE-10, EPM7512AE-12), these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to both global and array clocking.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 2.5 \pm 0.2$ V for commercial and industrial use.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in the ***1999 Data Book***.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON}	=	Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$	=	Highest clock frequency to the device
$\mathbf{tog_{LC}}$	=	Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C	=	Constants, shown in Table 7

Table 7. MAX 7000A I_{CC} Equation Constants

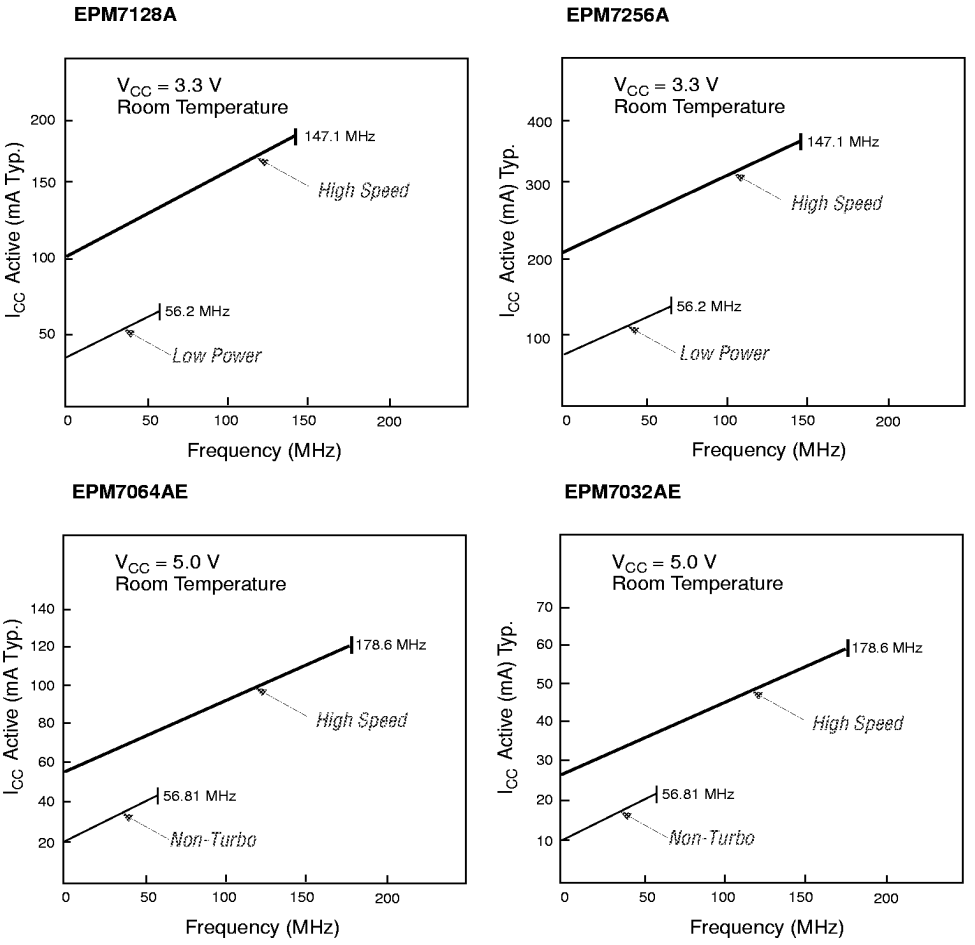
Device	A	β	C
EPM7032AE	0.82	0.31	0.054
EPM7064AE	0.82	0.31	0.054
EPM7128A, *Note (1)*	0.79	0.27	0.035
EPM7256A, *Note (1)*	0.79	0.27	0.035
EPM7384AE	*Note (2)*	*Note (2)*	*Note (2)*
EPM7512AE	*Note (2)*	*Note (2)*	*Note (2)*

Notes:
(1) Values for these devices are preliminary.
(2) Contact Altera Applications for these constants.

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 12 shows typical supply current versus frequency for MAX 7000A and 7000AE devices.

Figure 12. I_{CC} vs. Frequency for MAX 7000A Devices



Device Pin-Outs

Tables 8, 9, 10, and 11 show the pin names and numbers for the pins in each MAX 7000A device package.

Table 8. EPM7128A Dedicated Pin-Outs

Dedicated Pin	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine βGA	144-Pin TQFP	256-Pin FineLine βGA
INPUT/GCLK1	83	87	A6	125	D9
INPUT/GCLRn	1	89	B5	127	E8
INPUT/OE1	84	88	B6	126	E9
INPUT/OE2/GCLK2	2	90	A5	128	D8
TDI, *Note (1)*	14	4	A1	4	D4
TMS, *Note (1)*	23	15	F3	20	J6
TCK, *Note (1)*	62	62	F8	89	J11
TDO, *Note (1)*	71	73	A10	104	D13
GNDINT	42, 82	38, 86	D6, G5	52, 57, 124, 129	A8, C9, G9, K8, P9
GNDIO	7, 19, 32, 47, 59, 72	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8	3, 13, 17, 33, 59, 64, 85, 105, 135	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (3.3 V only)	3, 43	39, 91	D5, G6	51, 58, 123, 130	B9, C8, G8, K9, P8
VCCIO (2.5 V or 3.3 V)	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	C8, D4, E6, F5, G7, H3	24, 50, 73, 76, 95, 115, 144	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
No Connect (N.C.)	–	–	–	1, 2, 12, 19, 34, 35, 36, 43, 46, 47, 48, 49, 66, 75, 90, 103, 108, 120, 121, 122	A1, A2, A4, A5, A6, A7, A9, A10, A11, A12, A13, A14, A15, A16, B1, B2, B4, B6, B7, B8, B11, B12, B13, B14, B 15, B16, C1, C3, C4, C6, C11, C13, C15, C16, D1, D2, D3, D15, D16, E1, E2, E3, E14, E16, F1, F2, F15, F16, G1, G2, G14, G16, H1, H2, H15, H16, J1, J2, J15, J16, K1, K2, K3, K14, K15, K16, L1, L2, L15, L16, M1, M14, M16, N1, N2, N3, N14, N15, N16, P1, P2, P3, P4, P12, P13, P15, P16, R1, R4, R5, R6, R7, R8, R9, R11, R12, R13, R14, R15, R16, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T16
Total User I/O PIns	64	80	80	96	96

Note:

(1) This pin can function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or ISP, this pin is not available as a user I/O pin.

Table 9. EPM7128A I/O Pin-Outs (Part 1 of 2)

MC	LAβ	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine βGA	144-Pin TQFP	256-Pin FineLine βGA	MC	LAβ	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine βGA	144-Pin TQFP	256-Pin FineLine βGA
1	A	–	2	C1	143	F4	17	B	22	14	F4	18	J7
2	A	–	–	–	–	–	18	B	–	–	–	–	–
3	A	12	1	B1	142	E4	19	B	21	13	E2	16	H5
4	A	–	–	–	141	C5	20	B	–	–	–	15	H3
5	A	11	100	B2	140	E5	21	B	20	12	E1	14	H4
6	A	10	99	A2	139	D5	22	B	–	10	E3	11	H6
7	A	–	–	–	–	–	23	B	–	–	–	–	–
8	A	9	98	A3	138	D6	24	B	18	9	E4	10	H7
9	A	–	97	B3	137	E6	25	B	17	8	D2	9	G5
10	A	–	–	–	–	–	26	B	–	–	–	–	–
11	A	8	96	A4	136	D7	27	B	16	7	D1	8	G4
12	A	–	–	–	134	C7	28	B	–	–	–	7	F3
13	A	6	94	B4	133	E7	29	B	15	6	D3	6	G6
14	A	5	93	C4	132	F7	30	B	–	5	C2	5	F5
15	A	–	–	–	–	–	31	B	–	–	–	–	–
16	A	4	92	C5	131	F8	32	B	14 *(1)*	4 *(1)*	A1 *(1)*	4 *(1)*	D4 *(1)*
33	C	–	25	K1	32	N4	49	D	41	37	K5	56	N8
34	C	–	–	–	–	–	50	D	–	–	–	–	–
35	C	31	24	J1	31	M4	51	D	40	36	J5	55	M8
36	C	–	–	–	30	M2	52	D	–	–	–	54	P7
37	C	30	23	H1	29	L4	53	D	39	35	H5	53	L8
38	C	29	22	H2	28	L5	54	D	–	33	K4	45	N7
39	C	–	–	–	–	–	55	D	–	–	–	–	–
40	C	28	21	G2	27	K5	56	D	37	32	J4	44	M7
41	C	–	20	G1	26	K4	57	D	36	31	H4	42	L7
42	C	–	–	–	–	–	58	D	–	–	–	–	–
43	C	27	19	G3	25	K6	59	D	35	30	J3	41	M6
44	C	–	–	–	23	J3	60	D	–	–	–	40	P5
45	C	25	17	F2	22	J5	61	D	34	29	K3	39	N6
46	C	24	16	F1	21	J4	62	D	–	28	J2	38	M5
47	C	–	–	–	–	–	63	D	–	–	–	–	–
48	C	23 *(1)*	15 *(1)*	F3 *(1)*	20 *(1)*	J6 *(1)*	64	D	33	27	K2	37	N5

Table 9. EPM7128A I/O Pin-Outs (Part 2 of 2)

MC	LAβ	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine βGA	144-Pin TQFP	256-Pin FineLine βGA	MC	LAβ	84-Pin PLCC	100-Pin TQFP	100-Pin FineLine βGA	144-Pin TQFP	256-Pin FineLine βGA
65	E	44	40	K6	60	N9	81	F	–	52	J10	77	M13
66	E	–	–	–	–	–	82	F	–	–	–	–	–
67	E	45	41	J6	61	M9	83	F	54	53	H10	78	L13
68	E	–	–	–	62	R10	84	F	–	–	–	79	L14
69	E	46	42	H6	63	L9	85	F	55	54	H9	80	L12
70	E	–	44	K7	65	N10	86	F	56	55	J9	81	M12
71	E	–	–	–	–	–	87	F	–	–	–	–	–
72	E	48	45	J7	67	M10	88	F	57	56	G9	82	K12
73	E	49	46	H7	68	L10	89	F	–	57	G10	83	K13
74	E	–	–	–	–	–	90	F	–	–	–	–	–
75	E	50	47	J8	69	M11	91	F	58	58	G8	84	K11
76	E	–	–	–	70	P11	92	F	–	–	–	86	J14
77	E	51	48	K8	71	N11	93	F	60	60	F9	87	J12
78	E	–	49	K9	72	N12	94	F	61	61	F10	88	J13
79	E	–	–	–	–	–	95	F	–	–	–	–	–
80	E	52	50	K10	74	N13	96	F	62 *(1)*	62 *(1)*	F8 *(1)*	89 *(1)*	J11 *(1)*
97	G	63	63	F7	91	J10	113	H	–	75	C10	106	F13
98	G	–	–	–	–	–	114	H	–	–	–	–	–
99	G	64	64	E9	92	H12	115	H	73	76	B10	107	E13
100	G	–	–	–	93	H14	116	H	–	–	–	109	C12
101	G	65	65	E10	94	H13	117	H	74	77	B9	110	E12
102	G	–	67	E8	96	H11	118	H	75	78	A9	111	D12
103	G	–	–	–	–	–	119	H	–	–	–	–	–
104	G	67	68	E7	97	H10	120	H	76	79	A8	112	D11
105	G	68	69	D9	98	G12	121	H	–	80	B8	113	E11
106	G	–	–	–	–	–	122	H	–	–	–	–	–
107	G	69	70	D10	99	G13	123	H	77	81	A7	114	D10
108	G	–	–	–	100	F14	124	H	–	–	–	116	C10
109	G	70	71	D8	101	G11	125	H	79	83	B7	117	E10
110	G	–	72	C9	102	F12	126	H	80	84	C7	118	F10
111	G	–	–	–	–	–	127	H	–	–	–	–	–
112	G	71 *(1)*	73 *(1)*	A10 *(1)*	104 *(1)*	D13 *(1)*	128	H	81	85	C6	119	F9

Note:

(1) This pin can function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or for ISP, this pin is not available as a user I/O pin.

Table 10. EPM7256A Dedicated Pin-Outs

Dedicated Pin	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA
INPUT/GCLK1	87	125	184	D9
INPUT/GCLRn	89	127	182	E8
INPUT/OE1	88	126	183	E9
INPUT/OE2/GCLK2	90	128	181	D8
TDI, *Note (1)*	4	4	176	D4
TMS, *Note (1)*	15	20	127	J6
TCK, *Note (1)*	62	89	30	J11
TDO, *Note (1)*	73	104	189	D13
GNDINT	38, 86	52, 57, 124, 129	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO	11, 26, 43, 59, 74, 95	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 72, 94, 116, 134, 152, 174, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (3.3 V Only)	39, 91	51, 58, 123, 130	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO (3.3 V or 2.5 V)	3, 18, 34, 51, 66, 82	24, 50, 73, 76, 95, 115, 144	5, 23, 41, 63, 85, 107, 125, 143, 165, 191	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
No Connect (N.C.)	–	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208.	A1, A2, A6, A12, A13, A14, A15, A16, B1, B2, B15, B16, C1, C15, C16, D1, D3, D15, D16, G1, G16, H15, H16, J1, K1, L1, L2, M1, M16, N1, N2, N14, N15, N16, P1, P2, P15, P16, R1, R14, R15, R16, T7, T8, T10, T11, T14, T16
Total User I/O Pins	80	116	160	160

Note:
(1) This pin can function as either a JTAG pin or a user I/O pin. If the device is programmed to use the JTAG ports for BST or ISP, this pin is not available as a user I/O pin.

Table 11. EPM7256A I/O Pin-Outs (Part 1 of 4)

MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA	MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA
1	A	–	–	153	C3	17	B	–	–	141	F5
2	A	–	–	–	–	18	B	–	–	–	–
3	A	–	2	154	C4	19	B	–	10	142	F2
4	A	–	–	–	–	20	B	–	–	–	–
5	A	–	1	159	E5	21	B	–	9	144	E1
6	A	–	143	160	D5	22	B	–	–	145	F4
7	A	–	–	–	–	23	B	–	–	–	–
8	A	2	–	161	C5	24	B	8	8	146	F3
9	A	1	–	162	B4	25	B	7	7	147	E2
10	A	–	–	–	–	26	B	–	–	–	–
11	A	100	142	163	A4	27	B	6	6	148	D2
12	A	–	–	–	–	28	B	–	–	–	–
13	A	–	141	164	A5	29	B	5	5	149	E3
14	A	99	140	166	D6	30	B	–	–	150	E4
15	A	–	–	–	–	31	B	–	–	–	–
16	A	98	139	167	C6	32	B	4 *(1)*	4 *(1)*	151	D4 *(1)*
33	C	–	36	108	N4	49	D	31	44	92	N6
34	C	–	–	–	–	50	D	–	–	–	–
35	C	–	35	109	P3	51	D	30	43	93	T5
36	C	–	–	–	–	52	D	–	–	–	–
37	C	–	34	110	N3	53	D	29	42	95	M6
38	C	–	–	111	M4	54	D	28	41	96	R5
39	C	–	–	–	–	55	D	–	–	–	–
40	C	25	32	112	M2	56	D	–	40	97	M5
41	C	24	31	113	L4	57	D	–	–	98	P5
42	C	–	–	–	–	58	D	–	–	–	–
43	C	23	30	114	L5	59	D	–	39	99	N5
44	C	–	–	–	–	60	D	–	–	–	–
45	C	22	29	115	K6	61	D	–	38	100	T4
46	C	–	–	117	K5	62	D	–	–	101	R4
47	C	–	–	–	–	63	D	–	–	–	–
48	C	21	28	118	K4	64	D	27	37	102	P4
65	E	–	–	168	B6	81	F	–	–	130	H5
66	E	–	–	–	–	82	F	–	–	–	–
67	E	–	–	169	E6	83	F	–	19	131	H1

Table 11. EPM7256A I/O Pin-Outs (Part 2 of 4)

MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA	MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA
68	E	–	–	–	–	84	F	–	–	–	–
69	E	–	138	170	F7	85	F	–	18	132	H2
70	E	–	–	171	E7	86	F	–	–	133	H3
71	E	–	–	–	–	87	F	–	–	–	–
72	E	97	137	172	D7	88	F	14	16	135	H4
73	E	96	136	173	C7	89	F	13	15	136	G6
74	E	–	–	–	–	90	F	–	–	–	–
75	E	94	134	175	B7	91	F	12	14	137	G5
76	E	–	–	–	–	92	F	–	–	–	–
77	E	93	133	176 *(1)*	A7	93	F	10	12	138	G2
78	E	–	132	177	F8	94	F	–	–	139	G4
79	E	–	–	–	–	95	F	–	–	–	–
80	E	92	131	178	B8	96	F	9	11	140	F1
97	G	–	–	119	K3	113	H	37	–	79	M8
98	G	–	–	–	–	114	H	–	–	–	–
99	G	–	27	120	K2	115	H	36	54	80	N8
100	G	–	–	–	–	116	H	–	–	–	–
101	G	–	26	121	J7	117	H	–	53	81	L8
102	G	–	–	122	H7	118	H	35	–	84	R7
103	G	–	–	–	–	119	H	–	–	–	–
104	G	20	25	123	J5	120	H	–	49	86	P7
105	G	19	23	124	J2	121	H	–	48	87	N7
106	G	–	–	–	–	122	H	–	–	–	–
107	G	17	22	126	J3	123	H	–	47	88	M7
108	G	–	–	–	–	124	H	–	–	–	–
109	G	16	21	127 *(1)*	J4	125	H	33	46	89	L7
110	G	–	–	128	H6	126	H	–	–	90	T6
111	G	–	–	–	–	127	H	–	–	–	–
112	G	15 *(1)*	20 *(1)*	129	J6 *(1)*	128	H	32	45	91	R6
129	I	80	114	197	C11	145	J	63	–	27	J15
130	I	–	–	–	–	146	J	–	–	–	–
131	I	81	116	196	B11	147	J	64	90	26	J16
132	I	–	–	–	–	148	J	–	–	–	–
133	I	–	117	195	A11	149	J	65	91	25	J10
134	I	–	–	194	F10	150	J	–	–	24	H14

Table 11. EPM7256A I/O Pin-Outs (Part 3 of 4)

MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA	MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA
135	I	–	–	–	–	151	J	–	–	–	–
136	I	–	118	193	E10	152	J	–	92	22	H13
137	I	–	119	192	A10	153	J	–	93	21	H12
138	I	–	–	–	–	154	J	–	–	–	–
139	I	83	120	190	C10	155	J	67	94	20	H11
140	I	–	–	–	–	156	J	–	–	–	–
141	I	84	121	189 *(1)*	D10	157	J	–	96	19	H10
142	I	–	–	188	F9	158	J	–	–	18	G11
143	I	–	–	–	–	159	J	–	–	–	–
144	I	85	122	187	A9	160	J	68	97	17	G14
161	K	–	–	38	K11	177	L	–	–	78	R8
162	K	–	–	–	–	178	L	–	–	–	–
163	K	57	82	37	K12	179	L	–	55	77	T9
164	K	–	–	–	–	180	L	–	–	–	–
165	K	–	83	36	K14	181	L	–	56	76	R9
166	K	–	–	35	K13	182	L	–	–	73	N9
167	K	–	–	–	–	183	L	–	–	–	–
168	K	58	84	34	K15	184	L	40	60	71	M9
169	K	–	86	33	K16	185	L	41	61	70	L9
170	K	–	–	–	–	186	L	–	–	–	–
171	K	60	87	31	J13	187	L	42	62	69	R10
172	K	–	–	–	–	188	L	–	–	–	–
173	K	61	88	30 *(1)*	J14	189	L	44	63	68	N10
174	K	–	–	29	J12	190	L	–	–	67	M10
175	K	–	–	–	–	191	L	–	–	–	–
176	K	62 *(1)*	89 *(1)*	28	J11 *(1)*	192	L	45	65	66	L10

Table 11. EPM7256A I/O Pin-Outs (Part 4 of 4)

MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA	MC	LAβ	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine βGA
193	M	–	106	4	B14	209	N	–	–	16	G13
194	M	–	–	–	–	210	N	–	–	–	–
195	M	75	107	3	C13	211	N	69	98	15	G12
196	M	–	–	–	–	212	N	–	–	–	–
197	M	–	108	206	B13	213	N	–	99	13	F16
198	M	–	–	205	F12	214	N	–	–	12	F15
199	M	–	–	–	–	215	N	–	–	–	–
200	M	–	109	204	E12	216	N	70	100	11	F13
201	M	76	110	203	D12	217	N	–	101	10	F14
202	M	–	–	–	–	218	N	–	–	–	–
203	M	77	111	202	C12	219	N	71	102	9	E16
204	M	–	–	–	–	220	N	–	–	–	–
205	M	–	–	201	B12	221	N	72	103	8	E14
206	M	78	112	199	E11	222	N	–	–	7	E13
207	M	–	–	–	–	223	N	–	–	–	–
208	M	79	113	198	D11	224	N	73 *(1)*	104 *(1)*	6	D13 *(1)*
225	O	–	–	49	R13	241	P	46	66	65	R11
226	O	–	–	–	–	242	P	–	–	–	–
227	O	–	74	48	P13	243	P	47	67	64	P11
228	O	–	–	–	–	244	P	–	–	–	–
229	O	–	75	47	N13	245	P	48	68	62	N11
230	O	–	–	46	M14	246	P	49	69	61	M11
231	O	–	–	–	–	247	P	–	–	–	–
232	O	52	77	45	M13	248	P	–	–	60	T12
233	O	53	78	44	L13	249	P	–	70	59	R12
234	O	–	–	–	–	250	P	–	–	–	–
235	O	54	79	43	L14	251	P	–	–	58	M12
236	O	–	–	–	–	252	P	–	–	–	–
237	O	55	80	42	L12	253	P	–	71	57	P12
238	O	–	–	40	L15	254	P	–	–	56	N12
239	O	–	–	–	–	255	P	–	–	–	–
240	O	56	81	39	L16	256	P	50	72	55	T13

Note:

(1) This pin can function as either a JTAG pin or a user I/O pin. If the device is programmed to use the JTAG ports for BST or ISP, this pin is not available as a user I/O pin.

Tables 12 through 20 show the pin names and numbers for the pins in each MAX 7000AE device package.

Table 12. EPM7032AE Dedicated Pin-Outs

Dedicated Pin	44-Pin J-Lead	44-Pin TQFP
INPUT/GCLK1	43	37
INPUT/GCLRn	1	39
INPUT/OE1	44	38
INPUT/OE2/GCLK2	2	40
TDI, *Note (1)*	7	1
TMS, *Note (1)*	13	7
TCK, *Note (1)*	32	26
TDO, *Note (1)*	38	32
GND	10, 22, 30, 42	4, 16, 24, 36
VCC	3, 15, 23, 35	9, 17, 29, 41
No Connect (N.C.)	–	–
Total User I/O Pins	36	36

Table 13. EPM7032AE I/O Pin-Outs

MC	LAβ	44-Pin J-Lead	44-Pin TQFP	MC	LAβ	44-Pin J-Lead	44-Pin TQFP
1	A	4	42	17	B	41	35
2	A	5	43	18	B	40	34
3	A	6	44	19	B	39	33
4	A	7 *(1)*	1 *(1)*	20	B	38 *(1)*	32 *(1)*
5	A	8	2	21	B	37	31
6	A	9	3	22	B	36	30
7	A	11	5	23	B	34	28
8	A	12	6	24	B	33	27
9	A	13 *(1)*	7 *(1)*	25	B	32 *(1)*	26 *(1)*
10	A	14	8	26	B	31	25
11	A	16	10	27	B	29	23
12	A	17	11	28	B	28	22
13	A	18	12	29	B	27	21
14	A	19	13	30	B	26	20
15	A	20	14	31	B	25	19
16	A	21	15	32	B	24	18

Table 14. EPM7064AE Dedicated Pin-Outs

Dedicated Pin	44-Pin J-Lead	44-Pin TQFP	84-Pin J-Lead	100-Pin TQFP	100-Pin FineLine BGA
INPUT/GCLK1	43	37	83	87	A6
INPUT/GCLRn	1	39	1	89	B5
INPUT/OE1	44	38	84	88	B6
INPUT/OE2/GCLK2	2	40	2	90	A5
TDI, *Note (1)*	7	1	14	4	A1
TMS, *Note (1)*	13	7	23	15	F3
TCK, *Note (1)*	32	26	62	62	F8
TDO, *Note (1)*	38	32	71	73	A10
GND	10, 22, 30, 42	4, 16, 24, 36	7, 19, 32, 42, 47, 59, 72, 82	11, 26, 38, 43, 59, 74, 86, 95	C3, D6, D7, E5, F6, G4, G5, H8
VCCINT (3.3 V Only)	3, 15, 23, 35	9, 17, 29, 41	3, 43	39, 91	D5, G6
VCCIO (2.5 V or 3.3 V)	–	–	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	C8, D4, E6, F5, G7, H3
No Connect (N.C.)	–	–	–	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78	B1, B10, C1, C9, C10, D8, E3, E4, H1, H9, H10, J1, J2, J10, K1, K9
Total User I/O Pins	36	36	68	68	68

Table 15. EPM7064AE I/O Pin-Outs (44-Pin J-Lead & 44-Pin TQFP Packages)

MC	LAβ	44-Pin J-Lead	44-Pin TQFP	MC	LAβ	44-Pin J-Lead	44-Pin TQFP
1	A	12	6	17	B	21	15
2	A	–	–	18	B	–	–
3	A	11	5	19	B	20	14
4	A	9	3	20	B	19	13
5	A	8	2	21	B	18	12
6	A	–	–	22	B	–	–
7	A	–	–	23	B	–	–
8	A	7 *(1)*	1 *(1)*	24	B	17	11
9	A	–	–	25	B	16	10
10	A	–	–	26	B	–	–
11	A	6	44	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	5	43	30	B	14	8
15	A	–	–	31	B	–	–
16	A	4	42	32	B	13 *(1)*	7 *(1)*
33	C	24	18	49	D	33	27
34	C	–	–	50	D	–	–
35	C	25	19	51	D	34	28
36	C	26	20	52	D	36	30
37	C	27	21	53	D	37	31
38	C	–	–	54	D	–	–
39	C	–	–	55	D	–	–
40	C	28	22	56	D	38 *(1)*	32 *(1)*
41	C	29	23	57	D	39	33
42	C	–	–	48	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	31	25	62	D	40	34
47	C	–	–	63	D	–	–
48	C	32 *(1)*	26 *(1)*	64	D	41	35

Table 16. EPM7064AE I/O Pin-Outs (84-Pin J-Lead, 100-Pin TQFP & 100-Pin FineLine βGA Packages)

MC	LAβ	84-Pin J-Lead	100-Pin TQFP	100-Pin FineLine βGA	MC	LAβ	84-Pin J-Lead	100-Pin TQFP	100-Pin FineLine βGA
1	A	22	14	F4	17	B	41	37	K5
2	A	21	13	E2	18	B	40	36	J5
3	A	20	12	E1	19	B	39	35	H5
4	A	18	10	D2	20	B	37	33	K4
5	A	17	9	D1	21	B	36	32	J4
6	A	16	8	D3	22	B	35	31	H4
7	A	15	6	C2	23	B	34	30	J3
8	A	14 *(1)*	4 *(1)*	A1 *(1)*	24	B	33	29	K3
9	A	12	100	B2	25	B	31	25	K2
10	A	11	99	A2	26	B	30	23	H2
11	A	10	98	A3	27	B	29	21	G2
12	A	9	97	B3	28	B	28	20	G1
13	A	8	96	A4	29	B	27	19	G3
14	A	6	94	B4	30	B	25	17	F2
15	A	5	93	C4	31	B	24	16	F1
16	A	4	92	C5	32	B	23 *(1)*	15 *(1)*	F3 *(1)*
33	C	44	40	K6	49	D	63	63	F7
34	C	45	41	J6	50	D	64	64	E9
35	C	46	42	H6	51	D	65	65	E10
36	C	48	44	K7	52	D	67	67	E8
37	C	49	45	J7	53	D	68	68	E7
38	C	50	46	H7	54	D	69	69	D9
39	C	51	47	J8	55	D	70	71	D10
40	C	52	48	K8	56	D	71 *(1)*	73 *(1)*	A10 *(1)*
41	C	54	52	K10	57	D	73	75	B9
42	C	55	54	J9	48	D	74	76	A9
43	C	56	56	G9	59	D	75	79	A8
44	C	57	57	G10	60	D	76	80	B8
45	C	58	58	G8	61	D	77	81	A7
46	C	60	60	F9	62	D	79	83	B7
47	C	61	61	F10	63	D	80	84	C7
48	C	62 *(1)*	62 *(1)*	F8 *(1)*	64	D	81	85	C6

Note to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 17. EPM7384AE Dedicated Pin-Outs

Dedicated Pin	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
INPUT/GCLK1	125	184	D9
INPUT/GCLRn	127	182	E8
INPUT/OE1	126	183	E9
INPUT/OE2/GCLK2	128	181	D8
TDI, *Note (2)*	4	176	D4
TMS, *Note (2)*	20	127	J6
TCK, *Note (2)*	89	30	J11
TDO, *Note (2)*	104	189	D13
GNDINT	52, 57, 124, 129	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 51, 72, 94, 116, 134, 152, 158, 174, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT	51, 58, 123, 130	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO	24, 50, 73, 76, 95, 115, 144	5, 23, 41, 63, 85, 105, 107, 125, 143, 165, 191, 207	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
No Connect (N.C.)	–	–	–
Total User I/O Pins	120	176	212

Table 18. EPM7384AE I/O Pin-Outs (Part 1 of 6)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
1	A	–	–	F7	17	B	140	166	A5
2	A	–	–	–	18	B	–	–	–
3	A	–	–	E7	19	B	–	167	D5
4	A	–	–	–	20	B	–	–	–
5	A	134	173	D7	21	B	139	168	E5
6	A	–	–	–	22	B	–	–	–
7	A	–	–	C7	23	B	–	–	E6
8	A	–	–	–	24	B	–	–	–
9	A	–	175	B7	25	B	–	169	D6
10	A	–	–	–	26	B	–	–	–
11	A	133	176 *(2)*	A7	27	B	138	170	C6
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	132	177	F8	30	B	137	171	B6
15	A	–	–	–	31	B	–	–	–
16	A	131	178	B8	32	B	136	172	A6
33	C	2	–	B2	49	D	8	–	E2
34	C	–	–	–	50	D	–	–	–
35	C	1	–	A2	51	D	–	–	E3
36	C	–	–	–	52	D	–	–	–
37	C	–	159	B4	53	D	7	153	C1
38	C	–	–	–	54	D	–	–	–
39	C	–	160	A4	55	D	–	–	B1
40	C	–	–	–	56	D	–	–	–
41	C	–	161	C4	57	D	–	154	A1
42	C	–	–	–	58	D	–	–	–
43	C	143	162	C3	59	D	6	155	D2
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	142	163	E4	62	D	5	156	D3
47	C	–	–	–	63	D	–	–	–
48	C	141	164	C5	64	D	4 *(2)*	157	D4 *(2)*

Table 18. EPM7384AE I/O Pin-Outs (Part 2 of 6)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
65	E	–	144	G2	81	F	19	135	J1
66	E	–	–	–	82	F	–	–	–
67	E	–	145	G1	83	F	–	136	H7
68	E	–	–	–	84	F	–	–	–
69	E	12	146	G6	85	F	18	137	H5
70	E	–	–	F5	86	F	–	–	H2
71	E	–	147	F2	87	F	–	138	H3
72	E	–	–	–	88	F	–	–	–
73	E	–	148	F3	89	F	–	139	H1
74	E	–	–	–	90	F	–	–	–
75	E	11	149	F1	91	F	16	140	H4
76	E	–	–	–	92	F	–	–	H6
77	E	–	–	F4	93	F	–	–	–
78	E	10	150	E1	94	F	15	141	G5
79	E	–	–	–	95	F	–	–	–
80	E	9	151	D1	96	F	14	142	G4
97	G	–	126	K4	113	H	–	117	M2
98	G	–	–	–	114	H	–	–	–
99	G	–	127 *(2)*	K3	115	H	–	118	M1
100	G	–	–	–	116	H	–	–	–
101	G	23	128	K2	117	H	28	119	M4
102	G	22	–	K1	118	H	–	–	M5
103	G	21	129	J7	119	H	–	120	L5
104	G	–	–	–	120	H	–	–	–
105	G	20 *(2)*	130	J6 *(2)*	121	H	27	121	L4
106	G	–	–	–	122	H	–	–	–
107	G	–	131	J5	123	H	–	122	L2
108	G	–	–	J4	124	H	–	–	L1
109	G	–	–	–	125	H	–	–	–
110	G	–	132	J3	126	H	26	123	K6
111	G	–	–	–	127	H	–	–	–
112	G	–	133	J2	128	H	25	124	K5

Table 18. EPM7384AE I/O Pin-Outs (Part 3 of 6)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
129	I	35	108	P3	145	J	39	98	M6
130	I	–	–	–	146	J	–	–	–
131	I	34	109	R1	147	J	–	99	R5
132	I	–	–	–	148	J	–	–	–
133	I	32	110	P2	149	J	38	100	T5
134	I	–	–	–	150	J	–	–	–
135	I	–	111	N3	151	J	–	101	P5
136	I	–	–	–	152	J	–	–	–
137	I	–	112	N2	153	J	–	102	N5
138	I	–	–	–	154	J	–	–	–
139	I	31	113	P1	155	J	37	103	T4
140	I	–	–	–	156	J	–	–	–
141	I	–	–	–	157	J	–	–	–
142	I	30	114	N1	158	J	–	104	R4
143	I	–	–	–	159	J	–	–	–
144	I	29	115	N4	160	J	36	106	P4
161	K	45	90	T7	177	L	54	79	M9
162	K	–	–	–	178	L	–	–	–
163	K	–	91	L8	179	L	–	80	L9
164	K	–	–	–	180	L	–	–	–
165	K	44	92	N7	181	L	53	81	R8
166	K	–	–	–	182	L	–	–	–
167	K	–	–	M7	183	L	–	84	T8
168	K	–	–	–	184	L	–	–	–
169	K	43	93	L7	185	L	49	86	N8
170	K	–	–	–	186	L	–	–	–
171	K	42	95	R6	187	L	48	87	M8
172	K	–	–	–	188	L	–	–	–
173	K	–	–	–	189	L	–	–	–
174	K	41	96	T6	190	L	47	88	R7
175	K	–	–	–	191	L	–	–	–
176	K	40	97	N6	192	L	46	89	P7

Table 18. EPM7384AE I/O Pin-Outs (Part 4 of 6)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
193	M	55	78	N9	209	N	–	67	M11
194	M	–	–	–	210	N	–	–	–
195	M	–	77	T9	211	N	–	66	N11
196	M	–	–	–	212	N	–	–	–
197	M	56	76	R9	213	N	65	65	P11
198	M	–	–	–	214	N	–	–	–
199	M	–	73	L10	215	N	–	–	R11
200	M	–	–	–	216	N	–	–	–
201	M	60	71	M10	217	N	–	64	T11
202	M	–	–	–	218	N	–	–	–
203	M	61	70	N10	219	N	66	62	K11
204	M	–	–	–	220	N	–	–	–
205	M	–	–	–	221	N	–	–	–
206	M	62	69	R10	222	N	67	61	M12
207	M	–	–	–	223	N	–	–	–
208	M	63	68	T10	224	N	68	60	N12
225	O	69	59	T12	241	P	74	49	R15
226	O	–	–	–	242	P	–	–	–
227	O	–	58	R12	243	P	75	48	P15
228	O	–	–	–	244	P	–	–	–
229	O	70	57	T13	245	P	–	47	N15
230	O	–	–	–	246	P	–	–	–
231	O	–	56	P12	247	P	–	46	T16
232	O	–	–	–	248	P	–	–	–
233	O	–	55	T14	249	P	–	45	R16
234	O	–	–	–	250	P	–	–	–
235	O	71	54	P13	251	P	77	44	P16
236	O	–	–	–	252	P	–	–	–
237	O	–	–	–	253	P	–	–	–
238	O	72	53	R13	254	P	78	43	N14
239	O	–	–	–	255	P	–	–	–
240	O	–	52	R14	256	P	79	42	N16

Table 18. EPM7384AE I/O Pin-Outs (Part 5 of 6)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
257	Q	80	40	M14	273	R	86	31	K14
258	Q	–	–	–	274	R	–	–	–
259	Q	–	39	N13	275	R	87	30 *(2)*	K15
260	Q	–	–	–	276	R	–	–	–
261	Q	81	38	M16	277	R	88	29	K16
262	Q	–	–	M13	278	R	89 *(2)*	–	J11 *(2)*
263	Q	–	37	L14	279	R	–	28	J12
264	Q	–	–	–	280	R	–	–	–
265	Q	–	36	L15	281	R	–	27	J13
266	Q	–	–	–	282	R	–	–	–
267	Q	82	35	L16	283	R	–	26	J14
268	Q	–	–	L13	284	R	–	–	J15
269	Q	–	–	–	285	R	–	–	–
270	Q	83	34	L12	286	R	–	25	K13
271	Q	–	–	–	287	R	–	–	–
272	Q	84	33	K12	288	R	90	24	J16
289	S	91	22	H10	305	T	96	13	G16
290	S	–	–	–	306	T	–	–	–
291	S	–	21	H11	307	T	–	12	G11
292	S	–	–	–	308	T	–	–	–
293	S	92	20	H12	309	T	97	11	F12
294	S	–	–	H15	310	T	–	–	F13
295	S	–	19	H16	311	T	–	10	F14
296	S	–	–	–	312	T	–	–	–
297	S	–	18	H14	313	T	–	9	F15
298	S	–	–	–	314	T	–	–	–
299	S	93	17	H13	315	T	98	8	F16
300	S	–	–	G12	316	T	–	–	E12
301	S	–	–	–	317	T	–	–	–
302	S	–	16	G13	318	T	99	7	E13
303	S	–	–	–	319	T	–	–	–
304	S	94	15	G14	320	T	100	6	E14

Table 18. EPM7384AE I/O Pin-Outs (Part 6 of 6)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
321	U	101	–	E16	337	V	–	–	B15
322	U	–	–	–	338	V	–	–	–
323	U	–	–	D16	339	V	107	–	A15
324	U	–	–	–	340	V	–	–	–
325	U	102	4	C16	341	V	108	206	B14
326	U	–	–	–	342	V	–	–	–
327	U	–	–	B16	343	V	–	205	A14
328	U	–	–	–	344	V	–	–	–
329	U	–	3	A16	345	V	–	204	B13
330	U	–	–	–	346	V	–	–	–
331	U	103	2	D15	347	V	109	203	A13
332	U	–	–	–	348	V	–	–	–
333	U	–	–	–	349	V	–	–	–
334	U	104 *(2)*	1	D13 *(2)*	350	V	–	202	C13
335	U	–	–	–	351	V	–	–	–
336	U	106	208	C15	352	V	110	201	D12
353	W	111	199	C12	369	X	117	–	F10
354	W	–	–	–	370	X	–	–	–
355	W	–	198	B12	371	X	–	–	E10
356	W	–	–	–	372	X	–	–	–
357	W	112	197	A12	373	X	118	192	D10
358	W	–	–	–	374	X	–	–	–
359	W	–	–	E11	375	X	–	–	C10
360	W	–	–	–	376	X	–	–	–
361	W	–	196	D11	377	X	119	190	A10
362	W	–	–	–	378	X	–	–	–
363	W	113	195	C11	379	X	120	189 *(2)*	J10
364	W	–	–	–	380	X	–	–	–
365	W	–	–	–	381	X	–	–	–
366	W	114	194	A11	382	X	121	188	F9
367	W	–	–	–	383	X	–	–	–
368	W	116	193	B11	384	X	122	187	A9

Notes to table:

(1) The EPM7384AE device in the 208-pin PQFP package supports vertical migration from the EPM7256E, EPM7256S, and EPM7256A devices. The EPM7384AE device contains additional I/O pins which are no connects on the EPM7256E, EPM7256S, and EPM7256A devices. To support these additional I/O pins, the EPM7384AE device has two additional VCCIO (pins 105 and 207) and GNDIO (pins 51 and 158) pins that are no-connect pins on the EPM7256E, EPM7256S, and EPM7256A devices. To achieve vertical migration between the EPM7256A and EPM7384AE devices, the no-connect pins 105 and 207 may be tied to VCC and pins 51 and 58 may be tied to GND on the EPM7256A devices. On the EPM7256E and EPM7256S devices, these no-connect pins must not be tied to V_{CC} and ground. The EPM7384AE and EPM7512AE devices have identical pin-outs.

(2) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Table 19. EPM7512AE Dedicated Pin-Outs

Dedicated Pin	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
INPUT/GCLK1	125	184	D9
INPUT/GCLRn	127	182	E8
INPUT/OE1	126	183	E9
INPUT/OE2/GCLK2	128	181	D8
TDI, *(2)*	4	176	D4
TMS, *(2)*	20	127	J6
TCK, *(2)*	89	30	J11
TDO, *(2)*	104	189	D13
GNDINT	52, 57, 124, 129	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 51, 72, 94, 116, 134, 152, 158, 174, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT	51, 58, 123, 130	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO	24, 50, 73, 76, 95, 115, 144	5, 23, 41, 63, 85, 105, 107, 125, 143, 165, 191, 207	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10,L3, L6, M15, P14, T2, T3
No Connect (N.C.)	–	–	–
Total User I/O Pins	120	176	212

Table 20. EPM7512AE I/O Pin-Outs (Part 1 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
1	A	134	173	D7	17	B	–	169	D6
2	A	–	–	–	18	B	–	–	–
3	A	–	–	–	19	B	–	–	–
4	A	–	–	–	20	B	–	–	–
5	A	–	–	C7	21	B	138	170	C6
6	A	–	–	–	22	B	–	–	–
7	A	–	–	–	23	B	–	–	–
8	A	–	–	–	24	B	–	–	–
9	A	–	175	B7	25	B	137	171	B6
10	A	–	–	–	26	B	–	–	–
11	A	133	176 *(2)*	A7	27	B	136	172	A6
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	132	177	F8	30	B	–	–	F7
15	A	–	–	–	31	B	–	–	–
16	A	131	178	B8	32	B	–	–	E7
33	C	142	163	E4	49	D	2	–	B2
34	C	–	–	–	50	D	–	–	–
35	C	–	–	–	51	D	–	–	–
36	C	–	–	–	52	D	–	–	–
37	C	141	164	C5	53	D	1	–	A2
38	C	–	–	–	54	D	–	–	–
39	C	–	–	–	55	D	–	–	–
40	C	–	–	–	56	D	–	–	–
41	C	140	166	A5	57	D	–	159	B4
42	C	–	–	–	58	D	–	–	–
43	C	–	167	D5	59	D	–	160	A4
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	139	168	E5	62	D	–	161	C4
47	C	–	–	–	63	D	–	–	–
48	C	–	–	E6	64	D	143	162	C3

Table 20. EPM7512AE I/O Pin-Outs (Part 2 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
65	E	–	–	E3	81	F	–	147	F2
66	E	–	–	–	82	F	–	–	–
67	E	7	153	C1	83	F	–	148	F3
68	E	–	–	–	84	F	–	–	–
69	E	–	–	B1	85	F	11	149	F1
70	E	–	–	–	86	F	–	–	–
71	E	–	–	–	87	F	–	–	–
72	E	–	–	–	88	F	–	–	–
73	E	–	154	A1	89	F	–	–	F4
74	E	–	–	–	90	F	–	–	–
75	E	6	155	D2	91	F	10	150	E1
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	5	156	D3	94	F	9	151	D1
79	E	–	–	–	95	F	–	–	–
80	E	4 *(2)*	157	D4 *(2)*	96	F	8	–	E2
97	G	–	–	H6	113	H	19	135	J1
98	G	–	–	–	114	H	–	–	–
99	G	15	141	G5	115	H	–	136	H7
100	G	–	–	–	116	H	–	–	–
101	G	14	142	G4	117	H	18	137	H5
102	G	–	–	–	118	H	–	–	–
103	G	–	–	–	119	H	–	–	–
104	G	–	–	–	120	H	–	–	–
105	G	–	144	G2	121	H	–	–	H2
106	G	–	–	–	122	H	–	–	–
107	G	–	145	G1	123	H	–	138	H3
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	12	146	G6	126	H	–	139	H1
111	G	–	–	–	127	H	–	–	–
112	G	–	–	F5	128	H	16	140	H4

Table 20. EPM7512AE I/O Pin-Outs (Part 3 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
129	I	–	–	K1	145	J	–	122	L2
130	I	–	–	–	146	J	–	–	–
131	I	–	129	J7	147	J	–	–	L1
132	I	–	–	–	148	J	–	–	–
133	I	20 *(2)*	130	J6 *(2)*	149	J	26	123	K6
134	I	–	–	–	150	J	–	–	–
135	I	–	–	–	151	J	–	–	–
136	I	–	–	–	152	J	–	–	–
137	I	–	131	J5	153	J	25	124	K5
138	I	–	–	–	154	J	–	–	–
139	I	–	–	J4	155	J	23	126	K4
140	I	–	–	–	156	J	–	–	–
141	I	–	–	–	157	J	–	–	–
142	I	–	132	J3	158	J	22	127 *(2)*	K3
143	I	–	–	–	159	J	–	–	–
144	I	–	133	J2	160	J	21	128	K2
161	K	29	115	N4	177	L	34	109	R1
162	K	–	–	–	178	L	–	–	–
163	K	–	117	M2	179	L	–	–	–
164	K	–	–	–	180	L	–	–	–
165	K	–	118	M1	181	L	32	110	P2
166	K	–	–	–	182	L	–	–	–
167	K	–	–	–	183	L	–	–	–
168	K	–	–	–	184	L	–	–	–
169	K	28	119	M4	185	L	–	111	N3
170	K	–	–	–	186	L	–	–	–
171	K	–	–	M5	187	L	–	112	N2
172	K	–	–	–	188	L	–	–	–
173	K	–	–	–	189	L	–	–	–
174	K	–	120	L5	190	L	31	113	P1
175	K	–	–	–	191	L	–	–	–
176	K	27	121	L4	192	L	30	114	N1

Table 20. EPM7512AE I/O Pin-Outs (Part 4 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
193	M	–	101	P5	209	N	42	95	R6
194	M	–	–	–	210	N	–	–	–
195	M	–	–	–	211	N	–	–	–
196	M	–	–	–	212	N	–	–	–
197	M	–	102	N5	213	N	41	96	T6
198	M	–	–	–	214	N	–	–	–
199	M	–	–	–	215	N	–	–	–
200	M	–	–	–	216	N	–	–	–
201	M	37	103	T4	217	N	40	97	N6
202	M	–	–	–	218	N	–	–	–
203	M	–	104	R4	219	N	39	98	M6
204	M	–	–	–	220	N	–	–	–
205	M	–	–	–	221	N	–	–	–
206	M	36	106	P4	222	N	–	99	R5
207	M	–	–	–	223	N	–	–	–
208	M	35	108	P3	224	N	38	100	T5
225	O	47	88	R7	241	P	54	79	M9
226	O	–	–	–	242	P	–	–	–
227	O	46	89	P7	243	P	–	–	–
228	O	–	–	–	244	P	–	–	–
229	O	45	90	T7	245	P	–	80	L9
230	O	–	–	–	246	P	–	–	–
231	O	–	–	–	247	P	–	–	–
232	O	–	–	–	248	P	–	–	–
233	O	–	91	L8	249	P	53	81	R8
234	O	–	–	–	250	P	–	–	–
235	O	44	92	N7	251	P	–	84	T8
236	O	–	–	–	252	P	–	–	–
237	O	–	–	–	253	P	–	–	–
238	O	–	–	M7	254	P	49	86	N8
239	O	–	–	–	255	P	–	–	–
240	O	43	93	L7	256	P	48	87	M8

Table 20. EPM7512AE I/O Pin-Outs (Part 5 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
257	Q	55	78	N9	273	R	62	69	R10
258	Q	–	–	–	274	R	–	–	–
259	Q	–	–	–	275	R	63	68	T10
260	Q	–	–	–	276	R	–	–	–
261	Q	–	77	T9	277	R	–	67	M11
262	Q	–	–	–	278	R	–	–	–
263	Q	–	–	–	279	R	–	–	–
264	Q	–	–	–	280	R	–	–	–
265	Q	56	76	R9	281	R	–	66	N11
266	Q	–	–	–	282	R	–	–	–
267	Q	–	73	L10	283	R	65	65	P11
268	Q	–	–	–	284	R	–	–	–
269	Q	–	–	–	285	R	–	–	–
270	Q	60	71	M10	286	R	–	–	R11
271	Q	–	–	–	287	R	–	–	–
272	Q	61	70	N10	288	R	–	64	T11
289	S	66	62	K11	305	T	–	56	P12
290	S	–	–	–	306	T	–	–	–
291	S	–	–	–	307	T	–	–	–
292	S	–	–	–	308	T	–	–	–
293	S	67	61	M12	309	T	–	55	T14
294	S	–	–	–	310	T	–	–	–
295	S	–	–	–	311	T	–	–	–
296	S	–	–	–	312	T	–	–	–
297	S	68	60	N12	313	T	71	54	P13
298	S	–	–	–	314	T	–	–	–
299	S	69	59	T12	315	T	72	53	R13
300	S	–	–	–	316	T	–	–	–
301	S	–	–	–	317	T	–	–	–
302	S	–	58	R12	318	T	–	52	R14
303	S	–	–	–	319	T	–	–	–
304	S	70	57	T13	320	T	74	49	R15

Table 20. EPM7512AE I/O Pin-Outs (Part 6 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
321	U	75	48	P15	337	V	79	42	N16
322	U	–	–	–	338	V	–	–	–
323	U	–	–	–	339	V	80	40	M14
324	U	–	–	–	340	V	–	–	–
325	U	–	47	N15	341	V	–	39	N13
326	U	–	–	–	342	V	–	–	–
327	U	–	–	–	343	V	–	–	–
328	U	–	–	–	344	V	–	–	–
329	U	–	46	T16	345	V	81	38	M16
330	U	–	–	–	346	V	–	–	–
331	U	–	45	R16	347	V	–	–	M13
332	U	–	–	–	348	V	–	–	–
333	U	–	–	–	349	V	–	–	–
334	U	77	44	P16	350	V	–	37	L14
335	U	–	–	–	351	V	–	–	–
336	U	78	43	N14	352	V	–	36	L15
353	W	82	35	L16	369	X	89 *(2)*	–	J11 *(2)*
354	W	–	–	–	370	X	–	–	–
355	W	–	–	L13	371	X	–	28	J12
356	W	–	–	–	372	X	–	–	–
357	W	83	34	L12	373	X	–	27	J13
358	W	–	–	–	374	X	–	–	–
359	W	–	–	–	375	X	–	–	–
360	W	–	–	–	376	X	–	–	–
361	W	84	33	K12	377	X	–	26	J14
362	W	–	–	–	378	X	–	–	–
363	W	86	31	K14	379	X	–	–	J15
364	W	–	–	–	380	X	–	–	–
365	W	–	–	–	381	X	–	–	–
366	W	87	30 *(2)*	K15	382	X	–	25	K13
367	W	–	–	–	383	X	–	–	–
368	W	88	29	K16	384	X	90	24	J16

Table 20. EPM7512AE I/O Pin-Outs (Part 7 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
385	Y	91	22	H10	401	Z	–	–	G12
386	Y	–	–	–	402	Z	–	–	–
387	Y	–	21	H11	403	Z	–	16	G13
388	Y	–	–	–	404	Z	–	–	–
389	Y	92	20	H12	405	Z	94	15	G14
390	Y	–	–	–	406	Z	–	–	–
391	Y	–	–	–	407	Z	–	–	–
392	Y	–	–	–	408	Z	–	–	–
393	Y	–	–	H15	409	Z	96	13	G16
394	Y	–	–	–	410	Z	–	–	–
395	Y	–	19	H16	411	Z	–	12	G11
396	Y	–	–	–	412	Z	–	–	–
397	Y	–	–	–	413	Z	–	–	–
398	Y	–	18	H14	414	Z	97	11	F12
399	Y	–	–	–	415	Z	–	–	–
400	Y	93	17	H13	416	Z	–	–	F13
417	AA	–	10	F14	433	BB	–	–	D16
418	AA	–	–	–	434	BB	–	–	–
419	AA	–	9	F15	435	BB	102	4	C16
420	AA	–	–	–	436	BB	–	–	–
421	AA	98	8	F16	437	BB	–	–	B16
422	AA	–	–	–	438	BB	–	–	–
423	AA	–	–	–	439	BB	–	–	–
424	AA	–	–	–	440	BB	–	–	–
425	AA	–	–	E12	441	BB	–	3	A16
426	AA	–	–	–	442	BB	–	–	–
427	AA	99	7	E13	443	BB	103	2	D15
428	AA	–	–	–	444	BB	–	–	–
429	AA	–	–	–	445	BB	–	–	–
430	AA	100	6	E14	446	BB	104 *(2)*	1	D13 *(2)*
431	AA	–	–	–	447	BB	–	–	–
432	AA	101	–	E16	448	BB	106	208	C15

Table 20. EPM7512AE I/O Pin-Outs (Part 8 of 8)

MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA	MC	LAβ	144-Pin TQFP	208-Pin PQFP, *(1)*	256-Pin FineLine βGA
449	CC	–	–	B15	465	DD	–	202	C13
450	CC	–	–	–	466	DD	–	–	–
451	CC	–	–	–	467	DD	–	–	–
452	CC	–	–	–	468	DD	–	–	–
453	CC	107	–	A15	469	DD	110	201	D12
454	CC	–	–	–	470	DD	–	–	–
455	CC	–	–	–	471	DD	–	–	–
456	CC	–	–	–	472	DD	–	–	–
457	CC	108	206	B14	473	DD	111	199	C12
458	CC	–	–	–	474	DD	–	–	–
459	CC	–	205	A14	475	DD	–	198	B12
460	CC	–	–	–	476	DD	–	–	–
461	CC	–	–	–	477	DD	–	–	–
462	CC	–	204	B13	478	DD	112	197	A12
463	CC	–	–	–	479	DD	–	–	–
464	CC	109	203	A13	480	DD	–	–	E11
481	EE	–	196	D11	497	FF	118	192	D10
482	EE	–	–	–	498	FF	–	–	–
483	EE	–	–	–	499	FF	–	–	–
484	EE	–	–	–	500	FF	–	–	–
485	EE	113	195	C11	501	FF	–	–	C10
486	EE	–	–	–	502	FF	–	–	–
487	EE	–	–	–	503	FF	–	–	–
488	EE	–	–	–	504	FF	–	–	–
489	EE	114	194	A11	505	FF	119	190	A10
490	EE	–	–	–	506	FF	–	–	–
491	EE	116	193	B11	507	FF	120	189 *(2)*	J10
492	EE	–	–	–	508	FF	–	–	–
493	EE	–	–	–	509	FF	–	–	–
494	EE	117	–	F10	510	FF	121	188	F9
495	EE	–	–	–	511	FF	–	–	–
496	EE	–	–	E10	512	FF	122	187	A9

Notes:

(1) The EPM7512AE device in the 208-pin PQFP package supports vertical migration from the EPM7256E, EPM7256S, and EPM7256A devices. The EPM7512AE device contains additional I/O pins which are no connects on the EPM7256E, EPM7256S, and EPM7256A devices. To support these additional I/O pins, the EPM7512AE device has two additional VCCIO (pins 105 and 207) and GNDIO (pins 51 and 158) pins that are no-connect pins on the EPM7256E, EPM7256S, and EPM7256A devices. To achieve vertical migration between the EPM7256A and EPM7512AE devices, the no-connect pins 105 and 207 may be tied to VCC and pins 51 and 58 may be tied to GND on the EPM7256A devices. On the EPM7256E and EPM7256S devices, these no-connect pins must not be tied to V_{CC} and ground. The EPM7384AE and EPM7512AE devices have identical pin-outs.

(2) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

Figures 13, 14, 15, 16, 17, and 18 show the package pin-out diagrams for MAX 7000A devices.

Figure 13. 84-Pin PLCC Package Pin-Out Diagram

Package outline not drawn to scale.

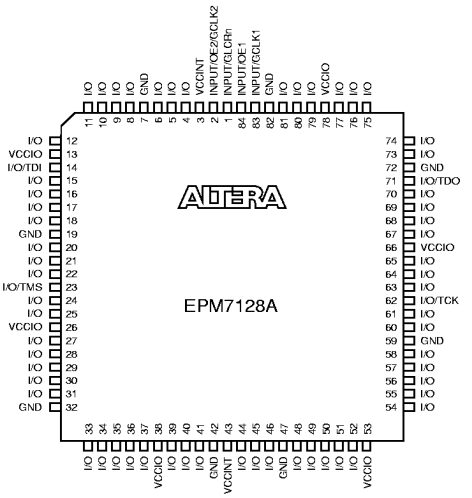


Figure 14. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

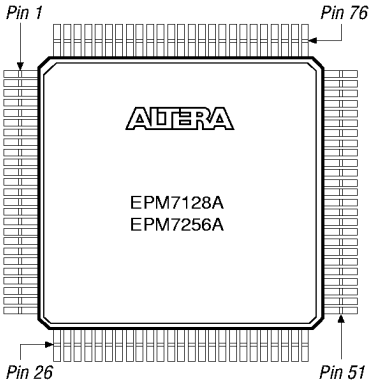


Figure 15. 100-Pin FineLine βGA Package

Package outline not drawn to scale.

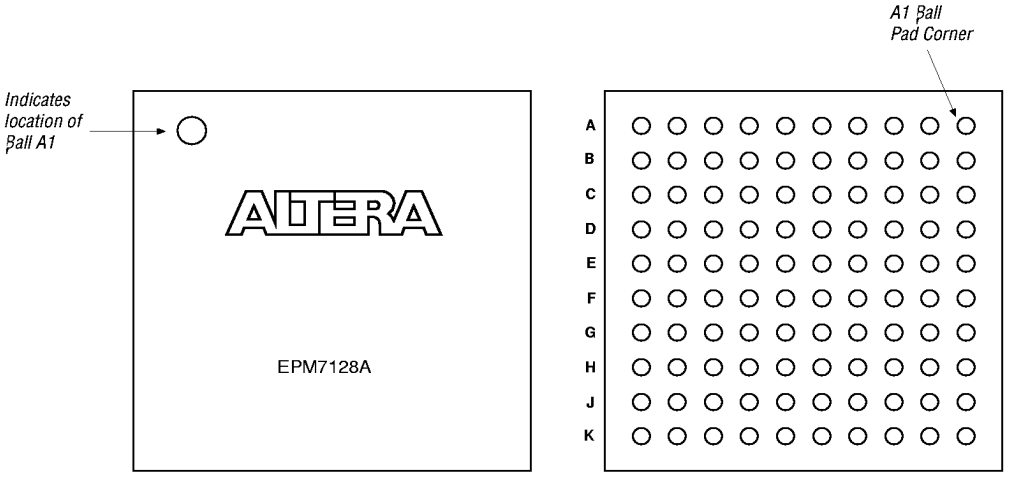


Figure 16. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

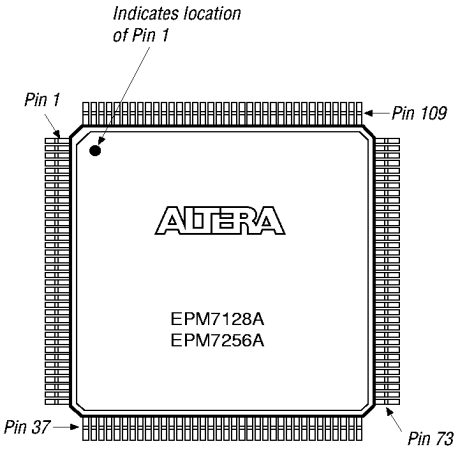
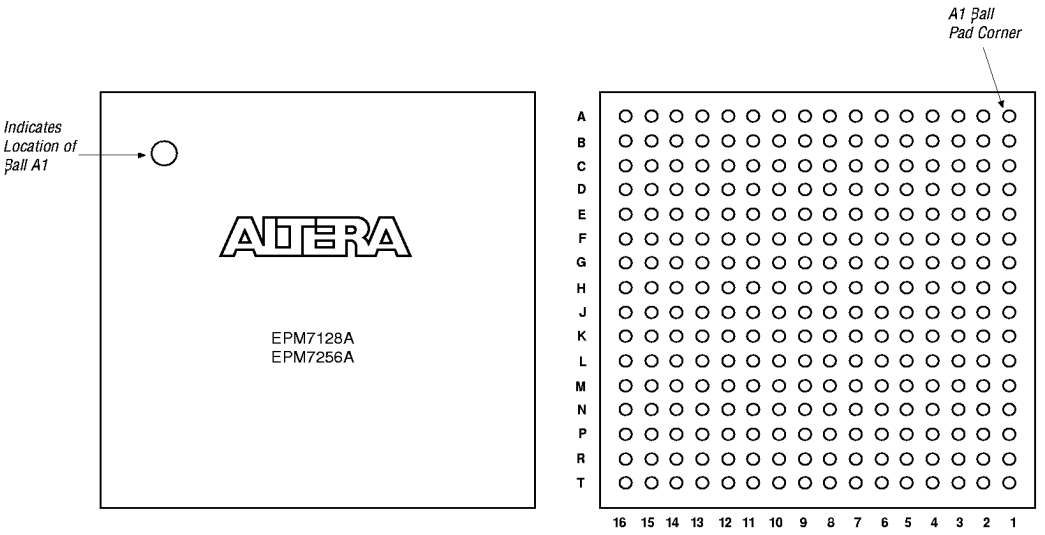


Figure 17. 208-Pin QFP Package Pin-Out Diagram

Package outline not drawn to scale.

Figure 18. 256-Pin FineLine βGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000A Programmable Logic Device Family Data Sheet* version 1.3 supersedes previous versions.

Version 1.3 Changes

- Added timing information for -4 speed grade MAX 7000AE devices.

Version 1.2 Changes

- Changed the t_{SU} value for EPM7032AE and EPM7064AE devices in Table 1. Changed the t_{FSU} value for the EPM7256A device in Table 1.
- Added bullet about MAX 7000A support for hot-socketing to the features list.
- Deleted value for EPM7256A, 100-pin FineLine BGA package in Table 3.
- Changed Figure 1 to read 6 to 16 rather than 3 to 16.
- Updated R_{ISP} in the MAX 7000A Device DC Operating Conditions table.
- Changed Notes 8, 9, and 10 below MAX 7000A Device Capacitance table.
- Updated hot-socketing information.
- Updated EPM7128A AC Operating Conditions table.
- Added MAX 7000AE Operating Conditions table.

- Changed Note (2) to AC Operating Conditions table.
- Added EPM7032AE and EPM7064AE ICC Equation Constants to Table 7.
- Added EPM7064AE and EPM7032AE information to Figure 12.
- Added Tables 12 through 20.
- Corrected the name of pins 25 and 26 to IO and VCCIO, respectively (see Figure 13).

Version 1.11 Changes

The *MAX 7000A Programmable Logic Device Family Data Sheet* version 1.11 contains the following changes:

- Corrected pin-out information in Table 11 for EPM7256A devices in 144-pin TQFP packages.
- Corrected information in the 100-pin FineLine BGA package pin-out diagram and 256-pin FineLine BGA package pin-out diagram.

Version 1.10 Changes

The *MAX 7000A Programmable Logic Device Family Data Sheet* version 1.10 contained the following changes:

- Added description of "F" suffix devices to the In-System Programmability (ISP) section.
- Updated timing information for EPM7128A and EPM7256A devices.
- Added pin-out information for EPM7128A and EPM7256A devices.
- Added power information for EPM7128A and EPM7256A devices.
- Renamed MAX 7000A devices with ISP enhancements as MAX 7000AE.
- Corrected voltage levels in the Absolute Maximum Ratings table.

Version 1.01 Changes

The *MAX 7000A Programmable Logic Device Family Data Sheet* version 1.01 contained the following changes:

- Clarified exclusion of EPM7128A and EPM7256A devices in the Features section.
- Corrected the number of pin- or logic-driven output enable signals in the Features section.
- Clarified the function of I/O pins during in-system programming in the In-System Programmability (ISP) section.
- Deleted note from Figure 10 about non-availability in 44-pin devices.
- Corrected GND pin information in Table 8.

- Added 144-pin TQFP pin-out information to Tables 8 and 9.
- Made minor textual, illustration, and style changes to the data sheet.

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