

EPM7096 EPLD

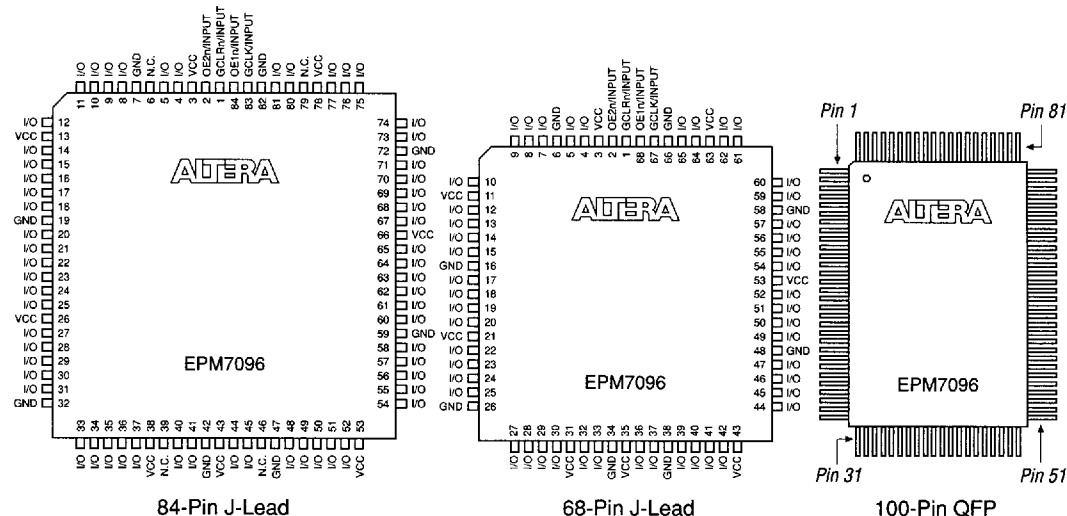
Features

- ❑ High-density, erasable CMOS EPLD based on second-generation MAX architecture
 - 1,800 usable gates
 - Combinatorial speeds with $t_{PD} = 7.5$ ns
 - Counter frequencies up to 125 MHz
- ❑ Advanced 0.8-micron CMOS EEPROM technology
- ❑ Programmable I/O architecture providing up to 76 inputs or 72 outputs
- ❑ 96 advanced macrocells to efficiently implement registered and complex combinatorial logic
- ❑ Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- ❑ Available in the following packages (see Figure 18):
 - 68- and 84-pin plastic J-lead chip carrier (PLCC)
 - 100-pin EIAJ-standard plastic quad flat pack (PQFP)

Preliminary Information

Figure 18. EPM7096 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 5 and 6 in this data sheet for pin-out information.



General Description

The Altera EPM7096 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 19. Fabricated on a 0.8-micron EEPROM technology, the EPM7096 provides 1,800 usable gates, counter speeds of 125 MHz, and propagation delays of 7.5 ns. The EPM7096 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and

Figure 19. EPM7096 Block Diagram

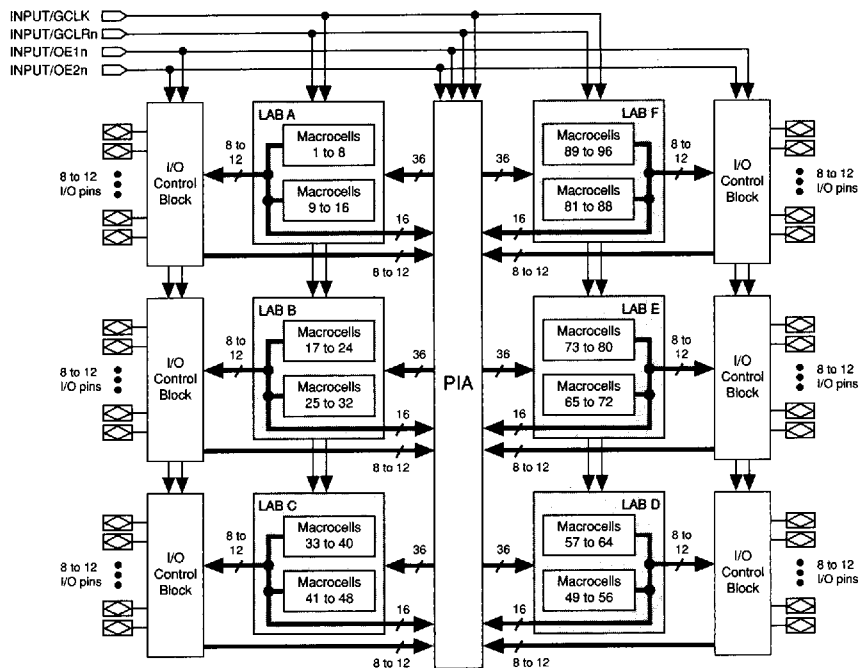


Figure 20 shows the output drive characteristics of EPM7096 I/O pins.

Figure 20. EPM7096 Output Drive Characteristics

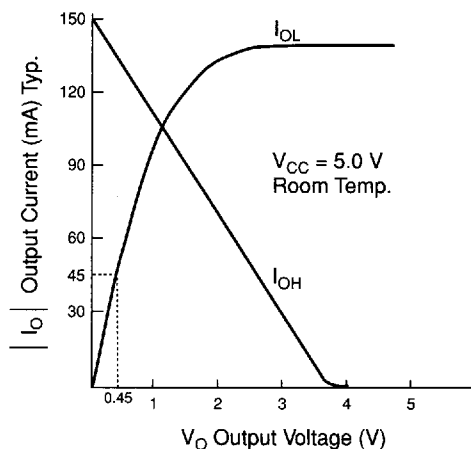


Figure 21 shows typical supply current versus frequency for the EPM7096.

Figure 21. EPM7096 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:

$$I_{CC} = (0.91 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0053 \times MC) \times f_{MAX}]$$

The parameters for this equation are:

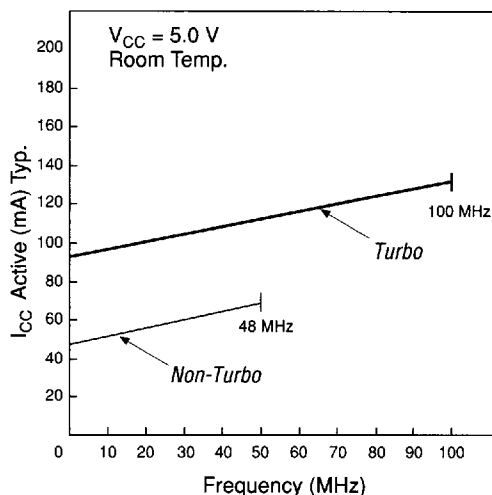
MC_{TON} = number of macrocells used with Turbo Bit on

MC_{TOFF} = number of macrocells used with Turbo Bit off

MC = total number of macrocells used in the design
($MC_{TON} + MC_{TOFF}$)

f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions ($V_{CC} = 5.0$ V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



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Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-2.0	7.0	V
V_I	DC input voltage	Note (1)	-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		-25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	-40	85	°C
T_C	Case temperature	For military use	-55	125	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level TTL output voltage	$I_{OH} = -4$ mA DC	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	-10		10	μA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	-40		40	μA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	$V_I =$ GND, No load Note (4)		50		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	$V_I =$ GND, No load, $f = 1.0$ MHz, Note (4)		55		mA

Capacitance Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		12	pF

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AC Operating Conditions Note (3)

External Timing Parameters			EPM7096-7		EPM7096-10		EPM7096-12		EPM7096-15		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10		12		15	ns
t_{PD2}	I/O input to non-registered output			7.5		10		12		15	ns
t_{SU}	Global clock setup time		6		8		10		11		ns
t_H	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.5		5		6		8	ns
t_{CH}	Global clock high time		3		4		4		5		ns
t_{CL}	Global clock low time		3		4		4		5		ns
t_{ASU}	Array clock setup time		3		3		4		4		ns
t_{AH}	Array clock hold time		2		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.5		10		12		15	ns
t_{ACH}	Array clock high time		3		4		5		6		ns
t_{ACL}	Array clock low time		3		4		5		6		ns
t_{CNT}	Minimum global clock period			8		10		11		13	ns
f_{CNT}	Max. int. global clock frequency	Note (4)	125.0		100		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			8		10		11		13	ns
f_{ACNT}	Max. int. array clock frequency	Note (4)	125.0		100		90.9		76.9		MHz
f_{MAX}	Maximum clock frequency	Note (6)	166.7		125		125		100		MHz

Internal Timing Parameters			EPM7096-7		EPM7096-10		EPM7096-12		EPM7096-15		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.5		1		2		2	ns
t_{IO}	I/O input pad and buffer delay			0.5		1		2		2	ns
t_{SEXP}	Shared expander delay			4		5		7		8	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		1		1	ns
t_{LAD}	Logic array delay			3		5		5		6	ns
t_{LAC}	Logic control array delay			3		5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		2		3		4	ns
t_{ZX}	Output buffer enable delay			4		5		6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		5		6		6	ns
t_{SU}	Register setup time		3		3		4		4		ns
t_H	Register hold time		2		3		4		4		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			3		5		5		6	ns
t_{EN}	Register enable time			3		5		5		6	ns
t_{GLOB}	Global control delay			1		1		0		1	ns
t_{PRE}	Register preset time			2		3		3		4	ns
t_{CLR}	Register clear time			2		3		3		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		1		1		2	ns
t_{LPA}	Low power adder	Note (7)		10		11		12		13	ns

Notes to tables:

- (1) Minimum DC input is -0.3 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- (2) Typical values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{ V}$.
- (3) Operating conditions: $V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C for commercial use.
 $V_{CC} = 5.0\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C for industrial use.
 $V_{CC} = 5.0\text{ V} \pm 10\%$, $T_C = -55^\circ\text{C}$ to 125°C for military use.
- (4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0°C .
- (5) Capacitance measured at 25°C . Sample-tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF .
- (6) The f_{MAX} values represent the highest frequency for pipelined data.
- (7) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0°C to 70°C)	EPM7096-10, EPM7096-12, EPM7096-15
Industrial Temp.	(-40°C to 85°C)	EPM7096-15
Military Temp.	(-55°C to 125°C)	Consult factory

Product Replacement Guide

The following table shows which EEPROM EPM7096 devices should be used as replacements for the earlier EPROM EPM7096 devices.

EPROM Device	EEPROM Device
EPM7096	EPM7096-15
EPM7096-2	EPM7096-15
EPM7096-3	EPM7096-15

Pin-Out Information

Tables 5 and 6 provide pin-out information for the EPM7096 packages.

Table 5. EPM7096 Dedicated Pin-Outs			
Dedicated Pin	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
GCLK	67	83	89
GCLRn	1	1	91
OE1n	68	84	90
OE2n	2	2	92
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCC	3, 11, 21, 31, 35, 43, 53, 63	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93
No Connect (N.C.)	—	6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96

Table 6. EPM7096 I/O Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
1	A	13	16	8	17	B	23	28	23
2	A	—	—	—	18	B	—	—	—
3	A	—	15	7	19	B	22	27	22
4	A	12	14	6	20	B	—	—	21
5	A	—	—	4	21	B	20	25	19
6	A	10	12	3	22	B	—	24	18
7	A	—	—	—	23	B	—	—	—
8	A	9	11	2	24	B	19	23	17
9	A	8	10	1	25	B	18	22	16
10	A	—	—	—	26	B	—	—	—
11	A	—	9	100	27	B	17	21	15
12	A	7	8	99	28	B	—	20	14
13	A	—	—	98	29	B	15	18	12
14	A	5	5	95	30	B	—	—	11
15	A	—	—	—	31	B	—	—	—
16	A	4	4	94	32	B	14	17	10
33	C	33	41	39	49	D	36	44	42
34	C	—	—	—	50	D	—	—	—
35	C	32	40	38	51	D	37	45	43
36	C	—	—	35	52	D	—	—	46
37	C	30	37	34	53	D	39	48	47
38	C	—	36	33	54	D	—	49	48
39	C	—	—	—	55	D	—	—	—
40	C	29	35	32	56	D	40	50	49
41	C	28	34	31	57	D	41	51	50
42	C	—	—	—	58	D	—	—	—
43	C	27	33	30	59	D	42	52	51
44	C	—	—	29	60	D	—	—	52
45	C	25	31	27	61	D	44	54	54
46	C	—	30	26	62	D	—	55	55
47	C	—	—	—	63	D	—	—	—
48	C	24	29	25	64	D	45	56	56

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MAX 7000

Table 6. EPM7096 I/O Pin-Outs (Part 2 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
65	E	46	57	58	81	F	56	69	73
66	E	—	—	—	82	F	—	—	—
67	E	47	58	59	83	F	—	70	74
68	E	—	—	60	84	F	57	71	75
69	E	49	60	62	85	F	—	—	77
70	E	—	61	63	86	F	59	73	78
71	E	—	—	—	87	F	—	—	—
72	E	50	62	64	88	F	60	74	79
73	E	51	63	65	89	F	61	75	80
74	E	—	—	—	90	F	—	—	—
75	E	52	64	66	91	F	—	76	81
76	E	—	65	67	92	F	62	77	82
77	E	54	67	69	93	F	—	—	83
78	E	—	—	70	94	F	64	80	86
79	E	—	—	—	95	F	—	—	—
80	E	55	68	71	96	F	65	81	87