

Features

- 8-Bit Resolution.
- Maximum conversion rate: 5 MSPS. (TYP).
- Low power consumption: 60 mW.
- 3-state TTL compatible output.
- Power supply : 5V single.
- Reference impedance : 300 Ω (TYP)
- Low input capacitance : 20pF.
- Built-in reference voltage self bias circuit.

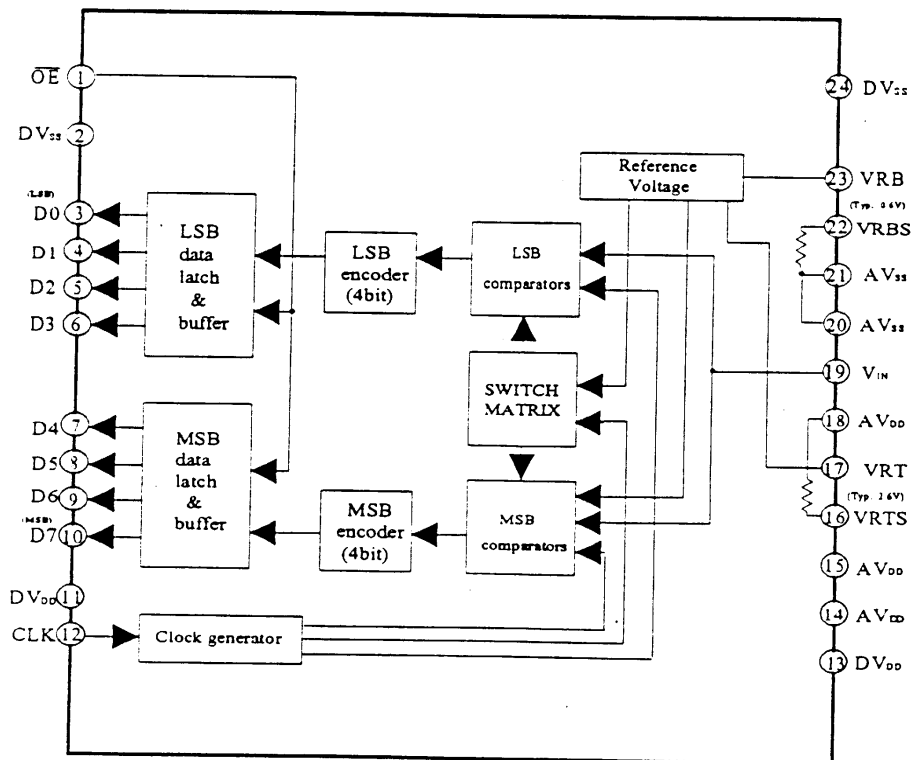
DESCRIPTION

ES52096 is an 8 Bit CMOS A / D converter for scanner use. Conversion rates up to 5 MSPS can be attained while operating at low power consumption. This A / D converter consists of a reference voltage, data latches, encoder, comparators and clock generator.

APPLICATIONS

- Scanner.

Block Diagram



PIN Assignment

1	OE	DV _{SS}	24
2	DV _{SS}	VRB	23
3	D0	ARBS	22
4	D1	AV _{SS}	21
5	D2	AV _{SS}	20
6	D3	V _{IN}	19
7		AV _{DD}	18
8	D5	VRT	17
9	D6	VRTS	16
10	D7	AV _{DD}	15
11	DV _{DD}	AV _{DD}	14
12	CLK	DV _{DD}	13

24PIN SOP, 24 PIN DIP

Pin Designation & Function

NO	Symbol	Description
2, 24	DV _{SS}	Digital GND
3 to 10	D0 to D7	D0(LSB)to D7 (MSB)output
12	CLK	Clock input
1	OE	When OE = LOW , data is output When OE =HIGH , D0 to D7 Pin turn to high impedance
16	V _{RTS}	Shorted with V _{RT} , generates+ 2.6v
20, 21	AV _{SS}	Analog GND
11,13	DV _{DD}	Digital+5v
14, 15, 18	AV _{DD}	Analog +5v
17	V _{RT}	Reference voltage(Top)
22	V _{RBS}	Shorted with V _{RB} ,generates +0.6v
19	V _{IN}	Analog input
23	V _{RB}	Reference voltage (Bottom)

Absolute Maximum Rating

Supply voltage(V _{DD})	-----	7V
Reference voltage(V _{RT} , V _{RB})	-----	V _{DD} ~V _{SS}
Analog input voltage(V _{IN})	-----	V _{DD} ~V _{SS}
Digital input voltage(CLK)	-----	V _{DD} ~V _{SS}
Digital output voltage(V _{OH} , V _{OL})	-----	V _{DD} ~V _{SS}
Storage temperature(T _{STG})	-----	-55~+150°C
Operating temperature(T _{OP})	-----	-20~75°C
Lead Temperature(Soldering 10seconds)	-----	+300°C

Recommended Operating Conditions

Supply voltage	AV _{DD} , AV _{SS}	4.75 to 5.25	V
	DV _{DD} , AV _{SS}	4.75 to 5.25	V
	D _{GND} , A _{GND}	0 to 100	mV
Reference input voltage	V _{RB}	0 and above	V
	V _{RT}	V _{DD} and below	V
	V _{RT} -V _{RB}	1.0 to V _{DD}	V
Analog input voltage	V _{IN}	V _{RB} to V _{RT}	V

Electrical Characteristics

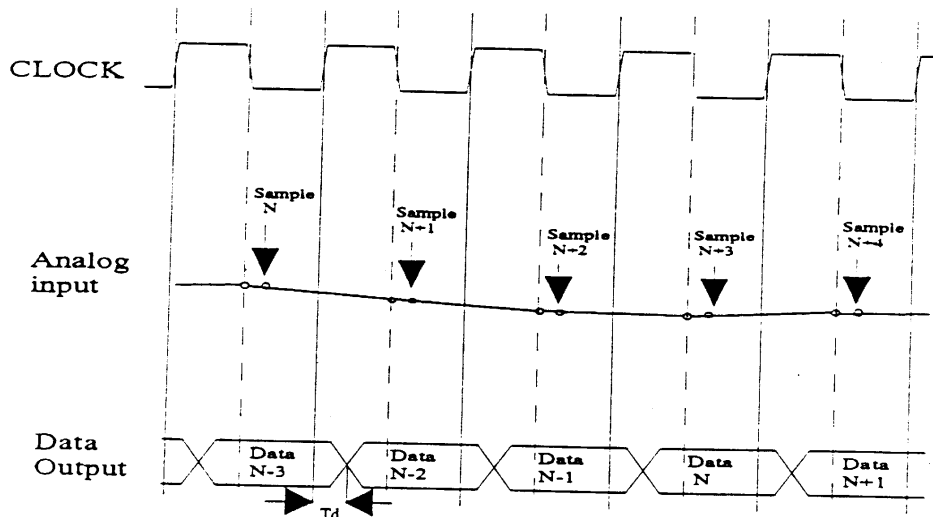
$T_a = 25^{\circ}\text{C}$, $F_c = 5\text{MSPS}$, $V_{DD} = +5\text{V}$, $V_{RB} = 0.6\text{V}$, $V_{RT} = 2.6\text{V}$

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Maximum conversion speed	F_c	$V_{IN} = 0.6\text{V TO } 2.6\text{V}$ $F_{in} = 1\text{kHz ramp}$	—	5	—	MSPS
Reference resistance	R_{ref}	V_{RT} to V_{RB}	230	300	450	Ω
Digital input voltage	V_{IH}		4.0	—	—	V
Digital input voltage	V_{IL}		—	—	1.0	V
Digital output current	I_{OH}	$\overline{OE} = V_{SS}$, $V_{DD} = 4.75\text{V}$ $V_{OH} = V_{DD} \sim 0.5\text{V}$	-1.1	—	—	mA
Digital output current	I_{OL}	$OE = V_{SS}$, $V_{DD} = 4.75\text{V}$ $V_{OL} = 0.4\text{V}$	3.7	—	—	mA
Differential Non-linearity	E_D	$F_c = 5\text{MSPS}$ $V_{in} = 0.6\text{v to } 2.6\text{v}$	—	± 0.3	± 0.5	LSB
Integral Non-linearity	E_L	$F_c = 5\text{MSPS}$ $V_{in} = 0.6\text{v to } 2.6\text{v}$	—	± 0.5	± 1.3	LSB

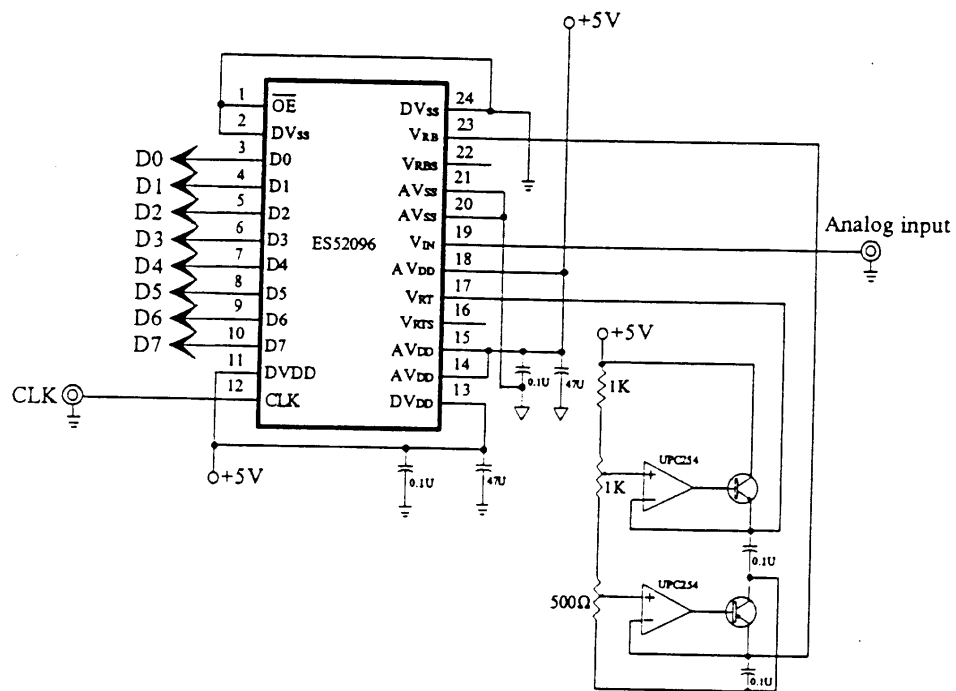
$T_a = 25^{\circ}\text{C}$, $F_c = 20\text{MSPS}$, $V_{DD} = +5\text{V}$, $V_{RB} = 0.6\text{V}$, $V_{RT} = 2.6\text{V}$

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Digital input Current	I_{IH}	$V_{DD} = 5.25\text{V}$ $V_{IH} = V_{DD}$	—	—	5	μA
Digital input Current	I_{IL}	$V_{DD} = 5.25\text{V}$ $V_{IL} = 0\text{V}$	—	—	5	μA
Supply current	I_{DD}	$F_c = 20\text{MSPS}$ NTSC ramp wave input	—	22	25	mA
Analog input Capacitance	C_{IN}	$V_{in} = 1.5\text{V} + 0.07\text{V}_{ms}$	—	11	—	pF
Reference pin current	I_{REF}		4.5	6.6	8.7	mA
Digital output current	I_{OZH}	$\overline{OE} = V_{SS}$, $V_{DD} = 5.25\text{V}$ $V_{OH} = V_{DD}$	—	—	16	μA
Digital output current	I_{OLH}	$\overline{OE} = V_{SS}$, $V_{DD} = 5.25\text{V}$ $V_{OL} = 0\text{V}$	—	—	16	μA
Self bias 1	$V_{RB} 1$	Short V_{RB} and V_{RBS}	0.6	0.64	0.68	V
	$V_{RT} 1 - V_{RB} 1$	Short V_{RT} and V_{RTS}	1.96	2.09	2.21	
Self bias 2	V_{RT2}	$V_{RB} = \text{AGND}$ Short V_{RT} and V_{RTS}	2.25	2.39	2.53	V
Offset voltage	E_{OT}		-10	-35	-60	mV
Offset voltage	E_{OB}		0	15	45	mV
Output data delay	T_d		—	15	30	ns

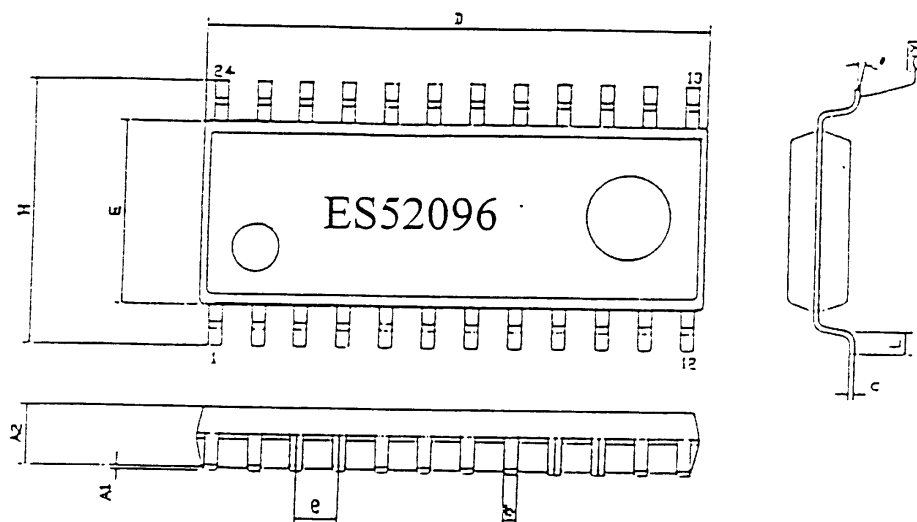
Timing Diagram



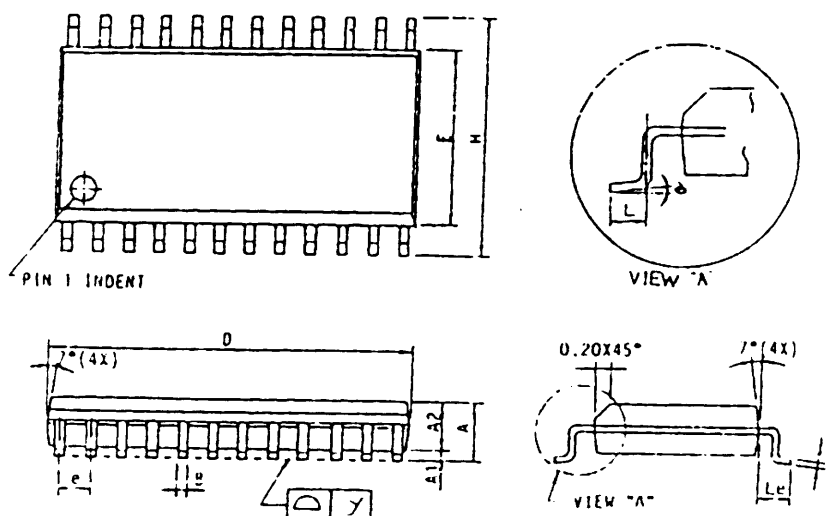
Application Circuit



ES52096 (24 PINS SOP)



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.06	0.11	0.21	0.002	0.004	0.008
A2	1.70	1.80	1.90	0.067	0.071	0.075
b	0.35	0.40	0.50	0.014	0.016	0.020
c	0.10	0.15	0.25	0.004	0.006	0.010
D	14.80	14.90	15.00	0.583	0.587	0.591
E	5.30	5.40	5.50	0.209	0.213	0.217
e	1.17	1.27	1.37	0.046	0.050	0.054
H	7.55	7.80	8.05	0.297	0.307	0.317
L	—	0.50	—	—	0.020	—
Y	—	—	0.10	—	—	0.004
θ	0°	—	10°	0°	—	10°

ES52096S3


PACKAGE NAME	LEAD TREATMENT	WIGHT(g)	ETIAJ CODE NO.	JEDEC CODE NO.		
24L-W/B	SOLDER PLATING	—	—	MS-013 AD		
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.49	2.65	0.092	0.098	0.105
A1	0.10	0.20	0.30	0.003	0.008	0.012
A2	2.20	2.28	2.36	0.087	0.090	0.093
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.22	0.25	0.33	0.009	0.010	0.013
D	15.20	15.40	15.49	0.598	0.606	0.610
E	7.37	7.50	7.60	0.290	0.295	0.299
e	—	1.27	—	—	0.050	—
H	10.00	10.35	10.65	0.393	0.407	0.420
L	0.40	—	1.27	0.015	—	0.050
Le	0.76	—	—	0.030	—	—
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°