3.3 Electrical Specifications

3.3.1 Maximum Ratings

Storage temperature	-40 to +125° C
Operating free-air temperature range	0 to +70° C
Supply voltage applied to ground potential	-0.5 to +7.0 V
DC voltage applied to outputs for high output state	-0.5 to Vdd max.
DC input voltage	+4.75V to +5.25 V
Supply current	200mA typ / 300 max.
Analog output current	45mA
Reference current	-15mA

3.3.2 Electrical Characteristics

The following condition applies unless otherwise specified: T(A) = 0 + 70° Vdd = 5.0 V ±5%

DC Characteristics Over Operating Temperature							
Symbol	**Parameter**	**I/O Cell**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{IH}	High Level Input Voltage	TTL		2.0			V
		CMOS		3.5			
		CMOS Schmidt trigger		4.0			
V_{IL}	Low Level Input Voltage	TTL				0.8	V
		CMOS				1.5	
		CMOS Schmidt trigger				1.0	
I_{IH}	High Level Output Current	Input buffer	V_{IN}=VCC	-10		10	uA
		Input buffer with pull-down		10		200	
I_{IL}	Low Level Output Current	Input buffer	V_{IN}=GND	-10		10	uA
		Input buffer with pull-up		-200		-10	
V_{OH}	High Level Output Voltage	BT2, BD2 TTL	I_{OH}=-2mA	2.4			V
		BT4, BT4 TTL	I_{OH}=-4mA				
		BT8, BD8 TTL	I_{OH}=-8mA				
		BTPCI, BDPCI TTL	I_{OH}=-2mA	2.4			
		ALL TTL	I_{OH}=-1uA	VCC-0.05			
		BT4, BD4 CMOS	I_{OH}=-4mA	3.5			
V_{OL}	Low Level Output Voltage	BT2, BD2 TTL	I_{OL}=2mA			0.5	V
		BT4, BT4 TTL	I_{OL}=4mA				
		BT8, BD8 TTL	I_{OL}=8mA				
		BTPCI, BDPCI TTL	I_{OL}=6mA			0.55	
		ALL TTL	I_{OL}=1uA			0.05	
		BT4, BD4 CMOS	I_{OL}=4mA			1.5	
I_{OZ}	High Impedance Leakage current	Output buffer	V_{OUT}=VCC or GND	-10		10	uA
		Output buffer with pull-up		-200		-10	
		Output buffer with pull-down		10		200	
V_H	Schmidt Trigger Hysteresis Voltage				0.6		V

NOTE: The MDRAM outputs (see pins below) are specifically designed to work into 220Ω loads, to VDD and ground, with reduced swing and a 50 percent duty cycle to achieve the high data exchange rate. Different loads may affect performance.

MDRAM Outputs	
Pins	**Function**
MD1<15:0>, MD0<15:0>	input/output
MM1<1:0>, MM0<1:0>	input to MDRAM
CLK1, CLK0	input to MDRAM

3.3.3 DAC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{REF}	Reference voltage		1.10	1.35	V
V_O (max)	Maximum output voltage	$I_O \leq 10mA$		1.5	V
I_O (max)	Maximum output current	$V_O \leq 1$ V		21	mA
	Full scale error	note A, B		±5	%
	DAC to DAC correlation	note B		±2	%
	Integral linearity, 6-bit	note B		±0.5	LSB
	Integral linearity, 8-bit	note B		±1	LSB
	Full-scale settling time*, 6-bit	note C		28	ns
	Full-scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

3.3.4 PLL Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
F_D	Frequency change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%
f_0	CLOCK0 operating range*		25	135	MHz
f_1	CLOCK1 operating range*		25	135	MHz
d_t	Duty cycle*		40/60	60/40	%
j_{1s}	Jitter, one sigma*			130ps	ps
j_{abs}	Jitter, absolute*		-300ps	300ps	ps
f_{ref}	Input reference frequency	typically 14.318MHz	5	25	MHz

NOTES:

A. Full scale error is derived from design equation

$$\{[(F.S.I_{out})R_L - 2.1\ (I_{REF})R_L]/[2.1(I_{REF})R_L]\}\ 100\%$$

$V_{BLACK\ LEVEL} = 0V$
$F.S.I_{OUT}$ = Actual full scale measured output

B. $R = 37.5\Omega$, $I_{REF} = -8.88mA$, $J_{REF} = V_{REF}/R_{SET}$

C. $Z_l = 37.5\Omega + 30pF$, $I_{REF} = -8.88mA$

Appendix C. Mechanical Specification

ET6000 208-pin Plastic Quad Flat Package