


SGS-THOMSON
 MICROELECTRONICS

T-75-11-13

ETC5057
ETC5054

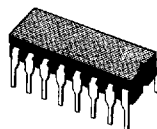
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SERIAL INTERFACE CODEC/FILTER

■ COMPLETE CODEC AND FILTERING SYSTEM (COMBO) INCLUDING :

- Transmit high-pass and low-pass filtering
- Receive low-pass filter with sin x/x correction
- Active RC noise filters
- A-law or μ -law compatible COder and DECOder
- Internal precision voltage reference
- Serial I/O interface
- Internal auto-zero circuitry
- A-LAW, 16-PINS-ETC5057
- μ -LAW WITHOUT SIGNALING, 16-PINS-ETC5054
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- SECOND SOURCE OF TP3057, TP3054

loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.



DIP16
 (Ceramic) J
 (Plastic) N

ORDER CODES : ETC5057J
 ETC5054J
 ETC5057N
 ETC5054N

DESCRIPTION

The ETC5057/ETC5054 family consists of A-law and μ -law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in figure 1, and a serial PCM interface. The devices are fabricated using double poly CMOS process.

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ -law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ -law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance

PIN CONNECTION

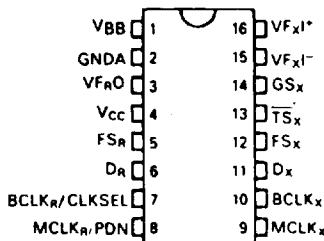
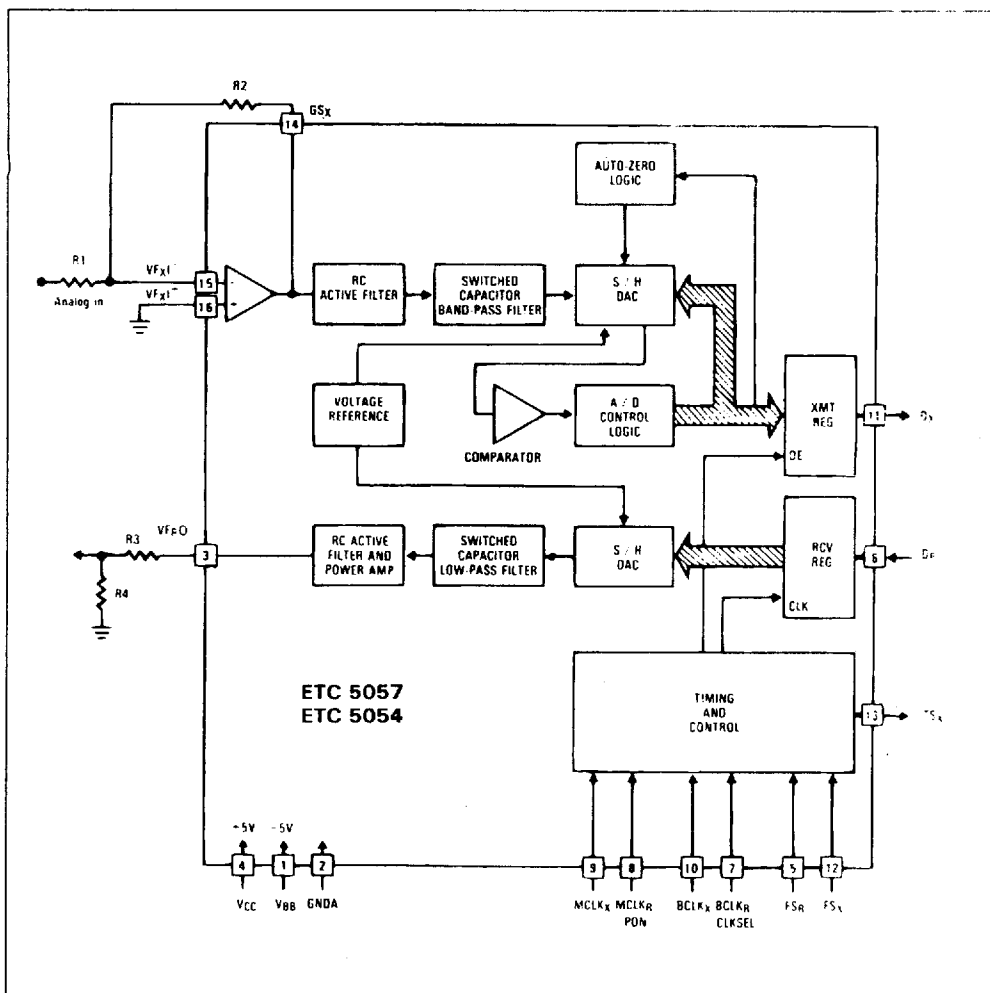


Figure 1 : Block Diagram.



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PIN DESCRIPTION

Name	Pin Type*	N°	Function	Description
V _{BB}	S	1	Negative Power Supply	V _{BB} = - 5 V ± 5 %
GNDA	GND	2	Analog Ground	All signals are referenced to this pin.
VF _{RO}	O	3	Receiver Filter Output	Analog Output of the Receive Filter
V _{CC}	S	4	Positive Power Supply	V _{CC} = + 5 V ± 5 %
FS _R	I	5	Receive Frame Sync Pulse	Enables BCLK _R to shift PCM data into D _R . FS _R is an 8 kHz pulse train. See figures 2,3 and 4 for timing details.
D _R	I	6	Receive Data Input	PCM data is shifted into D _R following the FS _R leading edge.
BCLK _R /CLKSEL	I	7	Shift-in Clock	Shifts data into D _R after the FS _R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLK _X is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
MCLK _R /PDN	I	8	Receive Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK _X , but should be synchronous with MCLK _X for best performance. When MCLK _R is connected continuously low, MCLK _X is selected for all internal timing. When MCLK _R is connected continuously high, the device is powered down.
MCLK _X	I	9	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK _R .
BCLK _X	I	10	Shift out Clock	Shift out the PCM data on D _X . May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK _X .
D _X	O	11	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS _X .
FS _X	I	12	Transmit Frame Sync Pulse	Enables BCLK _X to shift out the PCM data on D _X . FS _X is an 8 kHz pulse train. See figures 2, 3 and 4 for timing details.
TS _X	O	13	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Recommended to be grounded if not used.
GS _X	O	14	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF _{XI} -	I	15	Inverting Amplifier Input	Inverting input of the transmit input amplifier.
VF _{XI} +	I	16	Non-inverting Amplifier Input	Non-inverting input of the transmit input amplifier.

* I : Input, o : Output, S : Power Supply.

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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_x and V_{FR0} outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R/PDN$ pin and FS_x and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R/PDN$ pin high; the alternative is to hold both FS_x and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_x or FS_R pulse. Power-up will occur on the first FS_x or FS_R pulse. The TRI-STATE PCM data output, D_x , will remain in the high impedance state until the second FS_x pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_x$ and the $MCLK_R/PDN$ pin can be used as a power-down control. A low level on $MCLK_R/PDN$ powers up the device and a high level powers down the device. In either case, $MCLK_x$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_x$ and the $BCLK_R/CLKSEL$ can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R/CLKSEL$ pin, $BCLK_x$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R/CLKSEL$. In this synchronous mode, the bit clock, $BCLK_x$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_x$.

Table 1: Selection of Master Clock Frequencies.

$BCLK_R/CLKSEL$	Master Clock Frequency Selected	
	ETC 5057	ETC 5054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_x pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_x output on the positive edge of $BCLK_x$. After 8 bit clock periods, the TRI-STATE D_x output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_x$ (or $BCLK_R$ if running). FS_x and FS_R must be synchronous with $MCLK_x/R$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_x$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_x$, which is easily achieved by applying only static logic levels to the $MCLK_R/PDN$ pin. This will automatically connect $MCLK_x$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_x starts each encoding cycle and must be synchronous with $MCLK_x$ and $BCLK_x$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_x$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_x and FS_R , must be one bit clock period long, with timing relationships specified in figure 3. With FS_x high during a falling edge of $BCLK_x$, the next rising edge of $BCLK_x$ enables the D_x TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_x output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_x$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_x and FS_R , must be three or more bit clock periods long, with timing relationships specified in figure 4. Based on the transmit frame sync, FS_x , the

COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 2). The D_x TRI-STATE output buffer is enabled with the rising edge of FS_x or the rising edge of $BCLK_x$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_x$ rising edges clock out the remaining seven bits. The D_x output is disabled by the falling $BCLK_x$ edge following the eighth rising edge, or by FS_x going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R , will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_x$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 5. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or μ -law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input over-

load (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS_x frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_x at the next FS_x pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which totals 290 μ s. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or μ -law (ETC5054) and the 5th order low pass filter corrects for the $\sin x/x$ attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R , the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_x$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μ s later the decoder DAC output is updated. The total decoder delay is $\sim 10 \mu$ s (decoder update) plus 110 μ s (filter delay) plus 62.5 μ s (1/2 frame), which gives approximately 180 μ s.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND A	7	V
V_{BB}	V_{BB} to GND A	-7	V
V_{IN}, V_{OUT}	Voltage at Any Analog Input or Output	$V_{CC} + 0.3$ to $V_{BB} - 0.3$	V
	Voltage at Any Digital Input or Output	$V_{CC} + 0.3$ to GND A - 0.3	V
T_{oper}	Operating Temperature Range	-25 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

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ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{BB} = -5.0 \text{ V} \pm 5\%$, $G_{NDA} = 0 \text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C (unless otherwise noted); Typical characteristics specified at $V_{CC} = 5.0 \text{ V}$, $V_{BB} = -5.0 \text{ V}$, $T_A = 25^\circ\text{C}$; all signals are referenced to G_{NDA} .

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IL}	Input Low Voltage	–	–	0.6	V
V _{IH}	Input High Voltage	2.2	–	–	V
V _{OL}	Output Low Voltage				V
	I _L = 3.2 mA I _L = 3.2 mA, Open Drain	D _X TS _X	– –	– 0.4 0.4	
V _{OH}	Output High Voltage				V
	I _H = 3.2 mA	D _X	2.4	– –	
I _{IL}	Input Low Current (G _{NDA} ≤ V _{IN} ≤ V _{IL} , all digital inputs)	– 10	–	10	μA
I _{IH}	Input High Current (V _{IH} ≤ V _{IN} ≤ V _{CC}) except BCLK _R /BCLKSEL	– 10	–	10	μA
I _{OZ}	Output Current in High Impedance State (TRI-STATE) (G _{NDA} ≤ V _O ≤ V _{CC})	D _X	– 10	– 10	μA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{IXA}	Input Leakage Current ($-2.5 \text{ V} \leq V \leq +2.5 \text{ V}$) VF_{XI}^+ or VF_{XI}^-	– 200	–	200	nA
R_{IXA}	Input Resistance ($-2.5 \text{ V} \leq V \leq +2.5 \text{ V}$) VF_{XI}^+ or VF_{XI}^-	10	–	–	M Ω
R_{OXA}	Output Resistance (closed loop, unity gain)	–	1	3	Ω
R_{LXA}	Load Resistance	GS_X	10	–	k Ω
C_{LXA}	Load Capacitance	GS_X	–	–	50 pF
V_{OXA}	Output Dynamic Range ($R_L \geq 10 \text{ k}\Omega$)	GS_X	± 2.8	–	V
A_{VXA}	Voltage Gain (VF_{XI}^+ to GS_X)	5000	–	–	V/V
F_{UXA}	Unity Gain Bandwidth	1	2	–	MHz
V_{OSXA}	Offset Voltage	– 20	–	20	mV
V_{CMXA}	Common-mode Voltage	– 2.5	–	2.5	V
$CMRR_{XA}$	Common-mode Rejection Ratio	60	–	–	dB
$PSRR_{XA}$	Power Supply Rejection Ratio	60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R _O RF	Output Resistance VF _R O	—	1	3	Ω
R _L RF	Load Resistance (VF _R O = ± 2.5 V)	600	—	—	Ω
C _L RF	Load Capacitance	—	—	500	pF
VOS _R O	Output DC Offset Voltage	– 200	—	200	mV

ELECTRICAL CHARACTERISTICS (continued)**S 6 S-THOMSON****POWER DISSIPATION** (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC0}	Power-down Current	—	0.5	1.5	mA
I_{BB0}	Power-down Current	—	0.05	0.3	mA
I_{CC1}	Active Current	—	6.0	9.0	mA
I_{BB1}	Active Current	—	6.0	9.0	mA

TIMING SPECIFICATIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clocks Depends on the device used and the BCLK _R /CLKSEL pin.	MCLK _X and MCLK _R — — —	1.536 1.544 2.048	— — —	MHz
t_{WMH}	Width of Master Clock High	MCLK _X and MCLK _R	160	—	ns
t_{WML}	Width of Master Clock Low	MCLK _X and MCLK _R	160	—	ns
t_{RM}	Rise Time of Master Clock	MCLK _X and MCLK _R	—	50	ns
t_{FM}	Fall Time of Master Clock	MCLK _X and MCLK _R	—	50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High ($V_{IH} = 2.2$ V)	160	—	—	ns
t_{WBL}	Width of Bit Clock Low ($V_{IL} = 0.6$ V)	160	—	—	ns
t_{RB}	Rise Time of Bit Clock ($t_{PB} = 488$ ns)	—	—	50	ns
t_{FB}	Fall Time of Bit Clock ($t_{PB} = 488$ ns)	—	—	50	ns
t_{SBFM}	Set-up Time from BCLK _X High to MCLK _X Falling Edge (first bit clock after the leading edge of FS _X)	100	—	—	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0	—	—	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)	80	—	—	ns
t_{HBF1}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only)	FS _X or FS _R	100	—	ns
t_{DZF}	Delay time to valid data from FS _X or BCLK _X , whichever comes later and delay time from FS _X to data output disabled. ($C_L = 0$ pF to 150 pF)	20	—	165	ns
t_{DBD}	Delay Time from BCLK _X High to Data Valid (Load = 150 pF plus 2 LSTTL loads)	0	—	180	ns
t_{DZC}	Delay Time from BCLK _X Low to Data Output Disabled	50	—	165	ns
t_{SDB}	Set-up Time from D _R Valid to BCLK _{R/X} Low	50	—	—	ns
t_{HBD}	Hold Time from BCLK _{R/X} Low to D _R Invalid	50	—	—	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0	—	—	ns

Note : 1. For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

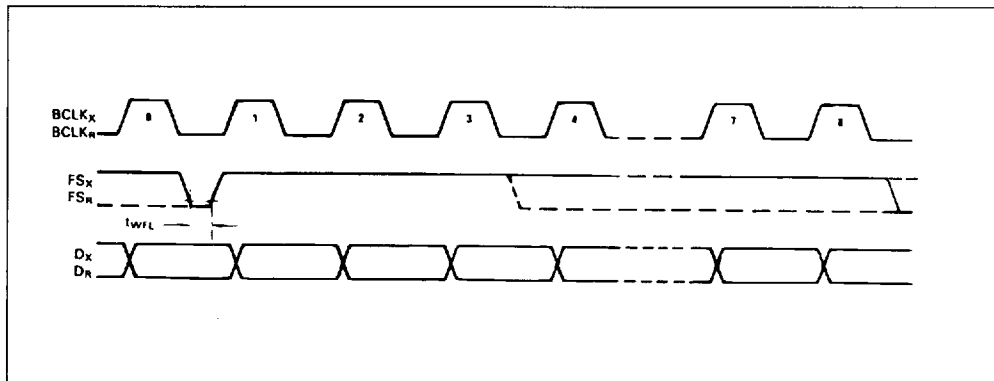
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TIMING SPECIFICATIONS (continued)

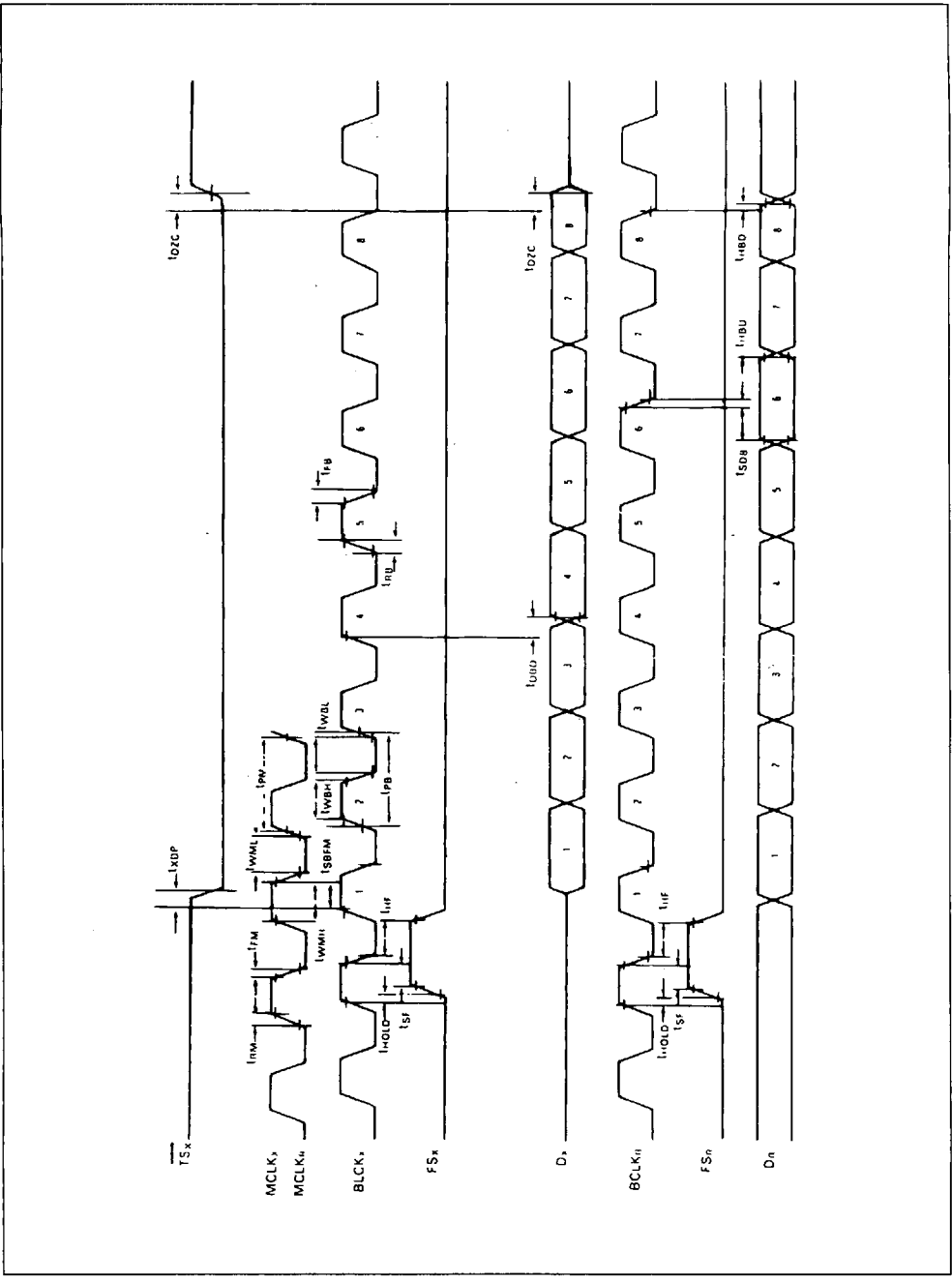
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80	—	—	ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100	—	—	ns
t_{XDP}	Delay Time. To TS_X Low (load = 150 pF plus 2 LSTTL loads)	—	—	140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160	—	—	ns

Note : 1. For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

Figure 2 : 64 k bits/s TIMING DIAGRAM (see next page for complete timing).



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TRANSMISSION CHARACTERISTICS

(all devices) $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$, $G_{ND} = 0\text{ V}$, $f = 1.02\text{ kHz}$, $V_{IN} = 0\text{ dBm0}$ transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0	–	1.2276	–	V_{rms}
t_{MAX}	Max Overload Level 3.14 dBm0 (A LAW) 3.17 dBm0 (U LAW)	– –	2.492 2.501	– –	V_{PK}
G_{XA}	Transmit Gain, Absolute ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{BB} = -5\text{ V}$) Input at $G_{SX} = 0\text{ dBm0}$ at 1020 Hz	– 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA} $f = 16\text{ Hz}$ $f = 50\text{ Hz}$ $f = 60\text{ Hz}$ $f = 180\text{ Hz}$ $f = 200\text{ Hz}$ $f = 300\text{ Hz} - 3000\text{ Hz}$ $f = 3300\text{ Hz}$ $f = 4000\text{ Hz}$ $f = 3400\text{ Hz}$ $f = 4600\text{ Hz}$ and up, measure response from 0 Hz to 4000 Hz	– – – – 2.8 – 1.8 – 0.15 – 0.35 – 0.7 – –	– – – – – – – – – –	– 40 – 30 – 26 – 0.2 – 0.1 0.15 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	– 0.1	–	+ 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$)	– 0.05	–	+ 0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 $V_{FXL}^+ = -40\text{ dBm0}$ to $+3\text{ dBm0}$ $V_{FXL}^- = -50\text{ dBm0}$ to -40 dBm0 $V_{FXL}^* = -55\text{ dBm0}$ to -50 dBm0	– 0.2 – 0.4 – 1.2	– – –	0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{BB} = -5\text{ V}$) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	– 0.15	–	0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} $f = 0\text{ Hz}$ to 3000 Hz $f = 3300\text{ Hz}$ $f = 3400\text{ Hz}$ $f = 4000\text{ Hz}$	– 0.15 – 0.35 – 0.7 –	– – – –	0.15 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	– 0.1	–	+ 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$)	– 0.05	–	+ 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to $+3\text{ dBm0}$ PCM level = – 50 dBm0 to -40 dBm0 PCM level = – 55 dBm0 to -50 dBm0	– 0.2 – 0.4 – 1.2	– – –	0.2 0.4 1.2	dB
V_{RO}	Receive Output Drive Level ($R_L = 600\text{ }\Omega$)	– 2.5	–	2.5	V

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TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D _{XA}	Transmit Delay, Absolute (f = 1600 Hz)	—	290	315	μs
D _{XR}	Transmit Delay, Relative to D _{XA}				μs
	f = 500 Hz – 600 Hz	—	195	220	
	f = 600 Hz – 800 Hz	—	120	145	
	f = 800 Hz – 1000 Hz	—	50	75	
	f = 1000 Hz – 1600 Hz	—	20	40	
	f = 1600 Hz – 2600 Hz	—	55	75	
	f = 2600 Hz – 2800 Hz	—	80	105	
D _{RA}	Receive Delay, Absolute (f = 1600 Hz)	—	180	200	μs
	Receive Delay, Relative to D _{RA}				μs
D _{RR}	f = 500 Hz – 1000 Hz	– 40	– 25	—	
	f = 1000 Hz – 1600 Hz	– 30	– 20	—	
	f = 1600 Hz – 2600 Hz	—	70	90	
	f = 2600 Hz – 2800 Hz	—	100	125	
	f = 2800 Hz – 3000 Hz	—	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N _{XP}	Transmit Noise, P Message Weighted (A LAW, V _{FxI} + = 0 V)	—	– 74	– 69 (note 1)	dBm0p
N _{RP}	Receive Noise, P Message Weighted (U LAW, PCM Code Equals Positive Zero)	—	– 82	– 79	dBm0p
N _{XC}	Transmit Noise, C Message Weighted U LAW (V _{FxI} + = 0 V)	—	12	15	dBm0
N _{RC}	Receive Noise, C Message Weighted (U LAW, PCM Code Equals Alternating Positive and Negative Zero)	—	8	11	dBm0
N _{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, V _{FxI} + = 0 Vrms	—	—	– 53	dBm0
PPSR _X	Positive Power Supply Rejection, Transmit V _{FxI} + = 0 Vrms, V _{CC} = 5.0 V _{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	—	—	dBp
NPSR _X	Negative Power Supply Rejection, Transmit V _{FxI} + = 0 Vrms, V _{BB} = – 5.0 V _{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	—	—	dBp
PPSR _R	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V _{CC} = 5.0 V _{DC} + 100 mVrms) f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 KHZ	40	—	—	dBp
		40	—	—	dB
		36	—	—	dB
NPSR _R	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V _{BB} = – 5.0 V _{DC} + 100 mVrms) f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	40	—	—	dBp
		40	—	—	dB
		36	—	—	dB

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TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_{X1}^+ , measure individual image signals at VF_{R0} 4600 Hz – 7600 Hz 7600 Hz – 8400 Hz 8400 Hz – 100,000 Hz	–	–	– 32 – 40 – 32	dB

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STD _X or STD _R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel Level = 3 dBm0 = 0 dBm0 to – 30 dBm0 = – 40 dBm0 = – 55 dBm0 XMT RCV XMT RCV	 33 36 29 30 14 15	 – – – – – –	 – – – – – –	dBp
SFD _X	Single Frequency Distortion, Transmit	–	–	– 46	dB
SFD _R	Single Frequency Distortion, Receive	–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, $VF_{X1}^+ = -4$ dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz	–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT _{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level $f = 300$ Hz – 3400 Hz, $D_R =$ Steady PCM Mode	–	– 90	– 75	dB
CT _{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level $f = 300$ Hz – 3400 Hz, $VF_{X1} = 0$ V	–	– 90	– 70 (note 2)	dB

Notes : 1. Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_{X1}^+ .

ENCODING FORMAT AT D_X OUTPUT

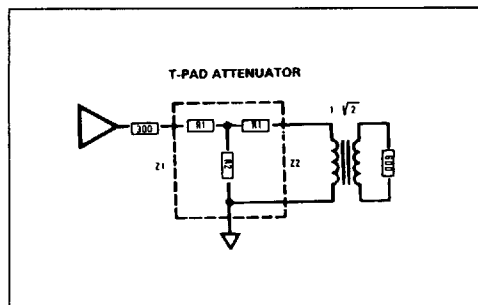
	A-Law (includes even bit inversion)	μ Law
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 1 0 1 0 1 0 1	0 1 1 1 1 1 1 1
	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATIONS INFORMATION

POWER SUPPLIES

While the pins of the ETC5050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector is useful.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin.



$$R1 = Z1 \left(\frac{N^2 + 1}{N^2 - 1} \right) - 2 \sqrt{Z1 \cdot Z2} \left(\frac{N}{N^2 - 1} \right)$$

$$R2 = 2 \sqrt{Z1 \cdot Z2} \left(\frac{N}{N^2 - 1} \right)$$

$$\text{Where : } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

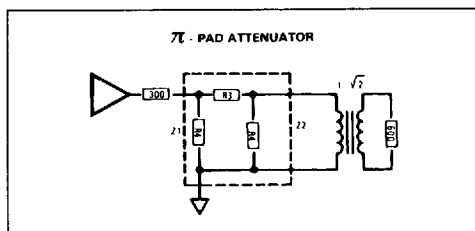
$$\text{and : } S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also : } Z = \sqrt{Z_{SC} \cdot Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination.

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$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}} \left(\frac{N^2 - 1}{N} \right)$$

$$R3 = Z1 \left(\frac{N^2 - 1}{N^2 - 2NS + 1} \right)$$

This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μ F supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} .

For best performance, the ground point of each/FILTER on a card should be connected to a common card. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μ F capacitors.

RECEIVE GAIN ADJUSTMENT

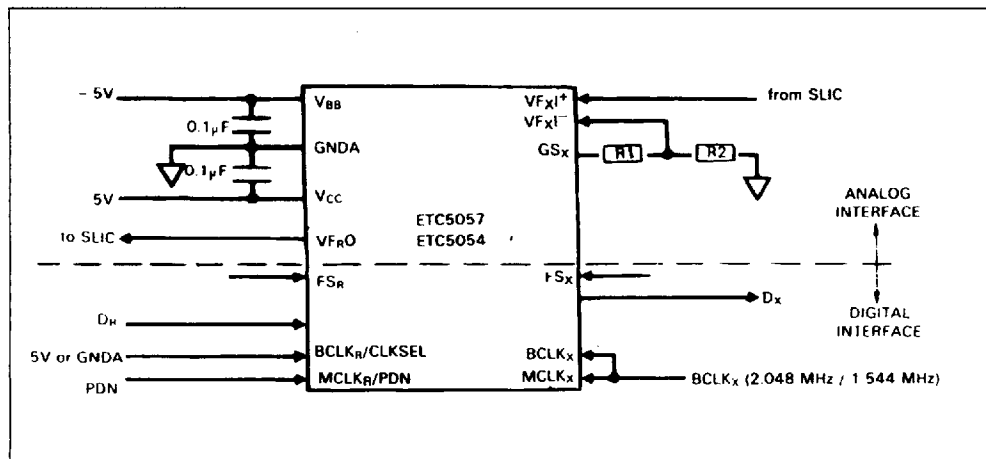
For applications where a ETC5050 family CODEC/filter receive output must drive a 600 Ω load, but a peak swing lower than ± 2.5 V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π -pad at the output. Table II lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

Table 2 : Attenuator Tables for $Z1 = Z2 = 300 \Omega$
(all values in Ω).

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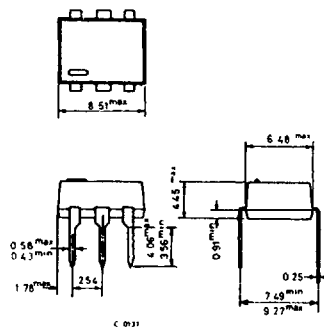
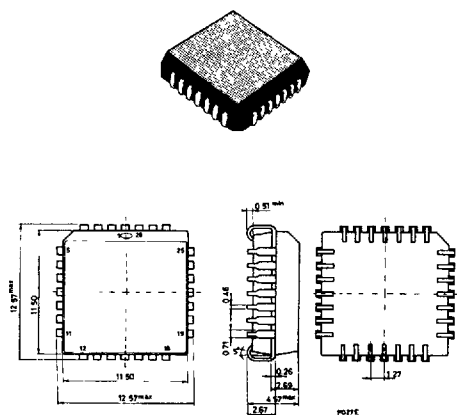
dB	R1	R2	R3	R4
0.1	1.7	26 k	3.5	52 k
0.2	3.5	13 k	6.9	26 k
0.3	5.2	8.7 k	10.4	17.4 k
0.4	6.9	6.5 k	13.8	13 k
0.5	8.5	5.2 k	17.3	10.5 k
0.6	10.4	4.4 k	21.3	8.7 k
0.7	12.1	3.7 k	24.2	7.5 k
0.8	13.8	3.3 k	27.7	6.5 k
0.9	15.5	2.9 k	31.1	5.8 k
1.0	17.3	2.6 k	34.6	5.2 k
2	34.4	1.3 k	70	2.6 k
3	51.3	850	107	1.8 k
4	68	650	144	1.3 k
5	84	494	183	1.1 k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17 k	386
20	246	61	1.5 k	366

Figure 5 : Typical Synchronous Application.

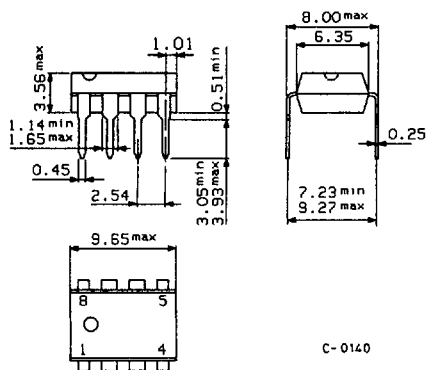
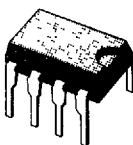


Note : 1. XMIT gain = $20 \cdot \log \left(\frac{R1 + R2}{R2} \right)$ (R1 + R2) > 10 kΩ.

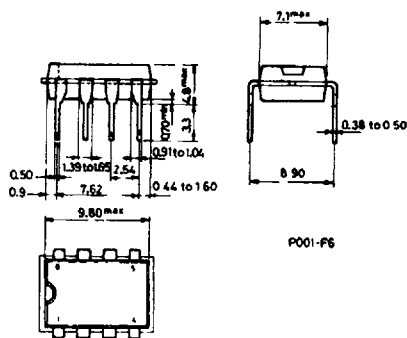
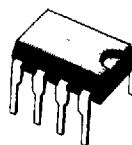
DIP-6



Minidip A Plastic

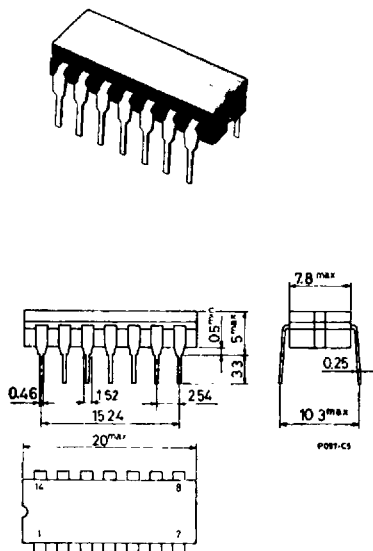


8 lead Plastic Minidip

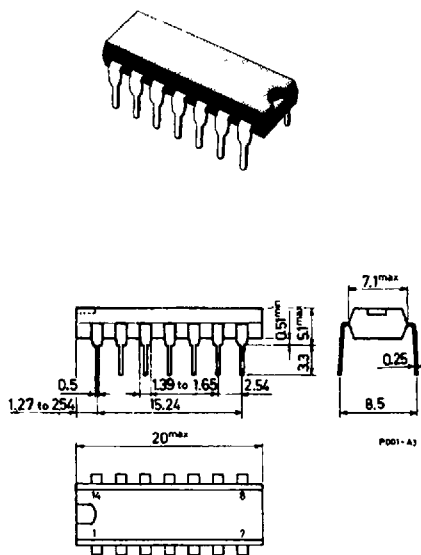


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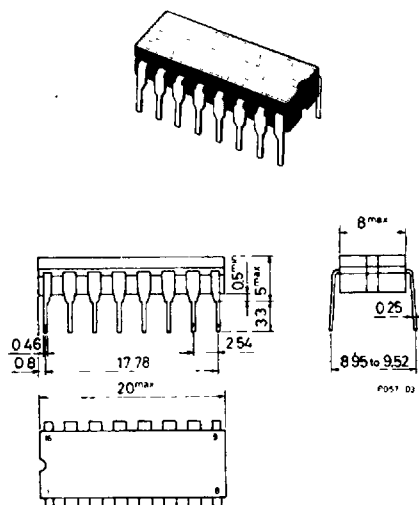
14 lead Ceramic Dip



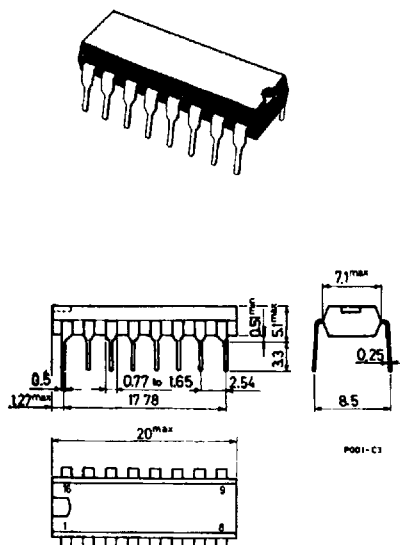
14 lead Plastic Dip



16 lead Ceramic Dip



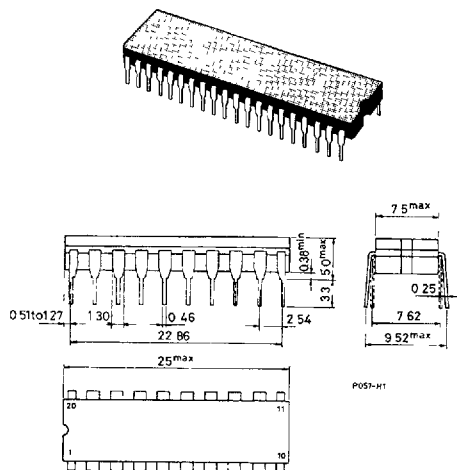
16 lead Plastic Dip (0.25)



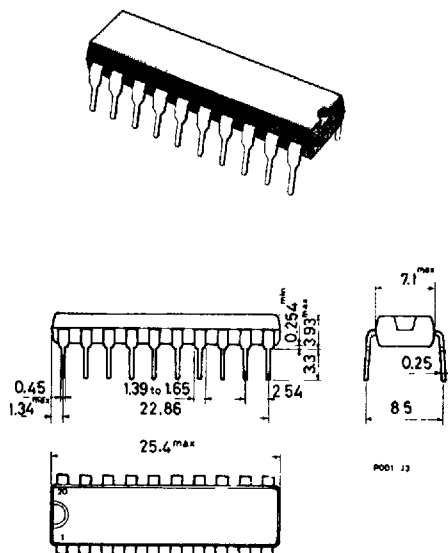
PACKAGES

S G S-THOMSON

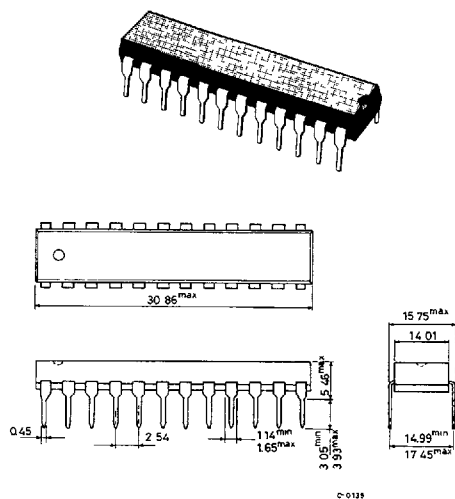
DIP-20 Ceramic



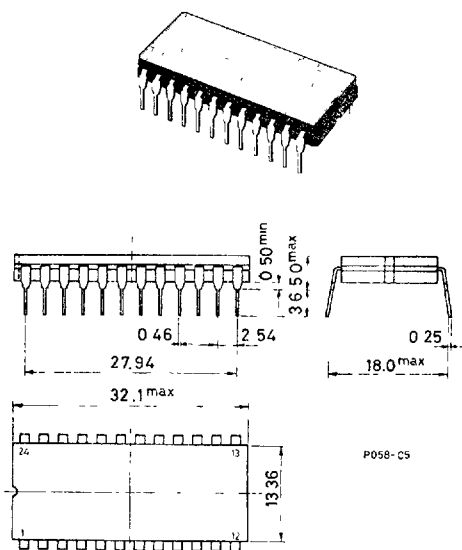
20 lead Plastic Dip (0.25)



DIP-24 Plastic

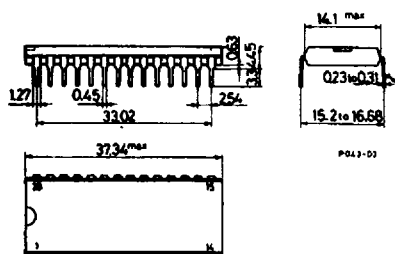
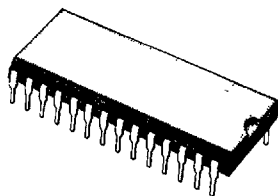


DIP-24 Ceramic (0.25)

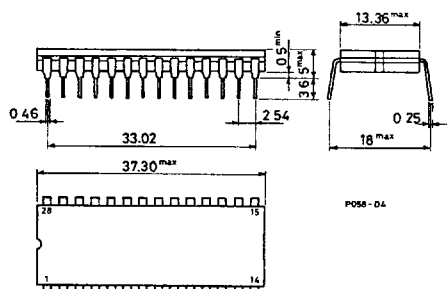
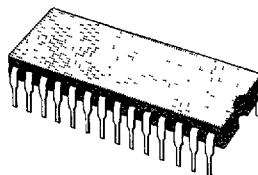


S G S-THOMSON

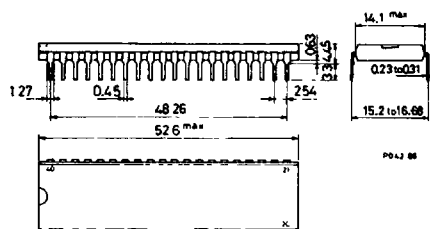
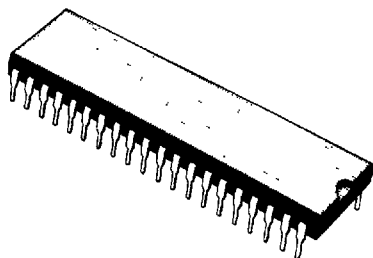
28 lead Plastic Dip



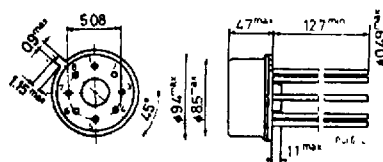
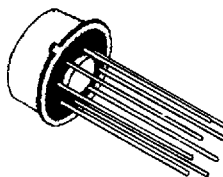
DIP-28 Ceramic (0.25)



40 lead Plastic Dip



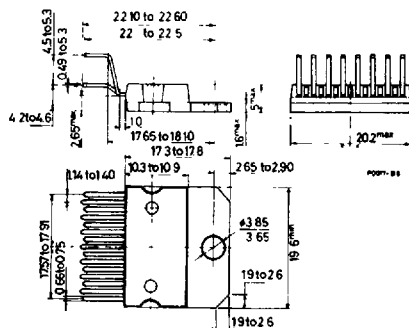
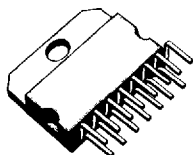
TO-99



PACKAGES

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MULTIWATT-15



FLEXIWATT-15

