EUROTECHNIQUE

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PRELIMINARY

ETC 9420/9421 AND ETC 9320/9321
SINGLE CHIP P²CMOS MICROCONTROLLERS

General description

The ETC 9420, C 9421, C 9320, C 9321 and ETC 9220, C 9221 fully static, single-chip P²CMOS microcontrollers are fully compatible with the COPS^{tm} family, fabricated using double-poly, silicon gate complementary MOS technology. These Controller Oriented processors are complete microcontrollers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of output architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation.

They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

- The ETC 9421 is identical to the ETC 9420, but with 19 I/O lines instead of 23.
- The ETC 9320/C 9321 and ETC 9220/C 9221 are the extended temperature range versions of ETC 9420/C 9421.
- The ETC 9320/C 9321 and ETC 9220/C 9221 are exact functional equivalents of the ETC 9420/C 9421.

Features

- Lowest power dissipation (50 µW typical).
- Power saving IDLE state and HALT mode.
- Powerful instruction set.
- 1K × 8 ROM, 64 × 4 RAM.
- 23 I/O lines (ETC 9420).
- True vectored interrupt, plus restart.
- 3-level subroutine stack.
- 4 µsec intruction time, plus software selectable oscillators.
- Single supply operation (2.4, 5.5 V).
- Programmable time base counter for real time processing.
- Internal binary counter register with MICROWIRE^{TM} serial 1/0 capability.
- General purpose and tri-state ^{TM} outputs.
- LSTTL/C MOS compatible.
- MICROBUS^{TM} compatible.
- Software/hardware compatible with other members of ET 9400 COP family.
- Extended temperature range devices ETC 9320/ETC 9321 and ETC 9220/ETC 9221.

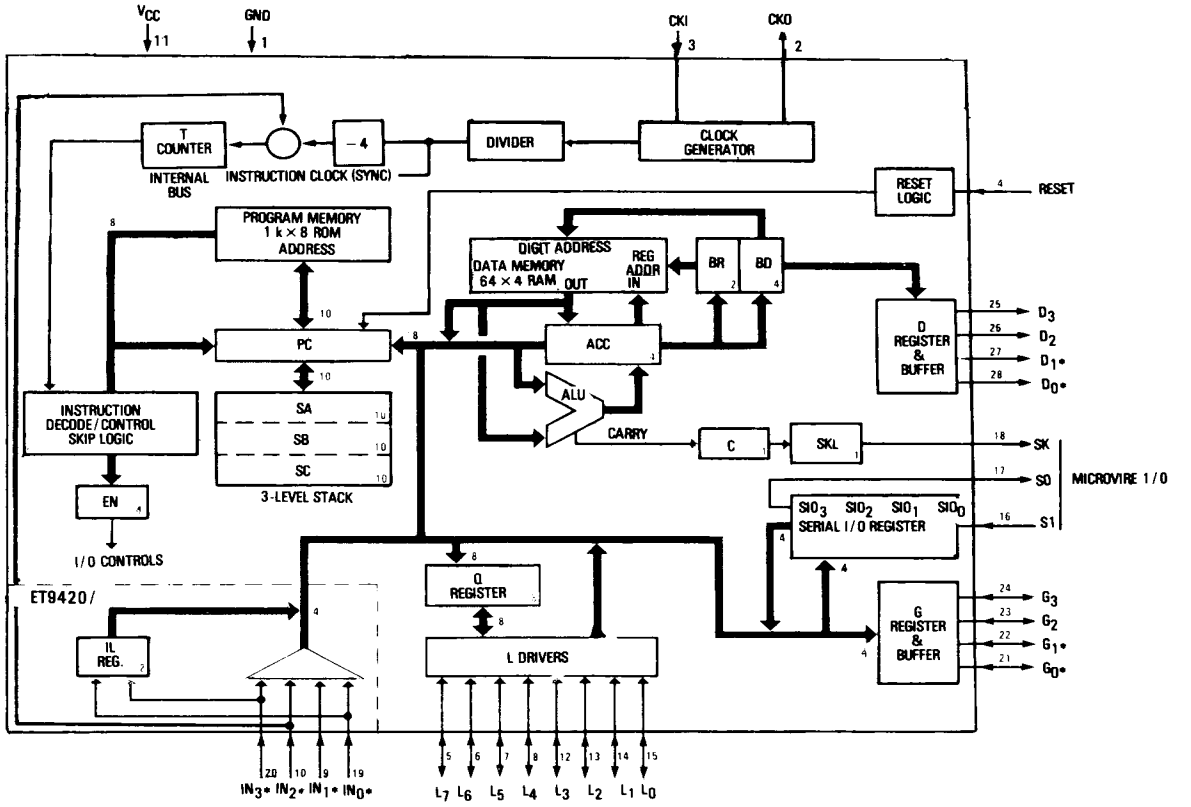


Figure 1. ETC 9420/9421 BLOCK DIAGRAM

Printed in France

Absolute Maximum Ratings

Voltage at any pin	− 0.3 V to V_{CC} + 0.3 V
Total Allowable Source current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0° C to + 70° C
Storage Temperature Range	− 65° C to + 150° C
Lead Temperature (soldering 10 seconds)	300° C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not insure when operating the device at absolute maximum ratings.

C ELECTRICAL CHARACTERISTICS (O° C to 70° C) unless otherwise stated)

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Supply Current	V_{CC} = 2.4 V Fin = 32 kHz (÷ 4 mode)		35	µA
(Note 1)	V_{CC} = 5.0 V Fin = 32 kHz (÷ 4)		80	µA
	V_{CC} = 5.0 V Fin = 500 kHz (÷ 8)		600	µA
	V_{CC} = 5.0 V Fin = 4 MhHz (÷16)		2500	µA
	V_{CC} = 5.0 V Fin = 4 MHz (÷32)		2500	µA
Idle State Current	V_{CC} = 2.4 V Fin = 32 kHz		15	µA
	V_{CC} = 5.0 V Fin = Max		250	µA
Halt Mode Current	V_{CC} = 5.0 V Fin = 0 kHz		12	µA
(Note 2)	V_{CC} = 2.4 V Fin = 0 kHz		5	µA
Input Voltage levels (RESET, CK)				
Logic High		0.9 V_{CC}		V
Logic Now			0.1 V_{CC}	V
All other inputs		0.7 V_{CC}		V
Logic High			0.2 V_{CC}	V
Pull up current	V_{CC} = 4.5, Vin = 0	30	330	µA
HZ input leakage		− 1	+ 1	µA
Output Voltage levels standard outputs				
LSTTL Operation	V_{CC} = 5.0 V ± 5 %			
Logic High	Ioh = − 25 µA	2.7		V
Logic Low	Iol = 400 µA		0.4	V
CMOS Operation				
Logic High	Ioh = − 10 µA	V_{CC} − 0.2		V
Logic Low	Iol = 10 µA		0.2	V
Output current levels sink	(except CKO)			
	V_{CC} = 4.5 V, Vout = V_{CC}	1.2		mA
	V_{CC} = 2.4 V, Vout = V_{CC}	0.2		mA
Source (standard option)	V_{CC} = 4.5 V, Vout = 0V	− 0.5		mA
	V_{CC} = 2.4 V, Vout = 0V	− 0.1		mA
Source (current option)	V_{CC} = 4.5 V, Vout = 0V	− 30	− 330	µA
	V_{CC} = 2.4 V, Vout = 0V	− 6	− 80	µA
CKO (at clock out current levels Sink	V_{CC} = 4.5 V, CKI = V_{CC}, Vout = V_{CC}			
Divide by 4		0.3		mA
Divide by 8	÷ 8	0.6		mA
Divide by 16 or 32	(full size buffer)	1.2		mA
Source	V_{CC} = 4.5 V, CKI = 0, Vout = 0			
Divide by 4		− 0.3		mA
Divide by 8	÷ 8	− 0.6		mA
Divide by 16 or 32	(full size buffer)	− 1.2		mA

Maximum Allowable loading on CKO (as HALT)			100	pF
Maximum Current needed to over-ride HALT				
To continue	V_{CC} = 4.5 V, Vin = 0.2 V_{CC}		0.5	mA
to halt	V_{CC} = 4.5 V, Vin = 0.7 V_{CC}		1.5	mA
TRI-STATE (R) or open drain Leakage current		− 2	+ 2	µA

Note 1 : Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V^{CC} with 20 K resistors.

Note 2 : The HALT mode will stop CKI from oscillating in the RC and cyrstal configurations. When forcing HALT mode, current is only needed for a short time (approx. 200 ns) to flip the HALT flip flop.

* AC ELECTRICAL CHARACTERISTICS (0° C T to 7O° C unless otherwise stated)

Parameter	Conditions	Min	Max	Units
Instruction cylce Time	V_{CC} > 4.5 V	4	DC	µS
	V_{CC} > 2.4 V	16	DC	µS
Operating CKI Frequency	÷ 4 mode	DC	1.0	MHz
	÷ 8 mode V_{CC} > 4.5 V	DC	2.0	MHz
	÷16 mode	DC	4.0	MHz
	÷32 mode	DC	4.0	MHz
	÷ 4 mode	DC	250	kHz
	÷ 8 mode V_{CC} > 2.4 V	DC	500	kHz
	÷16 mode	DC	1.0	MHz
	÷32 mode	DC	1.0	MHz
Instruction cycle Time − CKI (RC)	R = 30 k ± 5 %, V_{CC} = 5 V C = 82 pF ± 5 % (÷ 4 Mode)	8	16	µS
CKI duty cycle		40	60	%
Dual clock option				
Instruction cycle	V_{CC} > 4.5 V	4	DC	µS
	V_{CC} > 2.4 V	16	DC	µS
Operating Do frequency	÷ 4 mode V_{CC} > 4.5 V	DC	1	MHz
	÷ 8 mode	DC	2	MHz
	÷ 4 mode V_{CC} > 2.4 V	DC	250	kHz
	÷ 8 mode	DC	500	kHz
INPUTS (fig. 3)	G Inputs	(tc/4)+ 0.7		µS
	SI Input	0.3		µS
	All others	1.7		µS
	V_{CC} > 4.5 V	0.25		µS
	V_{CC} > 2.4 V	1.0		µS
Input capacitane			7	pF
OUTPUT				
PROGRAMMATION DELAY	Vout = 1.5 V, CL = 100 pF, RL = 5K			
t (pd1) t (pd0)	V_{CC} > 4.5 V		1.0	µS
t (pd1) t (pd0)	V_{CC} > 2.4 V		4.0	µS
MICROBUS$_{TM}$ TIMING	C_L = 50 pF, V_{CC} = 5 V ± 5 %			
A Read operation (fig. 4)				
Chip Select Stable before RD - t_{CSR}		50		ns
Chip Select Hold time for RD - t_{CSR}		5		ns
RD Pulse Width - t_{RR}		300		ns
Data Delay from RD-t_{RD}			250	ns
RD to Data Floating-t_{DF}			200	ns
B Write Operation (fig. 5)				
Chip Select Stable before WR - t_{CSW}		20		ns
Chip Select Hold Time for WR - t_{WCS}		20		ns
WR' Pulse Width - t_W		300		ns
Data Set up Time for WR - t_{DW}		200		ns
Data Hold Time for WR - t_{WD}		40		ns
INTR Transition time from WR - t_{WI}			700	ns

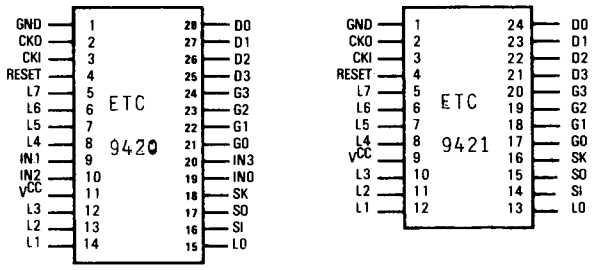


Figure 2. Connection Diagrams

Pin Description

L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_1	3 general purpose outputs
D_0	General purpose output or oscillator input
IN_3-IN_0L4 général purpose inputs (ETC 9420 only)	
SI	Serial INPUT
SO	Serial output
SK	Logic-controlled clock or general purpose output
CKI	System oscillator input
CKO	System oscillator output (or general purpose Input or Halt I/O Port
RESET	System reset input
V_{CC}	Power supply
GND	Ground

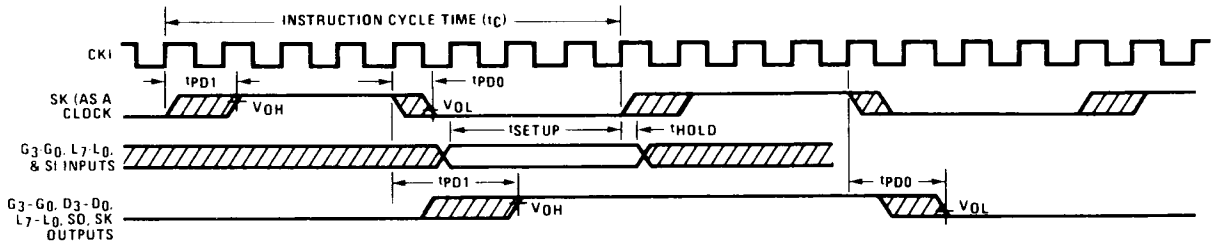


Figure 3. Input/Output Timing Diagrams (Divide-by 16 Mode)

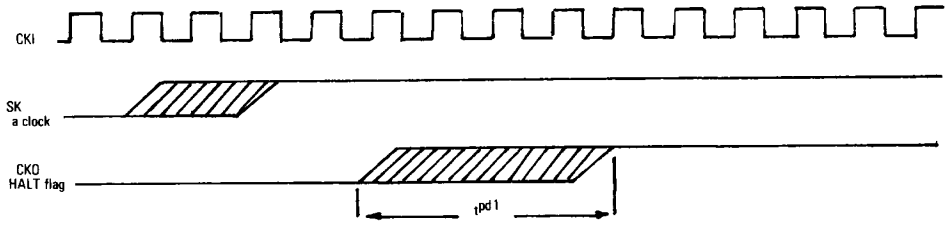


Figure 3A. CKO Output timing (Crystal divided EY 16 Mole)

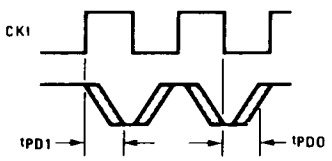
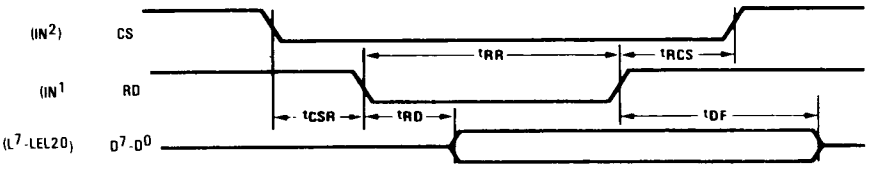
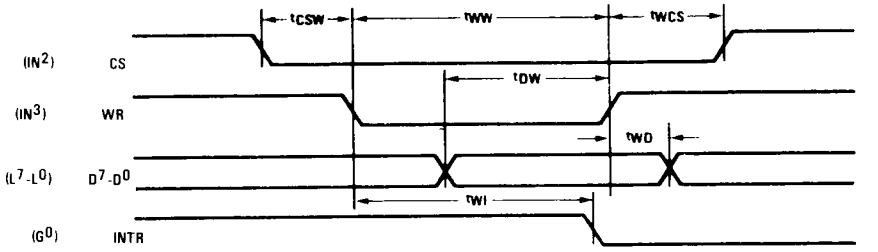


Figure 3B. CKO Output Timing



MICROBUS$_{TM}$ Write Operation Timing



MICROBUS$_{TM}$ Read Operation Timing

Functional description

To ease the reading of this description, only ETC 9420 and/or ETC 9421 are referenced. However, all such references apply equally to ETC 9320/92210 and/or ETC 9321/9221, respectively.

A block diagram of the ETC 9420 is given in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. When a bit is reset, it is a logic "1" when it is reset, it is a logic "0".

Program memory

Program memory consists of a 1024 byte ROM. As can be seen by an examination of the ETC 9420C/9421C instruction set, these words may be program instructions, program data, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be though of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a 10-bit PC register. Its binary value selects one of the 1024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is leaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are complemented by three 10-bit binary subroutine save registers SA, SB and SC, providing a last in, first out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded, and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consits of a 256-bit RAM, organized as 4 data registers of 16 4-bit digits. RAM addressing is implemented by a 6-bit **B-register** whose upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports and loaded into or from the 8 bit T time. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data directly to the D outputs.

Internal Logic

The internal logic of the ETC 9420/ETC 9421 is designed to insure fully static operation of the device.

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load 4 bits of the 8-bit Q latch data, to load 4 bits of the 8 bits timer and to perform data exchanges with the SIO register.

A 4-bit adder performs the artihmetic and logic functions of the ETC 9420/ETC 9421 storing its results in A. It also outputs the carry information to a 1-bit carry register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description below).

The 8-bit T counter is a binary up counter, which can be loaded to and from M and A. The input to this counter is hardware selectable (option 31) from 2 sources : the first coming from a divide by 4 prescalers (from instruction cycle frequency) thus providing a 10-bit time base counter . The second coming from IN_2 input, changing the T counter into an 8-bit external event counter. In this mode, a low going pulse ("1" to "0") of at least 2 instruction cycles wide will increment the counter.

When the counter overflows, an overflow flag will be set (see SKT instruction below and an interrupt signal will be sent to the processor. The T counter is cleared on reset.

Four **general-purpose inputs,** IN_3-IN_4, are provided ; IN_1, IN_2 and IN_3 may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS^{TM} applications (ETC 9420 only).

The **D register** provides 4 general purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode, D-register bit 0 controls the clock selection (see dual oscillator below).

The **G register** contents are outputs to 4 general-purpose bidirectional I/O ports. G^0 may be mask-programmed as an output for MICROBUS^{TM} applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS™ option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurence of a write strobe from the host CPU.

The **8 L drivers,** when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS™ option allows L I/O port data to be latched into the Q register.

The **D register** provides 4 general purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending upon the contents of the EN register (See EN register description below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. With SIO functioning as a serial shift register-ETC 9420/9421 is MICROWIRE™ compatible.

The **XAS instruction** copies C into the SKL Latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN_0 set, SIO is as asynchronous binary counter, DECREMENTING its value by one upon each low going pulse ("1" to "0") occuring on the SI input. Each pulse must be at least 2 (two) instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each instruction cycle time (See 4 below). The SK ouptut becomes a logic controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediatly following an interrupt, EN_1 is reset to disable further interrupts (ETC 9420 only).
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set binary counter option selected), SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected, disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

Table 1. Enable Register modes - Bits EN_0 and EN_3

EN_0	EN_3	SIO	SI	SO	SK after XAS
0	0	Shift Register	Input to shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary counter	Input to Counter	0	SK = SKL
1	1	Binary counter	Input to Counter	1	SK = SLK

Interrupt (ETC 9420/9320 only)

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupt.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 SA SB SC). Any previous contents of SC are lost. The program counter is set to hex address OF (the last word of page 3) and EN_1 reset.

b. An interrupt will be acknowledged only after the following conditions are met :

   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occures on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. ALl successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgment of an interrupt, the skip logic status is saved and later restored upon the execution of a subsequent RET instruction. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address OFF. At the end of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Since, as explained above, it is the RET instruction which enables the previously saved status of the skip logic, **subroutines should not be nested within the interrupt servicing routine** since their RET instruction will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

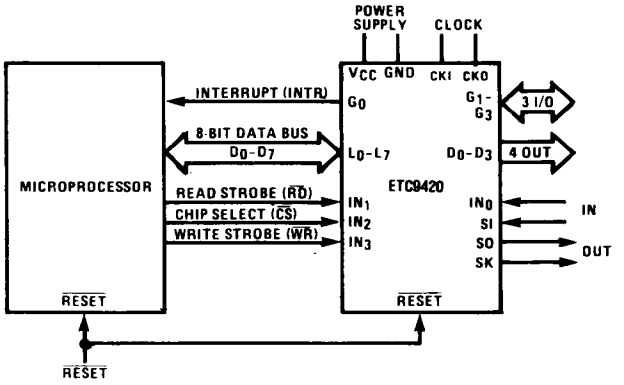
d. The first instruction of the interrupt routine at hex address OFF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

Microbus™ Compatible

The ETC 9420 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from to a host microprocessor (uP). IN_1 IN_2 and IN_3 general purposes input become **MICROBUS™ COMPATIBLE** read-strobe, chip-select, and write-strobe lines, respectively. IN_1 become RD – a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the uP. IN_2 becomes CS – a logic "0" on this line selects the 9420 as the uP peripheral device by enabling the operation of the RD and WR lines and allows for the selection of one of several peripheral components. IN_3 becomes WR – a logic "0" on this line will write bus data from the L ports to the Q latches for input to the ETC 9420. G_0 becomes INTR, a "ready" output, reset by a write pulse from the uP on the WR line, providing the "handshaking" capability neccessary for asynchronous data transfer between the host CPU and the ETC 9420.

The option has been designed for compatibility with MICROBUS™ a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS™ National Publication). The functioning and timing relationships between the ETC 9420 signal lines affected by this option are as specified for the MICROBUS™ interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figure 4 and 5). Connection of the ETC 9420 to the MICROBUS™ is shown in figure 6.

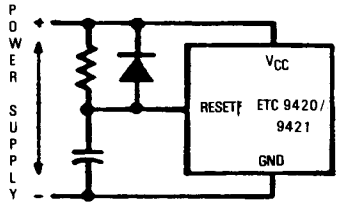


MICROBUS™ Option Interconnect

Initialization

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 11 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in Figure 5 must be connected to the RESET pin. The RESET pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the RESET input, providing it stays low for at least three instruction cycle times.

NOTE : if CKI clock is less than 32 kHz, the internal reset logic (option = 29 = 1) must be disabled.



RC > 5 x Power Supply Rise Time and RC > 100 x CKI period

Power-Up Clear Circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL and G registers are cleared. The SK ouptut is enabled as a SYNC output, providing a pulse each instruction cycle time. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

Oscillator

There are 4 basic clock oscillator configurations available, as shown in Figure ?

a. **Crystal controlled oscillator**
CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 32, 16, 8 or 4 optionnaly.

b. **External oscillator**
CKI is configurated as a LSTTL compatible input accepting an external clock signal. The external frequency is divided bu 32, 16, 8 or 4 optionaly to give the instruction cycle time. CKO is the HALT I/O port, or a general purpose input.

c. **RC controlled oscillator**
CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillator frequency divided by 4. CKO is the HALT I/O port, or a general purpose input.

d. **Dual oscillator**
By selecting the dual clock option, pin DO is now a clock input. The user may connect a 32 kHz watch crystal to CKI and CKO and up to **1 MHz** clock to DO (R/C or external). The user may then software select between the DO oscillator for faster processing (DO = 1) and the crystal for minimum current drain (DO = 0). **The time base counter runs off the CKI oscillator, even when the user selects** DO as the clock. Thus a real time clock can be maintained by the IT instruction even when running off the RC oscillator.

NOTE : dual clock is not allowed, when using divide by 32 options.

Halt mode

The ETC 9420/9421 is a FULLY STATIC circuit ; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may be also halted by the HALT instruction (with CKO open) or by forcing CKO high when it is used as an HALT/I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The HALT mode is the minimum power dissipation state.

The HALT mode has slight differences depending upon the type of oscillator used, and CKO option selected.

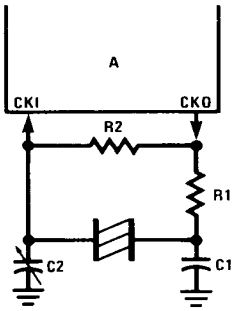
a. **One pin oscillator (RC or EXT) on CKI, CKO as HALT I/O port**
The HALT mode may be entered into by either program control (HALT instruction) or by forcing CKO to a logic "1" state.
The circuit may be awakened by one of two different methods :

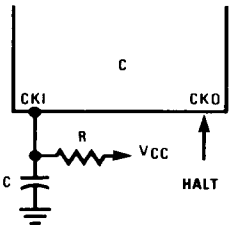
1. Continue function – by forcing CKO to a logic "0", the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
2. Restart – by forcing the RESET pin to a logic "0" (see initialization).

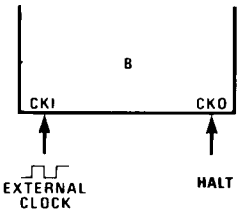
b. **One pin oscillator (RC or EXT) on CKI**
CKO as a general purpose input – software halt feature is still available, but the hardware halt and continue features associated with the CKO pin are not. Restart can only be achieved by resetting the circuit. CKO can be configured either a high-Z or a pull-up load input.

c. **Two-pin oscillator – (crystal or resonator)**
The HALT mode may be entered into by program control (HALT instruction) which forces the CKO input to a logic "1" state. The circuit can be awakened only by the RESET function (see initialization).

d. **DO as clock input for Dual Clock Mode**
DO input is configured as a schmitt trigger input allowing the customer to use either an RC or external oscillator. All of the features stated in part I apply directly to this option. The software halt instruction can be executed from either clock source, DO or CKI and each case, the HALT mode stops BOTH clock sources from oscillating.







Crystal or resonator

Crystal value	Component Values			
	R1	R2	C1 (pF)	C2 (pF)
32 kHz	220 K	20 M	30	5-36
455 kHz	4 K	10 M	80	40
2.096 MHz	1 K	10 M	30	6-36
4.0 MHz	1 K	1 M	56	6-36

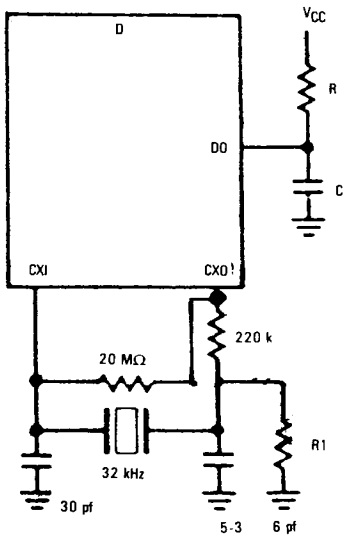
These value are for indication only.
Actual value may vary according to the crystal characterisation.

R/C controlled Oscillator

(V_{CC} > 4.5 V)

R	C	Cycle time
15 K	82 pF	4 to 9 uS
30 K	82 pF	8 to 16 uS
60 K	100 pF	16 to 32 uS

Note : R must be > 15 K, C < 300 PF



DUAL CLOCK

CKO pin options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network.

When another oscillator is selected, CKO can be selected as :

a. a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

b. the HALT I/O port (see HALT mode above).

ETC 9421

If the ETC 9420 is bonded in a 24 pin device, it becomes the ETC 9421, illustrated in Figure 1. ETC 9420/9421 connection diagram.

NOTE : That the ETC 9421 does not contain the 4 general purpose IN inputs (IN_3 - IN_0). Use of this option precludes, of course, use of the IN options, interrupt feature, usage of T as external event counter and the MICROBUS option which uses IN_1 - IN_3. All other options are available for the ETC 9421.

Power dissipation

The lowest drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. For example, à 500 kHz crystal input will typically draw 100 uA more than a squarewave input.

I/O OPTIONS

The ETC 9420 outputs have the following optional configurations, illustrated in Figure :

a. Standard (Push-Pull) - An N channel device to ground in conjunction with a P channel device to V_{CC}, compatible with C MOS and LSTTL.

b. Low Current - This is the same configuration as a) above except that the sourcing current is much less.

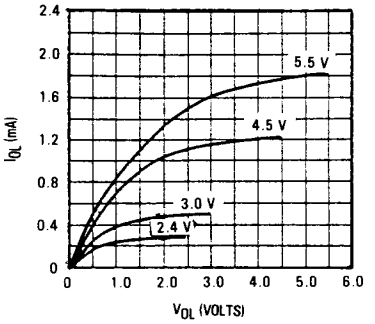
c. Open drain - An N channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE (R) L Outptut - A C MOS output buffer which may be disabled by program control.

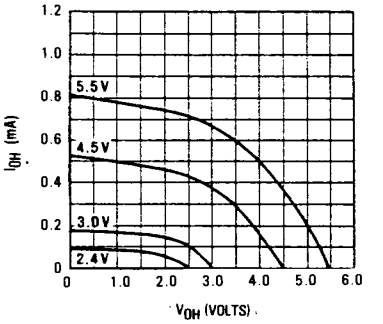
e. Low-Current TRI-STATE (R) L Output – This is the same as d) above except that the sourcing current is much less.

f. Open-Drain TRI-STATE (R) L Output - This has the N channel device to ground only.

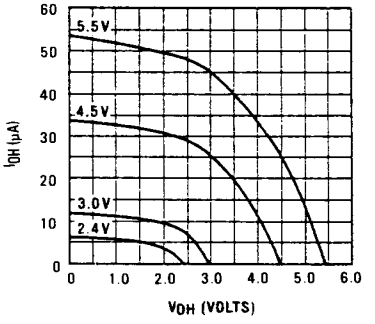
Minimum Sink Current



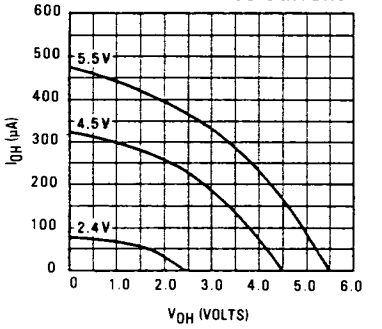
Standar
Minimum Source Current



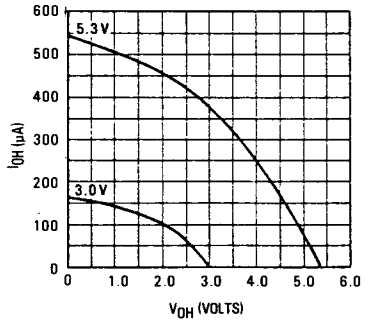
Low Current Option
Minimum Source Current



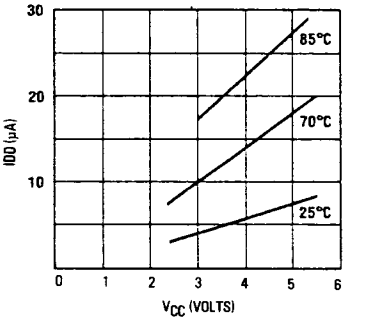
COP410C/COP411C
Low Current Option
Maximum Source Current



COP310C/COP311C
Low Current Option
Maximum Source Current



Maximum Quiescent Current



ETC 9420/9421 and ETC 9320/9321 Instruction Set

Table 2 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the ETC 9420/ETC 9421 instruction set.

Table 2. ETC 9420/9421 Instruction Set Table Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
IL	Two 1 bit Latches associated with the IN_3 or IN_0 Inputs
IN	4-bit Input Port
IP	8-bit Bidirectional ROM Address&Data Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
P	2-bit ROM Address Port
PC	10-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	10-bit Subroutine Save Register A
SB	10-bit Subroutine Save Register B
SC	10-bit Subroutine Save Register C
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output
T	8-bit Binary Counter Register

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
r	2-bit Operand Field, 0-3 binary (RAM Register Select)
a	10-bit Operand Field, 0-1023 binary (ROM Address)
y	4-bit Operand Field, 0-15 binary (Immediate Data)
RAM (s)	Contents of RAM location addressed by s
ROM (s)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
	Replaces
	Is exchanged with
.=	Is equal to
A/	The ones complement of A
+	Exclusive-OR
:	Range of values

Table 2. ETC 9420/9421 Instruction Set Table

Mnemonic	Operand	Hex Code	Machine Language code (binary)	Data flow	Skip conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33 3F	00110011 00111111	A $T_{7.4}$ RAM (B) $T_{3.0}$	None	Copy A, RAM to T
CTMA		33 2F	00110011 00101111	$T_{7.4}$ RAM (B) $T_{3.0}$ A	None	Copy T to RAM, A
CAMQ		33 3C	00110011 00111100	A $Q_{7.4}$ RAM (B) $Q_{3.0}$	None	Copy A RAM to Q
CQMA		33 2C	00110011 00101100	$Q_{7.4}$ RAM (B) $Q_{3.0}$ A	None	Copy Q to RAM A
LD	r	-5	00r0101	RAM (B) A Br + r Br	None None	Load RAM into A Exclusive OR Br with r
LDD	rd	23	00100011	RAM (r, d) A		Load A with RAM pointed to directly by r, d
LQID		BF	10111111	ROM ($PC_{9.8}$A,M) Q SB SC	None	Load Q indirect (Note 3)
RMB	0 1 2 3	4C 45 42 43	01001100 01000101 01000010 01000011	0 RAM $(B)_0$ 0 RAM $(B)_1$ 0 RAM $(B)_2$ 0 RAM $(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	01001101 01000111 01000110 01001011	1 RAM $(B)_0$ 1 RAM $(B)_1$ 1 RAM $(B)_2$ 1 RAM $(B)_3$	None	Set RAM Bit
STII	y	7-	1111 y	RAM (B) Bd + 1 Bd	None	Store Memory Immediate and Increment Bd
X	r	-6	00r0110	RAM (B) A Br + r Br	None	Exchange RAM with A Exclusive or Br with r.
XAD	r,d	23 --	00100011 10 r d	RAM (r,d) A	None	Exchange A with RAM pointed to directly by r, d
XDS	r	-7	00 r 0111	RAM (B) A Bd − 1 Bd Br + r Br	Bd decrements	Exchange RAM with A past 0 and Decrement Bd Exclusive OR Br with r
XIS	r	-4	00 r 0100	RAM (B) A Bd + 1 Bd Br + r Br	Bd increments past 15 Exclusive OR Br with r	Exchange RAM with A and increment Bd
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	01010000	A Bd	None	Copy A to Bd
CBA		4E	01001110	Bd A	None	Copy Bd to A
LBI	r,d	-- OR 33 -- (any d)	00 r (d − 1) 00110011 10 r d	r,d B	Skip until not a LBI	Load B immediate with r,d (Note 6)
LEI	y	33 6-	00110011 0110 y	y EN	None	Load EN immediate (Note 7)
XABR		12	0001 0010	A Br (0,0 A^3 A^2)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC	•	20	00100000	C = "1"	Skip of C is true	
SKE		21	00100001	A = RAM (B)	Skip if A Equals RAM	
SKGZ		33	00110011	$G_{3.0} = 0$	Skip of G is 0 (all 4 bits)	
SKGBZ		33	00110011	1st byte		Skip if G bit is Zero
	0	01	00000001	$G_0 = 0$		
	1	11	00010001	2nd byte	$G_1 = 0$	
	2	03	00000011	$G_2 = 0$		
	3	13	00010011	$G_3 = 0$		
SKMBZ	0	01	00000001	RAM $(B)_0 = 0$	Skip if RAM bit is zero	
	1	11	00010001	RAM $(B)_1 = 0$		
	2	03	00000011	RAM $(B)_2 = 0$		
	3	13	00010011	RAM $(B)_3 = 01$		
SKT		41	01000001	A time base	Skip on Timer counter carry has occured since last test	(Note 3)

Table 2. ETC 9420/9421 Instruction Set Table

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	00110011 00101010	G A	None	Input G Ports to A
ININ		33 28	00110011 00101000	IN A	None	Input IN Inputs to A (Note 2)
INIL		33	00110011	IL_3, "CKO", "0", IL_0 n	None	Input IL latches to A
		29	00101001	IL_0 A		(Notes 2 and 3)
INL		33 2E	00110011 00101110	$L_{7.4}$ RAM (B) $L_{3.0}$ A	None	Input L Ports to RAM, A
OBD		33 3E	00110011 00111110	Bd D	None	Output Bd to D outputs
OGI	y	33 5-	00110011 0101 y	y G	None	Output to G Ports Immediate
OMG		33 3A	00110011 00111010	RAM (B) G	None	Output RAM to G Ports
XAS		4F	01001111	A SIO, C SK	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicity defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ Instruction is not available on the 24 pin ETC 9421 since this device does not contain the IN inputs.

Note 3 : For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4 : The JP Instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3 JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus I e.g. to load the lower four bits of B (Bd) with the value 9 100_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (see Functional Description, EN Register).

Table 3. ETC 9420/9421 Instruction Set Table (mode 1)

ARITHMETIC INSTRUCTIONS						
ASC		30	00110000	A + C RAM (B) A Carry C	Carry	Add with Carry, Skip on Carry
ADD		31	00110001	A + RAM (B) A	None	Add A to RAM
ADT		4A	01001010	A + 10_{10} A	None	Add Ten to A
AISC	y	5-	0101 y	A + y A	Carry	Add Immediate skip on carry (y ≠ 0)
CASC		10	00010000	A = RAM (B) + C A Carry C	Carry	Complement and Add with carry, skip on carry
CLRA		00	00000000	0 to A	None	Clear A
COMP		40	01000000	A A	None	Ones complement of A to A
NOP		44	01000100	None	None	No operation
RC		32	00110010	"0" C	None	Reset C
SC		22	00100010	"1" C	None	Set C
XOR		02	00000010	A + RAM (B) A	None	Exclusive OR A with RAM

TRANSFER OF CONTROL INSTRUCTIONS

JID		FF	1 1 1 1 1 1 1 1	ROM ($PC_{9,8}$ A, M) $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6-	0 1 1 0 0 0 $a_{9,8}$	a PC	None	Jump
JP	a	--	$a_{7,0}$ (pages 2, 3 only) $a_{6,0}$ all other pages	a $PC_{6,0}$ a $PC_{5,0}$	None	Jump within page (Note 4)
JSRP	a	--	1 0 $a_{5,0}$	PC + 1 SA SB SC 0010 $PC_{9,6}$ a $PC_{5,0}$	None	Jump to subroutine PAGE (Note 5)
JSR	a	6- --	0 1 1 0 1 0 $a_{9,8}$ $a_{7,0}$	PC + 1 SA SB SC SC	None	Jump to subroutine
RET		48	0 1 0 0 1 0 0 0 5	SC SB SA PC	None	Return from subroutine
RETSK		49	0 1 0 0 1 0 0 1	SC SB SA PC	Always skip on return	Return from subroutine then skip
HALT		33 38	0 0 1 1 0 0 1 1 0 0 1 1 1 0 0 0		None	Halt processor
IT		33 39	0 0 1 1 0 0 1 1 0 0 1 1 1 0 0 1	PC PC		Idle till timer overflows, then continue

Description of selected instruction

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writting ETC 9420/9421 programs.

XAS instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register data. An XAS instruction will also affect the SK output, providing a logic controlled clock. An XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by 10-bit word, $PC_{9,8}$, A, M, PC_9 and PC_8 are not affected by this instruction.

Note that JID requires two instruction cycles to execute.

INIL instruction

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see Figure 8) and CKO into A. The IL_3 and the IL_0 latches are set if a low-going pulse ("1" to "0") has occured on the IN_3 and the IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A_3 and A_0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A_2. If CKO has not been so programmed, a "1" will be placed in A_2. A "0" is always placed in A_1 upon the execution of an INIL. The general purpose inputs IN_3-IN_0 are input to A upon execution of an ININ instruction. (See table 2, ININ instruction). INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read convently by an ININ instruction.

IL latches are cleared on reset. IL latched are not available on the ETC 9421.

LQID instruction

LQID (Load Q indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC_9, PC_8, A, M. LQID can be used for table look-up or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 SA SB SC) and replaces the least significant 8-bits of PC as follow A PC_{7-4} RAM (B) PC_{3-0} leaving PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next the stack is "popped" (SC SB SA PC) restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB SC the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB SC).

Note that LQID takes two instruction cycle times to execute.

SKT instruction

The SKT (Skip on Timer) instruction tests the state of the T counter (see internal logic, above) overflow latch, executing the next program instruction if the latch is not set. If the latch has been set since the last test, the next program instruction is skipped and the latch is reset. The features associated with the instruction allow the processor to generate its own time base for real time processing, rather than relying on an external input signal.

IT instruction

The IT (Idle Till Timer) instruction halts the processor and puts it in an idle state until the time base counter overflows. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped.

The inputs have the following options :

1. Input with on chip load device to V_{CC}.

2. HI-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available : Select the low-current output option.

Now, by setting the output registers to a logic "1" level, the p-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

All output drivers use one or more of three common devices numbered 1 to 3 minimum and maximum current (I out and V out) curves are given in Figure 8 for each of these devices to allow the designer to effectively use these I/o configurations.

OPTION LIST

The ETC 9420/9320 mask programmable options are assigned numbers which correspond with the ETC 9420 pins.

The following is a list of the ETC 9420 options. When specifying an ETC 9421 chip, options 9, 10, 19 and 20 must all be set to zero.

The options are programmed at the same time as the ROM pattern to provide the user with the flexibility to interface to various I/O components using little or no external circuitry.

Option 01 : Ground
Not an option

Option 02 : CKO
00 : Clock generator output to XTAL
01 : Halt I/O port
02 : General purpose input. load device to V_{CC}
03 : General purpose input HI-Z

Option 03 : CKI
00 : XTAL % 4
01 : XTAL % 8
02 : XTAL % 16
03 : XTAL % 32
04 : RC % 4
05 : EXT % 4
06 : EXT % 8
07 : EXT % 16
08 : EXT % 32
09 : XTAL % 8 FULL SIZE BUFFER

Option 04 : Reset
00 : Load device to V_{CC}
01 : HI-Z input

Option 05, 06, 07, 08 : L7, L6, L5, L4 drivers
00 : Standard tri-state push-pull output
01 : Low-current
02 : Open-drain

Option 09, 10 : IN_1 and IN_2 inputs
00 : Load device to V_{CC}
01 : HI-Z input

Option 11 : V_{CC}
Not an option

Option 12, 13, 14, 15 : L3, L2, L1, L0 drivers
00 : Standard tri-state push-pull output
01 : Low-current
02 : Open-drain

Option 16 : SI input
00 : Load device to V_{CC}
01 : Hi-Z input

Option 17, 18 : SO and SK drivers
00 : Standard push-pull
01 : Low-current
02 : Open-drain

Option 19, 20 : IN_0 and IN_3 inputs
00 : Load device to V_{CC}
01 : HI-Z input

Option 21, 22, 23, 24 : GO, G1, G2, G3 I/O port
00 : Standard push-pull
01 : Low-current
02 : Open-drain

Option 25, 26, 27, 28 : D3, D2, D1, D0 output
00 : Standard push-pull
01 : Low-current
02 : Open-drain

Option 29 : Internal initialization logic
00 : Normal operation
01 : No INI, INIT logic (must be selected if CKI is less than 32 KHz)

Option 30 : Clock mode
00 : Normal operation
01 : Dual clock do RC OSC input
02 : Dual clock do Schmitttrigger ext, clock input

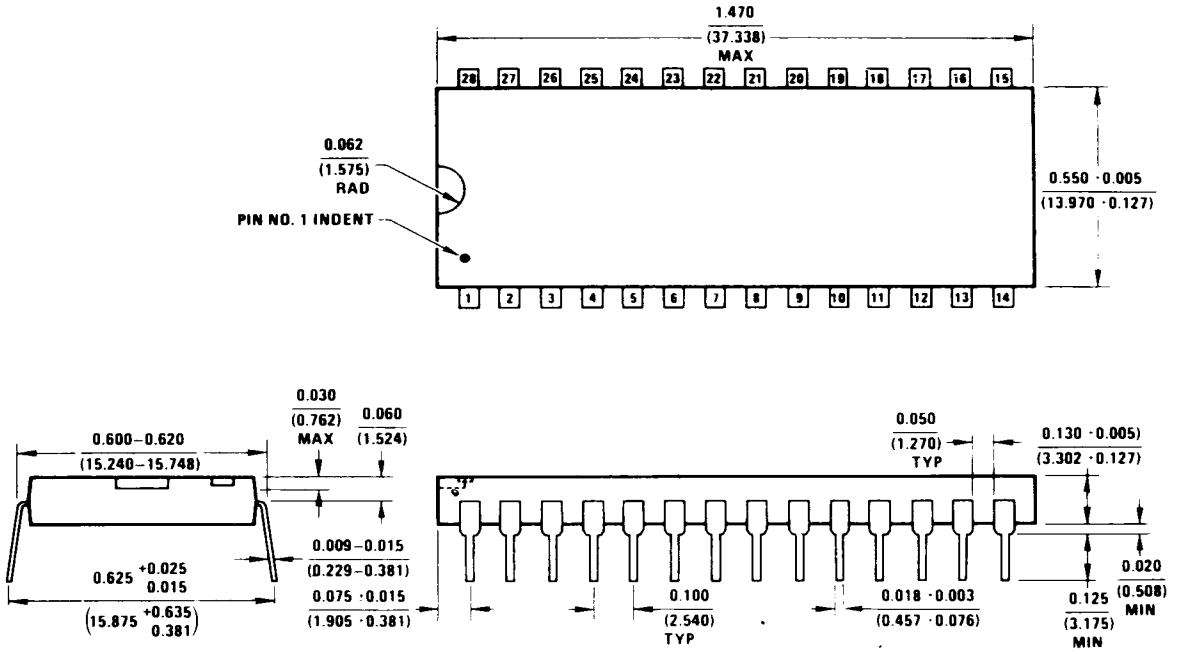
Option 31 : Timer
00 : Time-base counter
01 : Ext. event counter

Option 32 : Function
00 : Normal operation
01 : Microbus

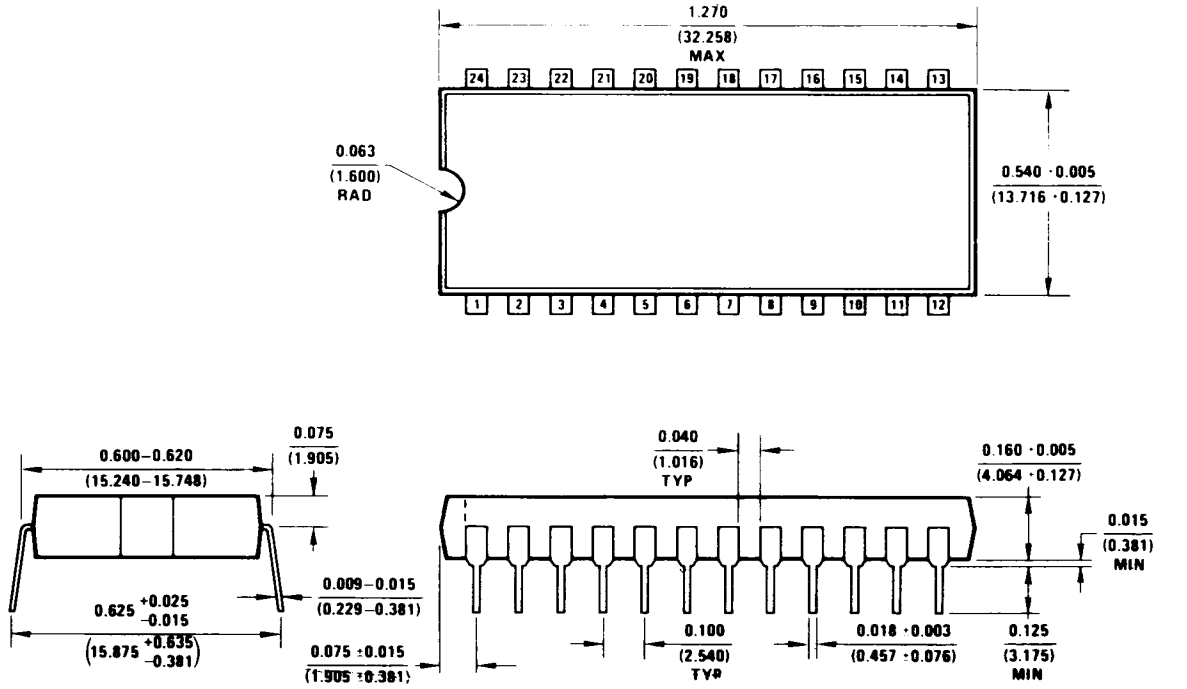
Option 33 : Chip bonding
00 : ETC 9420 (28 PIN)
01 : ETC 9421 (24 PIN)
02 : ETC 9420 and ETC 9421 (28 or 24 Pins)

Option 34 : Clock timer mode
00 : % 4, % 8, % 16
O1 : % 32
02 : Metal gate Cops 420 C compatible

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number ETC94520 N or ETC9320N
Package Number N28A



Molded Dual-In-Line Package (N)
Order Number ETC94521 N or ETC9321N
Package Number N24A

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