

### ■ Description

The EWA111 consists of a reference voltage circuit and two comparators. This bipolar IC is used to monitor the open-collector output voltage of a power supply.

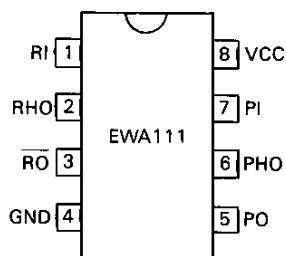
### ■ Features

- Two built-in output circuits for low supply voltage detection and reset signals
- Not many external discrete components are needed. (only three resistors for a standard application circuit)
- Wide operating voltage range ( $V_{CC} = 4.5$  to  $40V$ )
- Stable reference voltage circuit ( $2.95V$  typical)
- Stable voltage detection by built-in hysteresis circuit (hysteresis externally adjustable)

### ■ Applications

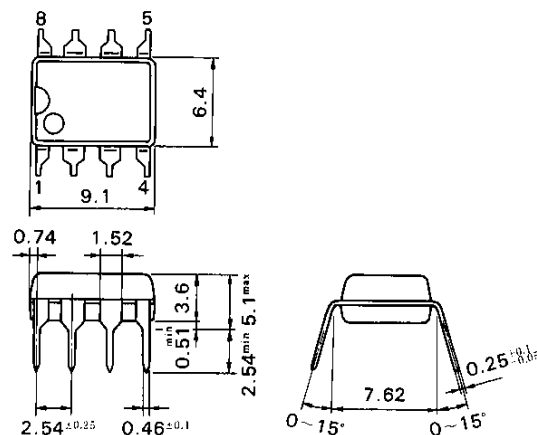
- Memory protection of microprocessor system
- Reset signal generation circuit for supply voltage drop and return
- Detection of upper and lower voltage limits

### ■ Pin assignment



### ■ Dimensions, mm

#### ● DIP-8



Pin No.	Pin symbol	Description
1	RI	RESET comparator input
2	RHO	RESET hysteresis output
3	RO	RESET output
4	GND	Ground
5	PO	P-DOWN output
6	PHO	P-DOWN hysteresis output
7	PI	P-DOWN comparator input
8	VCC	Power supply

### ■ Absolute maximum ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage *	V <sub>CC</sub>	−0.6 to +41	V
Input current	I <sub>IN</sub>	2	mA
Input voltage	V <sub>IN</sub>	−0.3 to +6.5	V
Output current	I <sub>O</sub>	30	mA
Output voltage	V <sub>O</sub>	35	V
Hysteresis circuit output current	I <sub>O HY</sub>	1	mA
Power dissipation	P <sub>d</sub>	350	mW
Operating temperature	T <sub>opr</sub>	−20 to +85	°C
Storage temperature	T <sub>stg</sub>	−30 to +150	°C

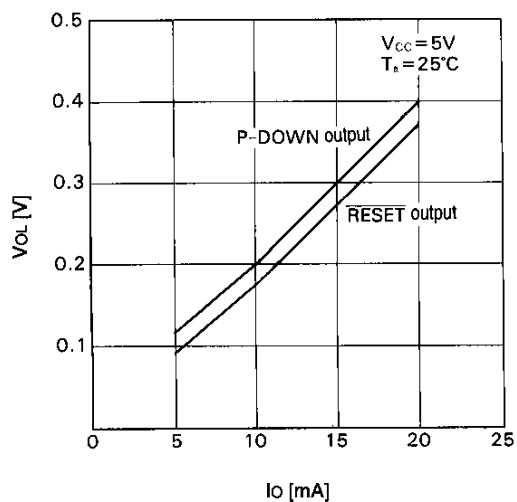
\* Recommended operation voltage range: V<sub>CC</sub> = 4.5 to 40V  
Lower limit of voltage detection: 5V

### ■ Electrical characteristics (Ta = 25°C, V<sub>CC</sub> = 5V)

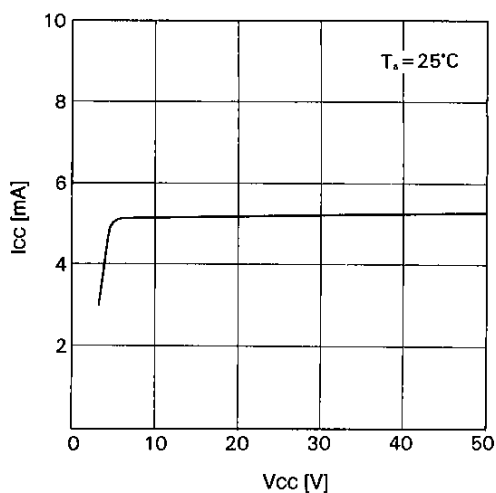
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input current	I <sub>IN</sub>				5	μA
H-level input threshold voltage	V <sub>THH</sub>		2.80	2.95	3.10	V
L-level input threshold voltage	V <sub>THL</sub>		2.67	2.82	2.96	V
Internal circuit hysteresis voltage	dV		0.10	0.13	0.17	V
L-level output voltage	V <sub>OL1</sub>	I <sub>O</sub> = 5mA			0.20	V
	V <sub>OL2</sub>	I <sub>O</sub> = 10mA			0.25	V
L-level hysteresis output voltage	V <sub>OL HY</sub>	I <sub>O</sub> = 1mA			0.40	V
R <sub>O</sub> output current	I <sub>O R1</sub>	V <sub>OL</sub> = 1V	4.0			mA
	I <sub>O R2</sub>	V <sub>OL</sub> = 1V	10.0			mA
	I <sub>O R3</sub>	V <sub>OL</sub> = 1V	20.0			mA
P <sub>O</sub> output current	I <sub>OP</sub>	V <sub>OL</sub> = 1V	10.0			mA
Supply current	I <sub>CC</sub>	V <sub>IN</sub> = 0V	2.0		8.0	mA
Temperature coefficient of reference voltage		−20 to +85°C		0.02	0.05	%/°C

## ■ Characteristic curves

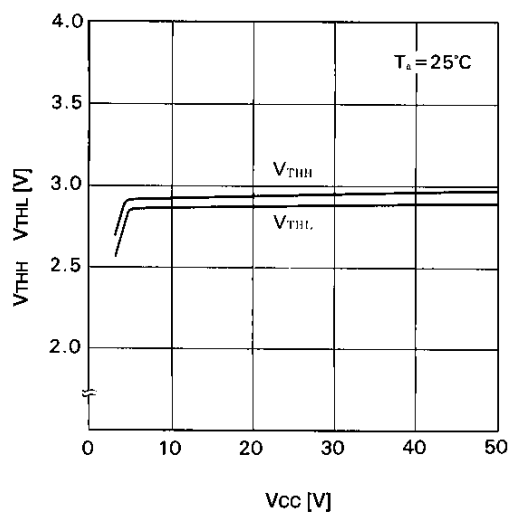
L-level output voltage ( $V_{OL}$ ) vs. output current ( $I_O$ )



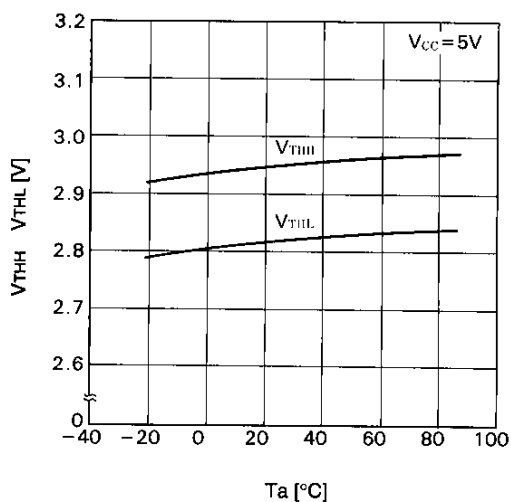
Supply current ( $I_{CC}$ ) vs. supply voltage ( $V_{CC}$ )



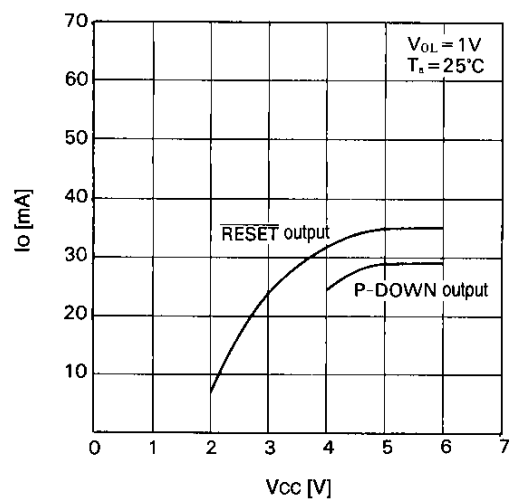
Input threshold voltage ( $V_{TH}$ ) vs. supply voltage ( $V_{CC}$ )



Input threshold voltage ( $V_{TH}$ ) vs. ambient temperature ( $T_a$ )



Output current ( $I_O$ ) vs. supply voltage ( $V_{CC}$ )



### ■ Explanation of circuits

Figure 1 shows the EWA111 block diagram. This IC consists of a reference voltage generator and two comparators. The comparator section is designed to continue functioning even when the supply voltage goes below the operating voltage range (about 2V to 4.5V). Fig 3 shows the basic use of the IC. Connect the supply voltage  $V_{IN}$  through a voltage divider formed by three external resistors ( $R_a$ ,  $R_b$ ,  $R_c$ ) to three terminals. These terminals are the input terminal PI of the P-DOWN (power down) detection circuit, the input terminal RI of the [RESET] circuit, and the power-supply terminal VCC.

Figure 2 shows how the P-DOWN and [RESET] outputs differ as the supply voltage  $V_{IN}$  varies. The [RESET] signal generation level  $V_{RIH}$  and [P-DOWN] signal generation level  $V_{PIH}$  after an increase in supply voltage  $V_{IN}$  can be calculated using formulas (1) and (2). Until the supply voltage  $V_{IN}$  exceeds  $V_{RIH}$ , the [RESET] signal output transistor remains ON and continues to output the reset signal. Until the supply voltage  $V_{IN}$  exceeds  $V_{PIH}$ , the [P-DOWN] signal output transistor remains OFF and continues to output the power-off signal.

The [RESET] signal generation level  $V_{RIL}$  and [P-DOWN] signal generation level  $V_{PIL}$  after a decrease in supply voltage  $V_{IN}$  can be calculated using formulas (3) and (4). When the supply voltage  $V_{IN}$  falls below  $V_{PIL}$ , the [P-DOWN] signal output transistor goes OFF and outputs the power-off signal. When the supply voltage  $V_{IN}$  falls below  $V_{RIL}$ , the [RESET] signal output transistor goes ON and outputs the reset signal.

$$V_{RIH} = V_{THH} \cdot (R_a + R_b + R_c) / (R_b + R_c) \quad (1)$$

$$V_{PIH} = V_{THH} \cdot (R_a + R_b + R_c) / R_c \quad (2)$$

$$V_{PIL} = V_{THL} \cdot (R_a + R_b + R_c) / R_c \quad (3)$$

$$V_{RIL} = V_{THL} \cdot (R_a + R_b + R_c) / (R_b + R_c) \quad (4)$$

Where,  $V_{THH} = 2.95V$  (typ.) and  $V_{THL} = 2.82V$  (typ.)

After power-on, the [RESET] signal must be output until the system supply voltage becomes stable. If the supply voltage decreases, the [P-DOWN] and [RESET] signals must be output within the guaranteed range of the supply voltage. For the signal output,  $V_{PIH}$  (or  $V_{PIL}$ ) and  $V_{RIH}$  (or  $V_{RIL}$ ) should be set higher than the voltage level  $V_s$  at which the supply voltage is guaranteed. The [RESET] and [P-DOWN] signal output timings depend on the rise and fall characteristics of  $V_{IN}$ . Therefore, design the system power supply by taking into consideration the signal generation levels explained above.

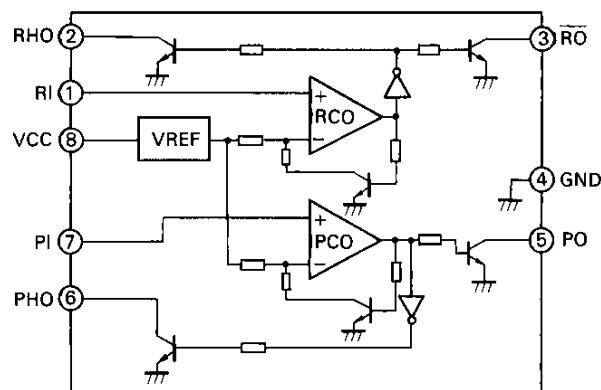


Fig. 1 Block diagram

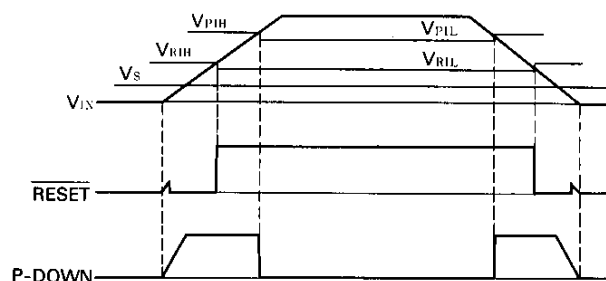


Fig. 2 Timing chart

## ■ Application circuits

### 1. Basic circuit

As shown in Fig. 3, the external part of the basic circuit consists of three resistors only. The output circuit is an open collector and may require a pull-up resistor.

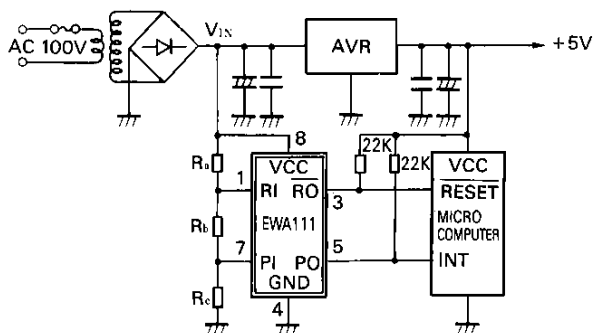


Fig. 3 Basic circuit

### 2. Hysteresis voltage external setting circuit

System power-supply conditions may require a change in hysteresis voltage value of the input voltage detection circuit. Figure 4 shows an application circuit for external adjustment of the hysteresis voltage value.  $V_{RIH}$  (or  $V_{PIH}$ ) and  $V_{RIL}$  (or  $V_{PIL}$ ) can be calculated using formulas (5) and (6).

$$V_{RIH} \text{ (or } V_{PIH}) = V_{THH} \cdot (R_a \cdot R_b + R_a \cdot R_h + R_b \cdot R_h) / (R_b \cdot R_h) \dots (5)$$

$$V_{RIL} \text{ (or } V_{PIL}) = V_{THL} \cdot (R_a + R_b) / R_b \dots (6)$$

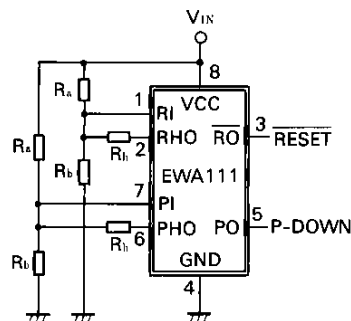


Fig. 4 Hysteresis voltage external setting circuit

### 3. Output circuit for RESET and $\overline{\text{RESET}}$ signals

A basic digital switching system often requires either  $\overline{\text{RESET}}$  or P-DOWN output only. Since the EWA111 uses exactly the same circuit for  $\overline{\text{RESET}}$  and [P-DOWN] signal detection, the output can be used as an inverted mode shown in Fig.5.

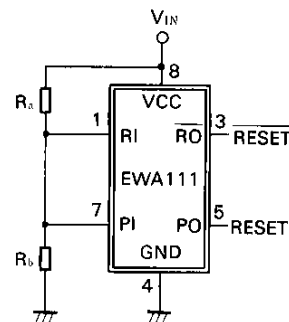


Fig. 5 Output circuit for RESET and  $\overline{\text{RESET}}$  signals

### 4. Circuit with improved output section

In some cases, the  $\overline{\text{RESET}}$  signal transistor must be ON to keep the circuit output active even when a supply voltage is not applied. The EWA111 can keep its output transistor ON even in a comparatively low voltage area (about 2V min). To obtain better output characteristics, however, the output section should be improved as shown in Fig 6. In this example, a P-channel junction-type FET is connected to the  $\overline{\text{RO}}$  terminal. Because of the depression-type characteristic, this FET remains ON even when there is no voltage between the gate and source. To ensure that the FET goes OFF when the supply voltage returns to a normal level, the gate voltage should be set higher (about 6V or more, depending on the FET type) than the source voltage. In the example shown in Fig. 6, the  $\overline{\text{RO}}$  terminal pull-up resistor is connected to  $V_{IN}$  for this purpose. Since the guaranteed breakdown voltage is 35V when the  $\overline{\text{RESET}}$  output transistor is OFF, set  $V_{IN}$  lower level than the voltage.

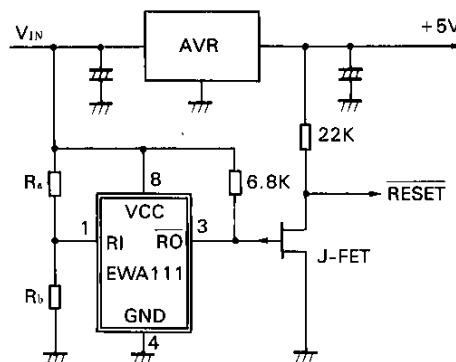


Fig. 6 Circuit with improved output section

### 5. Multi-voltage power supply monitoring

Some systems may require multiple regulated power supplies. To protect the system from a supply voltage drop, all the supply voltages must be monitored. As shown in Fig. 7, the EWA111 allows the primary voltage of the multi-voltage supply regulator to be used as  $V_{IN}$  because its operating voltage range is very wide (40V max). Since there is no need to prepare a monitoring circuit for each voltage, an application circuit can be created economically.

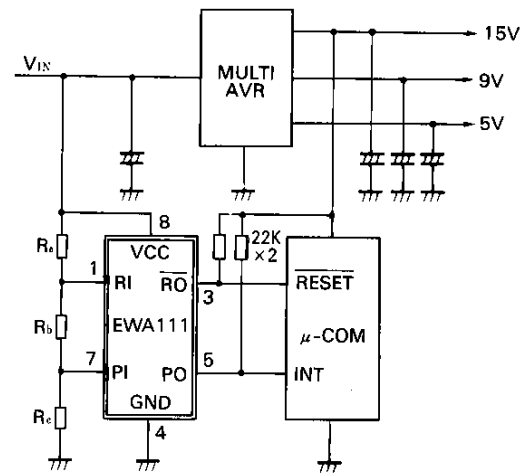


Fig. 7 Multi-voltage power supply monitoring

### 6. Signal timing delay circuit

In the examples shown so far, the IC [RESET] and [P-DOWN] signal timings depend on the rise and fall characteristics of the system power supply. However, when it is difficult to obtain the required timing (especially, delayed output timing) only by the rise and fall characteristics of the system power supply. The required timing can be obtained by using an application circuit shown in Fig. 8 to delay EWA111 signal timings. The delays  $t_{d1}$  and  $t_{d2}$  can be calculated roughly using formulas (7) and (8).

$$t_{d1} = -C \cdot \left( \frac{R_a \cdot R_b}{R_a + R_b} \right) \cdot \ln \left( 1 - \frac{T_{THH}}{V_{IN}} \cdot \frac{R_a + R_b}{R_b} \right) \dots \dots \dots (7)$$

$$t_{d2} = -C \cdot \left( \frac{R_a \cdot R_b}{R_a + R_b} \right) \cdot \ln \left( \frac{T_{THL}}{V_{IN}} \cdot \frac{R_a + R_b}{R_b} \right) \dots \dots \dots (8)$$

Where,  $V_{THH} = 2.95V$  (typ.) and  $V_{THL} = 2.82V$  (typ.)

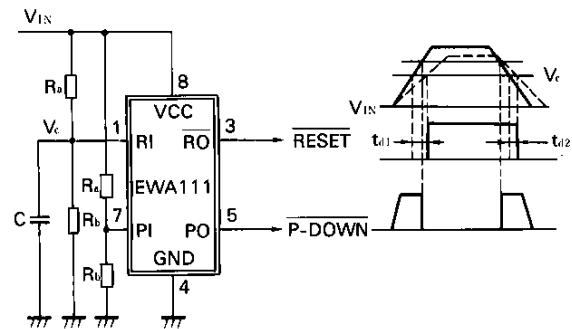


Fig. 8 Signal timing delay circuit

### 7. Upper and lower limit voltage detection circuit

The EWA111 can be used to create a circuit which issues an alarm if the supply voltage reaches its upper or lower limit. This IC has two open collector output circuits with opposite polarities. Therefore, an upper and lower limit voltage detection circuit can be created only by connecting the two output terminals ( $\overline{RO}$  and PO) as shown in Fig.9. The PI terminal is used for upper limit detection and the RI terminal for lower limit detection. The detection voltages  $V_{up}$  and  $V_{lo}$  can be calculated using formulas (9) and (10).

$$V_{up} = V_{THH} \cdot (R_a + R_b + R_c) / R_c \dots \dots \dots (9)$$

$$V_{lo} = V_{THL} \cdot (R_a + R_b + R_c) / (R_b + R_c) \dots \dots \dots (10)$$

Where,  $V_{THH} = 2.95V$  (Typ.) and  $V_{THL} = 2.82V$  (Typ.)

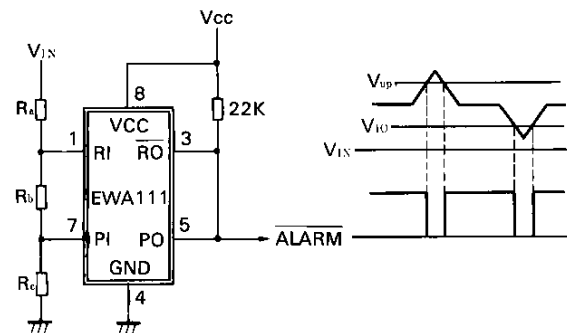


Fig. 9 Upper and lower limit voltage detection circuit

### 8. Battery protection circuit

A battery-operated circuit or device may require a battery protection circuit. The protection circuit should issue an alarm if the battery voltage  $V_{BB}$  decreases, and cut off the current if  $V_{BB}$  continues to decrease. Fig. 10 shows an example of such a protection circuit. Because of its comparatively large output sink current (20mA max), the EWA111 can control the comparatively large switching transistor  $Tr$  current. Aside from issuing an alarm signal [ALARM], this IC can also be used to drive an alarm LED as indicated by the dotted line.

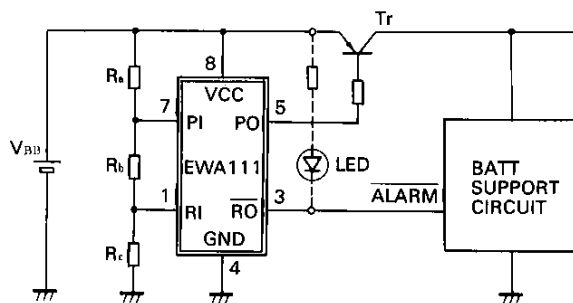


Fig. 10 Battery protection circuit

### 9. Pulse error detection circuit

The EWA111 can also be used to detect abnormal clock pulse widths, duty ratios, or frequencies to protect pulse transformers or similar. In Fig. 11, pulse signals from the system clock circuit are integrated through the buffer circuit into EWA111 input signals to detect pulse error.

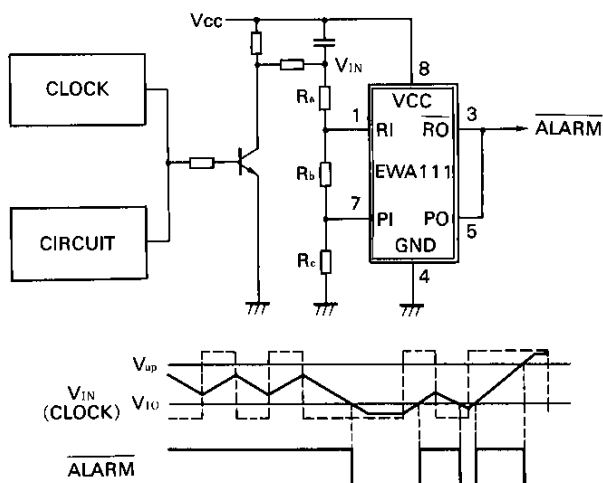


Fig. 11 Pulse error detection circuit

### 10. Monostable multivibrator circuit

With the EWA111, a monostable multivibrator circuit with an accurate input threshold voltage can be created. Figure 12 shows an example of such a monostable multivibrator circuit. The output pulse width,  $t_m$ , can be set easily using resistor  $R$  and capacitance  $C$ . Calculate it using formula (11).

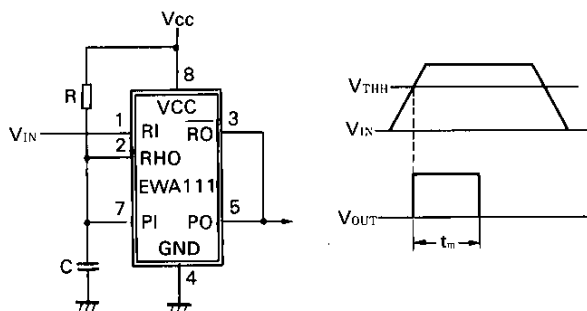


Fig. 12 Monostable multivibrator circuit

### 11. Delay circuit ①

In the monostable multivibrator circuit shown in Fig. 12, disconnect  $\overline{RO}$  output and PO output of the EWA111 to obtain a delay signal  $[V_{OUT2}]$  from the PO output terminal as shown in Fig.13. The delay time,  $t_d$ , can be set free with resistor R and capacitance C. Calculate it using formula (11).

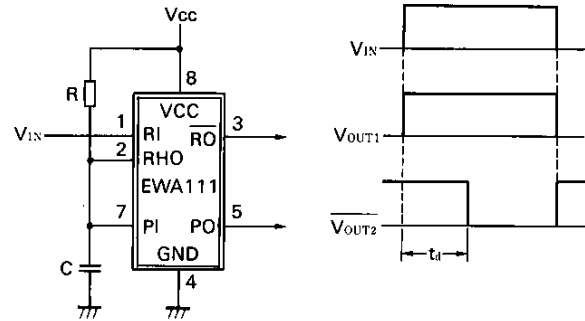


Fig. 13 Delay circuit ①

### 12. Delay circuit ②

Figure 14 shows a circuit for obtaining a inphase delay signal  $[V_{OUT1}]$  for an input signal. The delay time,  $t_d$ , can be set free with resistor R and capacitance C. Calculate it using formula (11).

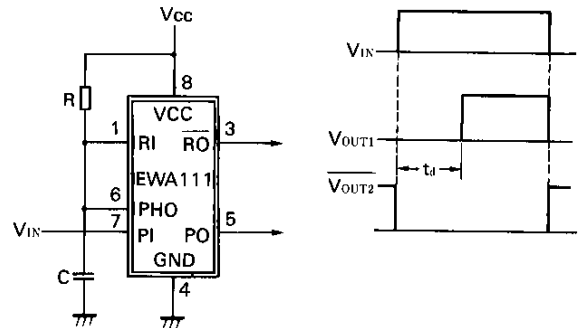


Fig. 14 Delay circuit ②

### 13. Astable multivibrator circuit

Figure 15 shows an example of an EWA111-applied astable multivibrator circuit. The output transistor ON time  $t_{on}$ , OFF time  $t_{off}$ , and cycle  $t$  can be calculated using formulas (12), (13), and (14).

$$t_{on} = C \cdot R \cdot \ln(V_{THL}/V_{THH}) \quad (12)$$

$$t_{off} = -C \cdot (R + R_L) \cdot \ln \left( 1 - \frac{V_{THH} - V_{THL}}{V_{CC} - V_{THL}} \right) \quad (13)$$

$$t = t_{on} + t_{off} \quad (14)$$

Where,  $V_{THH} = 2.95V$  (typ.) and  $V_{THL} = 2.82V$  (typ.)

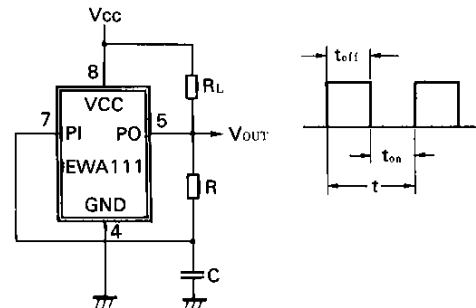


Fig. 15 Astable multivibrator circuit



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