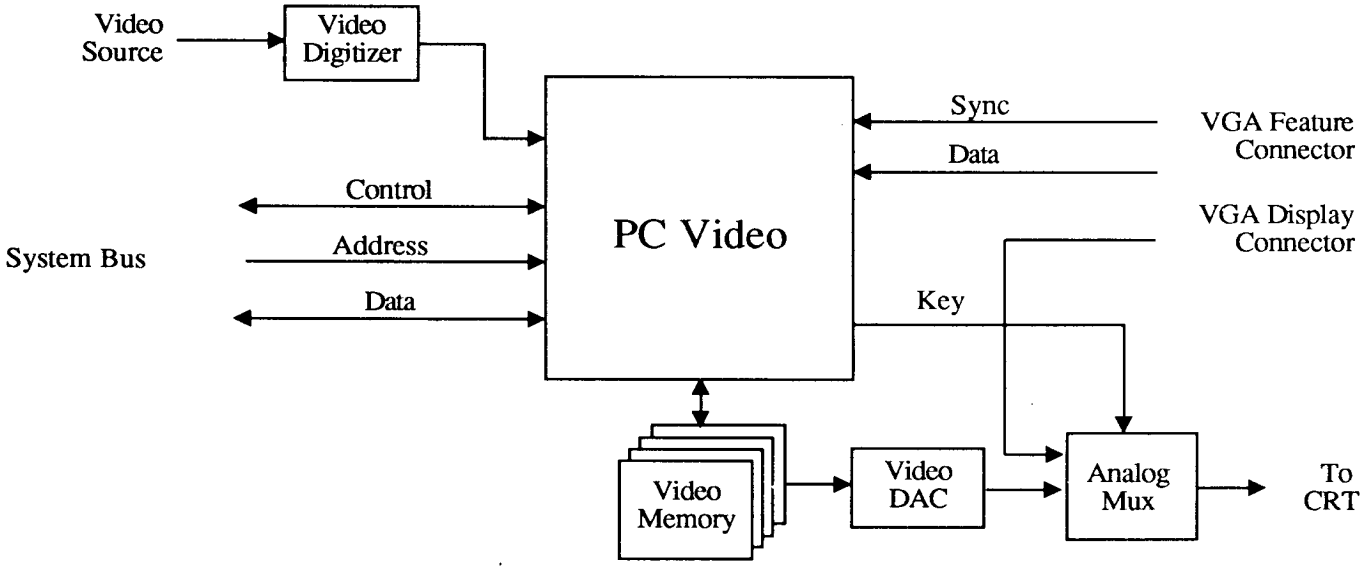
82C9001A
PC Video™
Video Windowing Controller

- Scan rate conversion and windowing control for display of a live video image on a computer graphics monitor
- Window positioning controlled by independent X-Y coordinates and by color keying
- Independent X-Y scaling of video image to 1/64 original image size
- Still-frame capture and display of true-color images
- Input resolutions up to 1024H x 512V pixels with full broadcast quality video bandwidth
- Up to 800 x 600 display resolution
- Supports NTSC, PAL, SECAM, S-VHS, and RGB input formats from industry-standard video digitizer chipsets
- Supports standard 4:1:1 and 4:2:2 YUV and 16-bit RGB digital formats
- Supports a memory efficient 2:1:1 YUV format
- Interlaced or non-interlaced input video
- Interlaced or non-interlaced output support
- Output zoom by factors of 2, 4 and 8
- Full-motion color video support on flat-panel displays with the 82C457



PC Video System Block Diagram

Revision History

Revision	Date	By	Comment
1.5	8/91	ME	Intinal Release
2.0	4/92	ME/ST	Modified Electrical Specifications Added Design Considerations

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Introduction

OVERVIEW

The PC Video video windowing chip is the core component of a video subsystem which converts a standard full-motion video image into a format for display on a computer graphics monitor. PC Video controls positioning and scaling of the video image on the output display and allows the video image to be merged with computer graphics for interactive multimedia applications. Market applications of a subsystem based on PC Video include interactive video training, computer-based education programs, point-of-sale information, business presentations, video conferencing, and desktop publishing. PC Video integrates all the controlling logic for video scan rate conversion, windowing control, and scaling. Operation with VGA graphics is supported via the graphics feature connector.

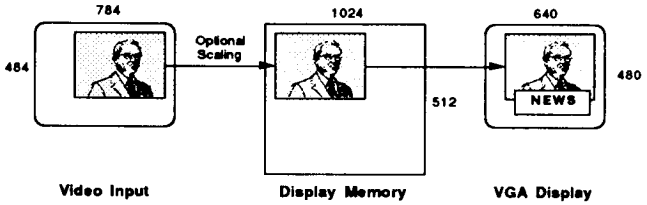
A video windowing sub-system can be implemented with the following components:

- PC Video
- A standard "Digital TV" chip set
- 4 VRAMs

Other optional configurations are supported for higher color and luminance bandwidth.

WINDOW ACQUISITION AND POSITIONING

PC Video provides the control signals for a standard video digitizer chip set. Interlaced and non-interlaced video sources, at full broadcast quality bandwidth, are supported at resolutions up to 1024 x 512 pixels. PC Video may be programmed to capture a full-size video image or a user-defined cropped or reduced area.



Acquisition & Display Process

Video output window positioning is provided by programmable X-Y coordinates and color keying to a specified color. Color Keying is based on the digital color information from the VGA feature connector. Color keying is supported independently or in conjunction with X-Y coordinates.

SCALING

PC Video provides independent X-Y scaling of the input video image in integer increments of 1/64. Images may be compressed down to 1/64 of the original image size, supporting video icons for graphical user interfaces.

MEMORY INTERFACE

PC Video operates with 256K x 4 100 ns VRAMs. Three configurations are supported: 4 VRAMs for 2:1:1 encoding, 6 VRAMs for 4:1:1 encoding, and 8 VRAMs for 4:2:2 and 16-bit RGB encoding.

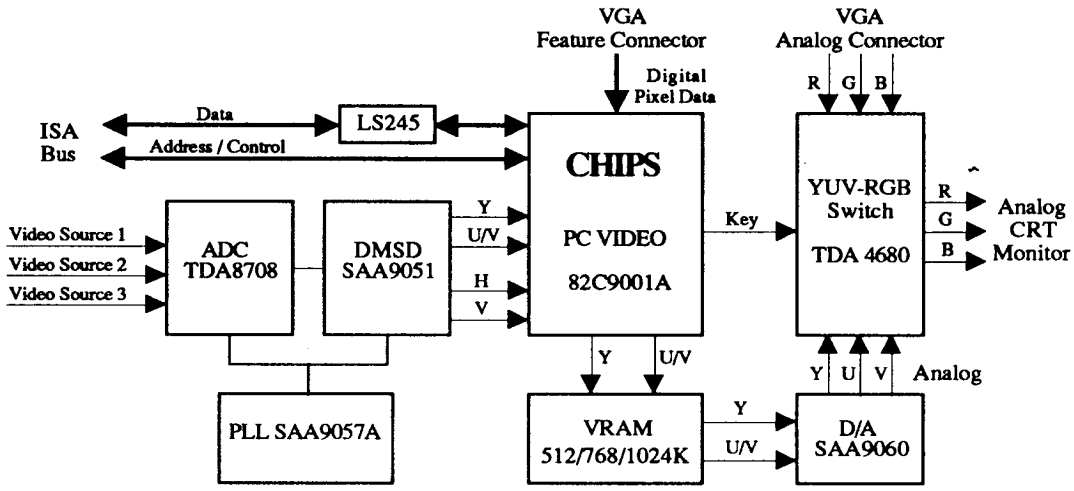
Memory Requirements

Bits per Pixel	Format	Memory Required	Video Quality
12-bit	2:1:1 YUV	4 VRAM	Compressed luminance bandwidth
12-bit	4:1:1 YUV	6 VRAM	Broadcast video bandwidth
16-bit	4:2:2 YUV	8 VRAM	Improved chroma bandwidth
16-bit	16-bit RGB	8 VRAM	65,536 colors

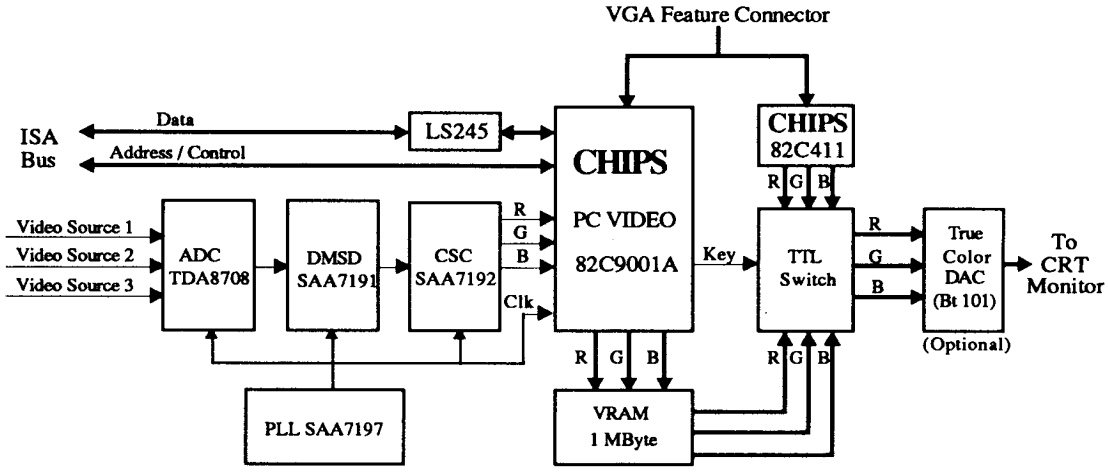
COLOR FLAT-PANEL SUPPORT

PC Video, with the 82C457 Color flat panel controller and the 82C411 pallette chip, provides full-motion video on a color LCD. The 82C457 dithers the PC Video output data to provide 20,000 colors on a 512-color display.

System Configuration Examples

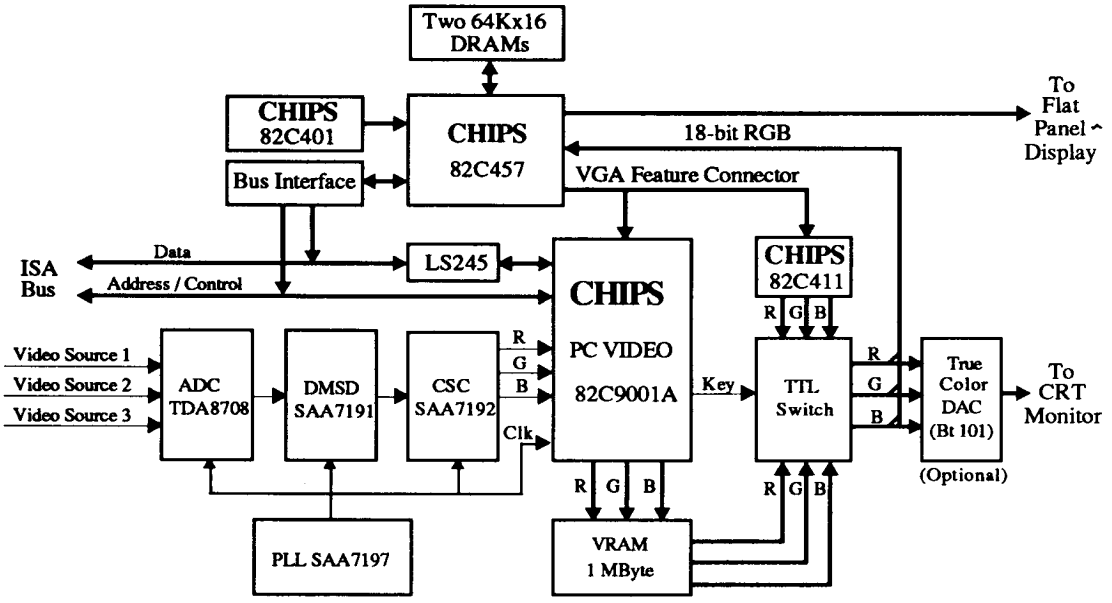


PC Video YUV Implementation



PC Video RGB Implementation

System Configuration Examples



Full-Motion Video on Color LCD Implementation

PC VIDEO DESCRIPTION

VIDEO FORMATS

Color images in computer graphics are typcially represented by R, G, and B components. Video and TV images are typically represented by one luma (Y) and two chroma (U, V) components which make up a composite video signal. The luma component has twice the bandwidth of the individual chroma components. Digitized video systems typically use luma/chroma components because of the ease of conversion to and from composite video signals. Representation of an image in luma/chroma is also more memory efficient than in R, G, and B components. A 640x480 image in 16-bit RGB produces 65,536 colors and requires 1 meg of VRAM. The same image can be saved in Luma/Chroma coordinates in 768k of VRAM and produces 2 million colors.

PC Video's flexibility allows it to support both R, G, B and Y, U, V components. Four main formats are supported as described below.

The X:Y:Z numbers refer to the number of samples for the three input video components.

1) 4:1:1 – The luma component (Y) is sampled every pixel and the chroma components (U, V, or Yr, Yb) are averaged over four pixels. For every four input pixels, there are four luma samples and one U and V (chroma) sample, for six samples total.

2) 4:2:2 – This format expands the color bandwidth of the 4:1:1 format. The chroma components are averaged over two pixels. For every four input pixels, there are four luma samples and two of each chroma samples, for eight samples total. This is the international broadcast standard CCIR 601.

3) 2:1:1 – This is the most memory efficient format. The luma component is averaged over two pixels and the chroma components are averaged over four pixels. For every four input pixels, there are two luma samples and one of each chroma samples, for four samples total.

4) 4:4:4 – This format is typically used for R, G, B components but could also be used for luma and chroma components. The components are sampled at every pixel, resulting in 12 samples to four pixel times. The bandwidth on all components is the same.

SIGNAL FLOW

Image acquisition and display in a PC Video subsystem are two independently programmable processes which occur at asynchronous clock rates.

Acquisiton

PC Video provides the control signals to a standard digital video chipset. The acquisition window coordinates are programmable, enabling cropping and panning of the input image. The digitized video passes through PC Video's internal FIFO and is stored in the frame buffer. The acquisition process is synchronized to the input video VSYNC and HBLANK signals, and is executed at the video sampling rate. The image acquisition data is applied to the random access ports of the dual-ported video rams. Scaling is performed upon the input video data as part of the acquisition process. The scaled image is stored in the frame buffer.

When acquiring PAL format video, a maximum of 512 lines of the 576 active lines are acquired, selected by the input cropping window or input scaling. Through input scaling the full PAL picture can be viewed on a VGA display with the aspect ratio preserved.

The input window supports both interlaced (default) and non-interlaced video. Four capture modes are available: (a) Interlaced frame, (b) Even field, (c) Odd field), and (d) Non-interlaced frame.

In unscaled, interlaced mode the raster address is advanced by two, with the even field writing the even line numbers and the odd field writing odd lines. The even field starts at line 0 and advances by 2's : 0,2,4... The odd field starts at line 1 and advances by 2's : 1,3,5... up to the maximum line count.

An address multiplexer selects addresses for the acquisition window, video display window or the host processor. Either live video acquisition or CPU read/write access may take place but not both simultaneously.

Display

The display process is synchronized to the VGA HSYNC, VSYNC, BLANK, and CLOCK signals from the feature connector. The data is output from the serial port of the video rams. The video image may be displayed inside or outside any rectangular window on the VGA screen.

SYSTEM CLOCKS

The video ram control/timing logic uses the double rate video input clock. The double clock rate of 27 MHz is line-locked, tracking variations in input video sync, which occur with video tape recorders (VTR's), still-video cameras and other non-time base stable sources. The maximum input clock rate is 30 MHz.

CPU INTERFACE

PC Video has a non-multiplexed 24-bit address bus and a 16-bit data bus. PC Video latches AT bus addresses LA[20:23] using the AT bus signal ALE. PC Video memory is accessible using 8 and 16-bit bus cycles while PC Video I/O registers are accessible using 8-bit cycles only. PC Video handles all byte swapping for memory accesses. PC Video supports 16-bit memory cycles and generates MEMCS16/ when memory is mapped above 1M byte in the PC address space. PC Video-based boards can be plugged in to a 16-bit bus slot.

PC Video may be programmed to respond to either a fixed I/O address or software programmed I/O address. When the bus RESET signal goes from high to low, the status of CS/ pin is sampled by PC Video. If CS/ is sampled active (low) then PC Video responds to I/O addresses 0AD6-7hx. However if CS/ is inactive (high) then it uses the Programmed I/O Address Register bits 7:0 and CS/ to detect the valid I/O address space. When this mode is selected, the Programmed I/O Address Register bits are written by the first CPU I/O write cycle with CS/ active. Since PC Video always occupies two consecutive I/O addresses, bit-0 of this register is ignored.

MEMORY INTERFACE

Memory is organized as 2 banks totaling 1024 wide by 512 high. The depth of the memory is either 12 bits for 4:1:1 multiplexed data format, or 16 bits for the 4:2:2 multiplexed and 4:4:4 non-multiplexed data formats.

PC Video uses 256Kx4, 100 nS VRAMs and it supports three VRAM configurations, (1) Two banks of VRAM with three VRAMs in bank-0 and one VRAM for chroma in bank-1, (2) Two banks of VRAM with three VRAMs per bank and (3) Two banks of VRAM with 4 VRAMs per bank. PC Video also supports the VRAM Write Bit Mask function. The frame buffer memory is accessible as a linear address space above 1024K (100000h), located on any 1024K boundary. The Video Frame Buffer memory can be accessed with byte or word cycles. PC Video generates one wait state for normal memory accesses, and more than one wait state when memory accesses conflict with VRAM refresh cycles or data transfer cycles. When PC Video memory is accessed by the CPU, video capture must be halted by software prior to the access. PC Video memory is not accessible on RESET and must explicitly be enabled to access the PC Video memory.

INTERRUPT SUPPORT

PC Video supports CPU interrupts upon receipt of a video Vsync. The interrupt source bits are held until cleared by software.

VIDEO RAM TIMING GENERATOR

A synchronous timing generator operates the video RAM control signals, derived from the double rate video data clock. The video RAM is operated as two banks each running in "fast-page" mode along the line. Each bank receives alternating pixels across the horizontal line, using a common data bus driven at the pixel rate of 13.5 MHz. The column address signal (CAS) or write enable (WE) of each bank strobes in the pixel data.

Memory refresh occurs during input video horizontal blanking. Processor access is limited to times when the acquisition window is "frozen" and page mode write cycles are disabled. CPU access utilizes a standard read/write cycle using the parallel data path, bypassing the input video FIFO.

The VGA display window uses the 1 MEG (256Kx4) VRAM serial shift register to scan-out the display data. The VRAM serial output is used only in read mode and two banks of VRAMs operate in a ping-pong style data organization providing 1024 pixels per line from two 512 pixel VRAM shift registers.

The following VRAM memory cycles are supported:

Cycle Type	Function
1) Random Read/Write cycle	processor access
2) CAS before RAS refresh	refresh only
3) Shift Register Load	loading shift register for output display
4) Fast-page mode write	video acquisition
5) Write Bit Mask	masking of data bits during video acquisition or CPU write
6) Shift register output	clocked at one half the output display rate

SCALING

Two independent input scaling ratios are supported: one for the horizontal, the other for the vertical. The vertical ratio accounts for interlace.

Scaling is performed by dropping pixels horizontally and dropping lines vertically. Independent scaling factors, ranging from 1/64 to 63/64 in multiples of 1/64 are supported in the horizontal and vertical directions. 64/64 is supported by turning the scaling off.

DISPLAY WINDOW OVERLAY

The mixing of the analog VGA and analog video data is performed externally using an analog multiplexer. The multiplexer control signal can be generated in three different ways:

a) By defining an output window in the PC Video X-Y Window Control Registers,
b) By keying to a VGA Color (Color compare) or
c) By writing a pattern in the LSB of display memory.

The multiplexer function for cases (a) and (b) is generated by PC Video and is clocked by the VGA clock (PCLK). In case (c), the LSB of display memory is externally gated to control the analog multiplexer.

X-Y Window Control Registers:
The X-Y window area is defined by four registers that specify a rectangular region using X-start, X-end, Y-start, and Y-end. The X-Y window position is referenced to the VGA sync signals. The size of the X-Y window is defined in VGA clocks and lines.

Color Keying:
A control signal is generated by comparing the 8 bit VGA TTL video data (P7:0) to an 8 bit value in the Color Key register. To support more than one color at a time, an 8 bit VGA Data Mask register is provided. This mask register suppresses the compare on those data bits for which a '1' is written to the corresponding bit position of the VGA Data Mask register. The VGA pixel data is sampled by PCLK.

LSB of display Data:
The LSB of the display memory may be used to control the analog multiplexer. PC Video supports the VRAM write-per-bit mask function. Software can write a pattern in the LSB of the display memory and use the mask to write-protect the keying pattern. The LSB of memory is then used to control the analog multiplexer on a pixel by pixel basis. Since the LSB of display memory is write protected, video acquisition cycles do not modify this bit. The write-per-bit mask may be used on any bit in the 16-bit wide data path. Typically the LSB of the luminance data is used since the luminance data is usually only 7 bits wide for 4:1:1 input.

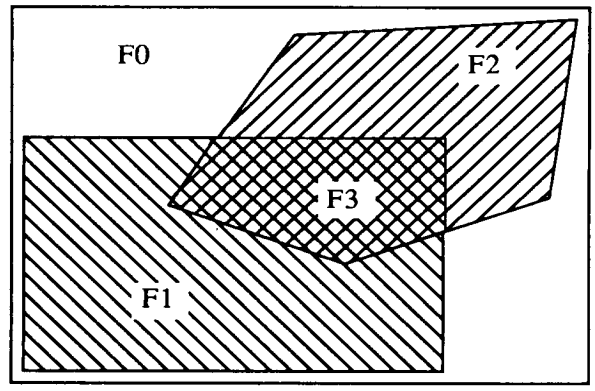
Overlay Functions:
There are four possible combinations of the display window and color key areas. They are: non window and non key area (F0), window area but not key (F1), key area but not window (F2) and both window and key area (F3). These four functions select one of the function bits on a pixel by pixel basis. If the function bit for that area is a '0', that display area shows the VGA graphics. If the function bit for that area is '1', the video output data is overlayed on top of the VGA graphics. If the X-Y window is disabled, areas F1 and F3 do not exist. If color keying is disabled, areas F2 and F3 do not exist.

DISPLAY AREA PANNING

Video data in the display area can be panned horizontally by 1024 pixels in steps of 4 pixels for 4:1:1 input Y/C format or in steps of 2 pixels for 4:2:2 input Y/C format. Video data may be panned vertically by 511 in steps of 1 scan line.

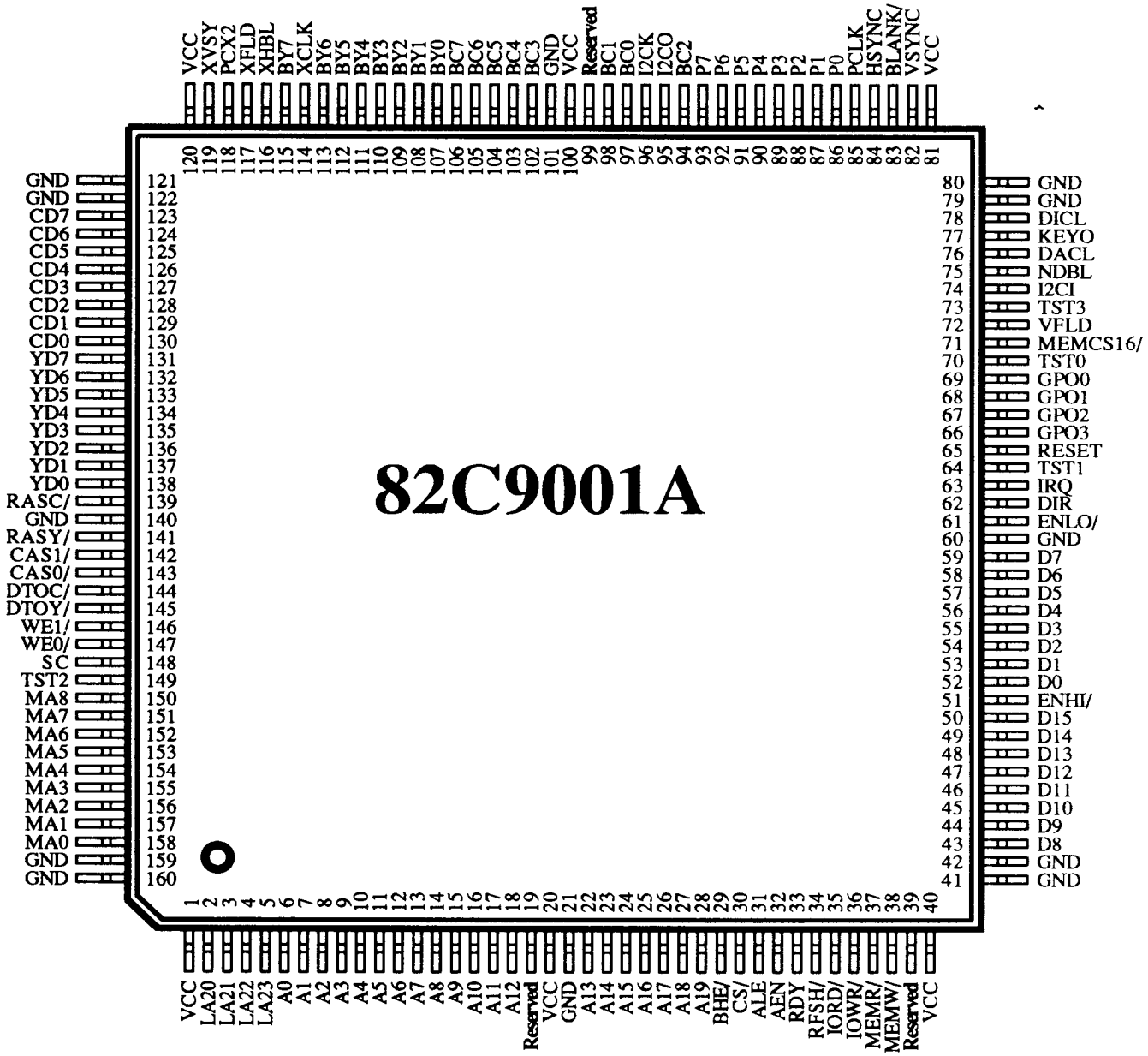
GLOBAL ENABLE/DISABLE OF PC VIDEO

PC Video I/O register index FFh is reserved for global enable and disable of PC Video. This register is a write only register. Bit-0 of this register is used to control register access. This bit is cleared on RESET. After PC Video's I/O address is determined, this bit should be set to '1' to enable access to other PC Video I/O registers. The PC Video frame buffer is accessable when bit-1 of this register is set to '1'. The upper 4 bits of this register are readable and they reflect the PC-Video Revision/Part Number.



Overlay Functions

Pinouts



PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name	Type	Active	Description
6	A0	In	High	20 bits of system address bus.
7	A1	In	High	
8	A2	In	HIgh	
9	A3	In	High	
10	A4	In	High	
11	A5	In	High	
12	A6	In	High	
13	A7	In	High	
14	A8	In	High	
15	A9	In	High	
16	A10	In	High	
17	A11	In	High	
18	A12	In	High	
22	A13	In	High	
23	A14	In	High	
24	A15	In	High	
25	A16	In	High	
26	A17	In	High	
27	A18	In	High	
28	A19	In	High	
2	LA20	In	High	Upper 4 bits of the system address bus. These address bits are latched on the falling edge of ALE.
3	LA21	In	High	
4	LA22	In	High	
5	LA23	In	High	
52	D0	I/O	High	System data bus.
53	D1	I/O	High	
54	D2	I/O	High	
55	D3	I/O	High	
56	D4	I/O	High	
57	D5	I/O	High	
58	D6	I/O	High	
59	D7	I/O	High	
43	D8	I/O	High	
44	D9	I/O	High	
45	D10	I/O	High	
46	D11	I/O	High	
47	D12	I/O	High	
48	D13	I/O	High	
49	D14	I/O	High	
50	D15	I/O	High	
65	RESET	In	High	Reset input.
34	RFSH/	In	Low	System Refresh. When this input is low, the current memory cycle is ignored.
61	ENLO/	Out	Low	Enable controls for external data transceivers for the Data bus.
51	ENHI/	Out	Low	

PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name	Type	Active	Description
62	DIR	High	High	Direction control for external data bus transceivers: 0 = read from PC Video, 1 = write to PC Video.
29	BHE/	In	Low	Enable for 16-bit interface. Low indicates that the high order byte at the current word address is being accessed. Along with A0, indicates which bytes are transferred over the bus (all byte steering is done internally): BHE/ A0 Effect 0 0 Both bytes on D15:0 0 1 High byte on D15:8 1 0 Low byte on D7:0
32	AEN	In	High	Defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (DMA cycle). If single-cycle DMA is used, memory addresses will be on the bus at the same time that IORD/ or IOWR/ is active. PC Video will not respond to IORD/ or IOWR/ while AEN=1.
31	ALE	In	High	Address latch enable. The system address is latched on the falling edge of this signal.
33	RDY	Out	High	Ready. Driven low to indicate the current cycle should be extended with wait states. Driven high at end of cycle to indicate 'ready' then tri-stated. This signal is normally tri-state and is only driven low if PC Video cannot respond immediately to a memory request and wait states are necessary.
71	MEMCS16/	Out	Low	Indicates 16-bit Memory cycle. Asserted by PC Video to indicate that the chip is capable of transferring 16 bits over the bus at the requested address.
37	MEMR/	In	Low	Indicates a memory read cycle from AT bus.
38	MEMW/	In	Low	Indicates a memory write cycle from AT bus.
35	IORD/	In	Low	Indicates an I/O Read cycle.
36	IOWR/	In	Low	Indicates an I/O Write cycle.
63	IRQ	Out	High	Video VSYNC Interrupt. This pin is low when interrupts are enabled but no interrupt is pending, and high when interrupts are enabled and an interrupt is pending.

PIN DESCRIPTIONS

Video Memory Interface

Pin #	Pin Name	Type	Active	Description
131	YD7	I/O	High	Luminance Data bus. These pins connect to the VRAM data pins.
132	YD6	I/O	High	
133	YD5	I/O	High	
134	YD4	I/O	High	
135	YD3	I/O	High	
136	YD2	I/O	High	
137	YD1	I/O	High	
138	YD0	I/O	High	
123	CD7	I/O	High	Chrominance Data bus. These pins connect to the VRAM data pins.
124	CD6	I/O	High	
125	CD5	I/O	High	
126	CD4	I/O	High	
127	CD3	I/O	High	
128	CD2	I/O	High	
129	CD1	I/O	High	
130	CD0	I/O	High	
150	MA8	Out	High	VRAM Address bus for both banks and planes of memory.
151	MA7	Out	High	
152	MA6	Out	High	
153	MA5	Out	High	
154	MA4	Out	High	
155	MA3	Out	High	
156	MA2	Out	High	
157	MA1	Out	High	
158	MA0	Out	High	
141	RASY/	Out	Low	VRAM Row Address Strobe for Luminance plane.
139	RASC/	Out	Low	VRAM Row Address Strobe for Chrominance plane.
142	CAS1/	Out	Low	VRAM Column Address Strobe. There is a strobe for each bank of memory.
143	CAS0/	Out	Low	
146	WE1/	Out	Low	VRAM Write Enable. There is an enable for each bank of memory.
147	WE0/	Out	Low	
145	DTOY/	Out	Low	Data Transfer / Output Enable. There is a control for each bank of memory.
144	DTOC/	Out	Low	
148	SC	Out	High	VRAM shift Clock for all VRAMs. This signal is also used to multiplex the output data from the VRAM banks.
86	P0	In	High	Pixel Data from the VGA feature connector. This data is used for color matching to control overlay of VGA graphics and video output.
87	P1	In	High	
88	P2	In	High	
89	P3	In	High	
90	P4	In	High	
91	P5	In	High	
92	P6	In	High	
93	P7	In	High	

PIN DESCRIPTIONS

VGA / Video Interface

Pin #	Pin Name	Type	Active	Description
85	PCLK	In	High	VGA Pixel Clock. This clock is used to latch the VGA pixel data and synchronize the video overlay window.
84	HSYNC	In	High	Horizontal, Vertical Sync, and Blank signals from the VGA feature connector. These signals are used to synchronize the overlay of video and VGA graphics.
82	VSYNC	In	High	
83	BLANK/	In	Low	
72	VFLD	In	High	External Field bit. When selected, this signal identifies the odd/even field sequence of the interlaced output video data stream.
107	BY0	In	High	Luminance Data from the digital video source. This data is buffered and stored in the VRAM for Video output.
108	BY1	In	High	
109	BY2	In	High	
110	BY3	In	High	
111	BY4	In	High	
112	BY5	In	High	
113	BY6	In	High	
115	BY7	In	High	
97	BC0	In	High	Chrominance Data from the digital video source. This data is buffered and stored in the VRAM for Video output.
98	BC1	In	High	
94	BC2	In	High	
102	BC3	In	High	
103	BC4	In	High	
104	BC5	In	High	
105	BC6	In	High	
106	BC7	In	High	
114	XCLK	In	High	Video Data Clock. This clock is to latch the Video data from the digital video source.
118	PCX2	In	High	Twice Video Data Clock. This clock is twice the Video data clock rate. It is used to generate the VRAM timing.
119	XVSY	In	High	Vertical Sync signal from the digital video source. This signal is used to synchronize the storage of the video data.
116	XHBL	In	High	Horizontal Blank. This signal is used to identify the active area in the digital video output data stream.
117	XFLD	In	High	External Field bit. PC Video uses internally generated field signal, by default. However, if required, the field signal from this pin can be selected by setting bit 6 of Register 21 to '1'.
30	CS/	In	Low	Chip Select (I/O only.) This pin is sampled on the falling edge of reset. If it is low, PC Video will respond to I/O accesses at locations 0AD6 and 0AD7. If it is high, then the Programmed I/O Register and the CS/ input are used to detect a valid I/O address.

PIN DESCRIPTIONS

Multi-function, Power, and Ground

Pin #	Pin Name	Type	Active	Description
96 95 74	I2CK I2CO I2CI	Out Out In	High High	These open collector I/O pins are designed to support the Intermetal Industrial Control (I^2C) bus.
78	DICL	In	High	Display Clock input. This input supplies the clock that is used to output the digital video data.
76	DACL	Out	High	Video DAC Clock. This signal clocks the output video data into the video DACs. Derived from DICL.
75	NDBL/	Out	Low	Video Blank output to DAC. This signal is synchronized with DICL and qualifies valid video data from the VRAM memory.
77	KEYO	Out	Low	Video / VGA Mux. When high, the output data mux selects Video data; when low, the output is VGA graphics.
66 67 68 69	GPO3 GPO2 GPO1 GPO0	Out Out Out Out	High High High High	General Purpose I/O and strobes. These pins may be used as I/O strobes for additional user defined external registers. GP01 can be defined as a phase locked loop reference output by setting bit 5 of register 18 to "0".
1 20 40 81 100 120	VCC	Pwr	-	+ 5V Power Pins
21 41 42 60 79 80 101 121 122 140 159 160	GND	Pwr	-	Ground Pins
70 64 149 73	TST0 TST1 TST2 TST3	Out Out Out Out	High High High High	Test Pins. These pins should be left unconnected.
19 39 99	Reserved Reserved Reserved	- - -	- - -	Reserved. These pins should be left unconnected.

Registers

REGISTER ADDRESSING

The address location of the PC Video control registers is determined by the status of the CS/ input at RESET. If the CS/ input is low on the falling edge of RESET, then PC Video responds to a fixed I/O address, 0AD6-7h. (CS/ must be low for a valid I/O decode.) If CS/ is inactive (high) then a programmable address is used. The value present on the data bus during the first valid I/O write (CS/=0, IOWR/=0) following a RESET cycle, is loaded into the Programmed I/O Address Register bits 7:0. This value is then used to determine the I/O address location for the PC Video registers. Since PC Video always occupies two consecutive I/O addresses, bit-0 of this register is ignored. The least significant 8 bits of the I/O address are determined by the value in the Programmed I/O register. The remaining address bits are then dependent on the external decode logic that generates the CS/ strobe.

The setup and control registers for the PC Video chip occupy two consecutive address locations. The first or even location contains an index register. The index register determines or "points" to all the other registers. The second or odd location is the data port for the selected register. To access a PC Video register, the index value for the desired register is written to the index register. The data for that register may then be read or written at the data register location.

There are four groups of control registers inside the PC Video chip. They are CPU interface, General Purpose I/O control, Video Acquisition, and Display Window control. All registers are read/write once PC Video has been enabled using bit-0 of the Global Enable Register.

CPU INTERFACE REGISTERS

These registers are used to enable/disable PC Video, store the I/O address location, specify the memory address and configuration, set the buffer memory write mask and service interrupts. Bit 0 of the Global Enable Register (Index: FFh) must be set to '1' before any other registers may be read or written. This register and the Index Register are write-only until this bit is set.

GENERAL PURPOSE I/O REGISTERS

These registers control the General Purpose I/O pins and the I^2C bus interface.

VIDEO ACQUISITION REGISTERS

These registers are used to control acquisition of a live motion video data stream. They provide data on the current acquisition status and control the input acquisition window, scaling, and storage location in memory.

DISPLAY WINDOW REGISTERS

These registers are used to control the output video data stream and color keying. They provide control of the output window location and size, data start location (panning), shift clock, analog multiplexer skew, VGA color key, and mask.

Register Quick Reference

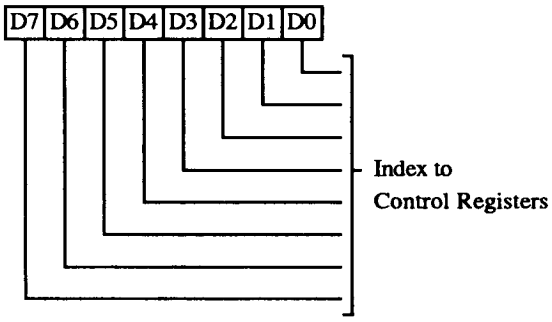
Register Description	Index	Data Bits 7-0							
Version/Global Enables	FF	0	0	0	1		IOW~Dlyd	Mem En	I/O En
I/O Address (default)	00	1	1	0	1	0	1	1	0
Memory Access Control	01		(0)		En WBMsk				
Linear Memory Base Add	06				(1)	Linear Memory Base Address			
Luma Bit Mask	07	Write Bit Mask for luminance data							
Chroma Bit Mask	08	Write Bit Mask for chrominance data							
Interupt Mask/Polling	09			Po VGA Hs	Po VGA Vs	Po VidFld	Po VidVs	Even VidVs	Odd VidVs
GPIO Reg 0	10								
GPIO Reg 1	11								
GPIO Reg 2	12								
GPIO Reg 3	13								
I2C Bus Control	18	(0)	(0)	Decode GP1	(0)	(0)	I2C RdBk	I2C CLK	I2C Out
Video Acquisition Mode	20	Nonintrlace		VidVsyHi	VidHsyHi	Acq OddFld	Acq Field	1 Frm Acq	Start Acq
Acquisition Window Ctl	21	InvFldPol	Sel XFLD	4 : 2 : 2	InDat~Mux	EnVerScale	EnHorScale	VdOutWin	En Crop
Acquisition X-Start Lo	22	Acquisition Window X-Start Low Register							
Acquisition X-Start Hi	23							Acq Win X-Start Hi	
Acquisition Y-Start Lo	24	Acquisition Window Y-Start Low Register							
Acquisition Y-Start Hi	25							Acq Win Y-Start Hi	
Acquisition X-End Lo	26	Acquisition Window X-End Low Register							
Acquisition X-End Hi	27							Acq Win X-End Hi	
Acquisition Y-End Lo	28	Acquisition Window Y-End Low Register							
Acquisition Y-End Hi	29							Acq Win Y-End Hi	
Acq Write Address Lo	2A	Acquisition Write Address 7:0							
Acq Write Address Middle	2B	Acquisition Write Address 15:8							
Acq Write Address Hi	2C					Acquisition Write Address 19:16			
Acq Data X-Scale	2D			Acquisition X-Scaling					
Acq Data Y-Scale	2E		Acquisition Y-Scaling						
Scaling Field Adjust	2F		Scaling Field Adjust						
Input Video Start Adjust	30			Input Video Start Adjust					
Scaling Control Register	38	Fast Wrt En	(0)	(0)	Y-Max En	X-Max En	Y OvrWrt	Chroma Mux Adjust	
Display Window Control	40	VGA Clock Skew		Display Window Mux Function				EnColrKey	En XY Win
Disp Window X-Start Lo	41	Display Window X-Start Position Low							
Disp Window X-Start Hi	42						Display Window X-Start Hi		
Disp Window Y-Start Lo	43	Display Window Y-Start Position Low							
Disp Window Y-Start Hi	44							Display Y-Start Hi	
Disp Window X-End Lo	45	Display Window X-End Position Low							
Disp Window X-End Hi	46						Display Window X-End Hi		
Disp Window Y-End Hi	47	Display Window Y-End Position Low							
Disp Window Y-End Lo	48							Display Y-End Hi	
Disp Window X-Pan Lo	49	Frame Buffer A8:1 specifying starting memory column							
Disp Window Y-Pan Lo	4A	Frame Buffer A7:0 specifying starting memory row							
Disp Window Pan Hi	4B				Row A8				Col A9
Shift Clock Start Posit	4C	Shift Clock Start Position							
Disp Win Control/Zoom	4D		(0)	VGAVsyHi	VGAHsyHi	Display Y-Zoom		Display X-Zoom	
VGA Color Compare	4E	Color Value for Color Key Window							
VGA Color Mask	4F	1 = ignore bit for color compare							
Display Interlace Control	50				Repli Odd	Repli Field	Invert Field	SelExtVFld	Dsply Intrlc

Control Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	State After Reset	Page
RX	--	Index Register	--	RW	xxxxxxxx	20
R00	CPU Interface	I/O Address	00h	RW	1101110-	20
R01	CPU Interface	Memory Access	01h	RW	-0-0---0	20
R06	CPU Interface	Linear Memory Base Address	06h	RW	---11111	20
R07	CPU Interface	Data Mask, Luminance Data	07h	RW	xxxxxxxx	21
R08	CPU Interface	Data Mask, Chrominance Data	08h	RW	xxxxxxxx	21
R09	CPU Interface	Interrupt Mask	09h	RW	--RRRR00	21
R10	G.P. I/O	General Purpose I/O 0	10h	External	--------	22
R11	G.P. I/O	General Purpose I/O 1	11h	External	--------	22
R12	G.P. I/O	General Purpose I/O 2	12h	External	--------	22
R13	G.P. I/O	General Purpose I/O 3	13h	External	--------	22
R18	G.P. I/O	General Purpose I/O Control	18h	RW	00000011	22
R20	Video Acquisition	Video Acquisition Mode	20h	RW	0-000000	23
R21	Video Acquisition	Acquisition Window Control	21h	RW	xxxxxxxx	23
R22	Video Acquisition	Acquisition Window, X-start Low	22h	RW	xxxxxxxx	24
R23	Video Acquisition	Acquisition Window, X-start High	23h	RW	------xx	24
R24	Video Acquisition	Acquisition Window, Y-start Low	24h	RW	xxxxxxxx	24
R25	Video Acquisition	Acquisition Window, Y-start High	25h	RW	------xx	24
R26	Video Acquisition	Acquisition Window, X-end Low	26h	RW	xxxxxxxx	25
R27	Video Acquisition	Acquisition Window, X-end High	27h	RW	------xx	25
R28	Video Acquisition	Acquisition Window, Y-end Low	28h	RW	xxxxxxxx	25
R29	Video Acquisition	Acquisition Window, Y-end High	29h	RW	------xx	25
R2A	Video Acquisition	Acquisition Address, Low	2Ah	RW	xxxxxxxx	26
R2B	Video Acquisition	Acquisition Address, Middle	2Bh	RW	xxxxxxxx	26
R2C	Video Acquisition	Acquisition Address, High	2Ch	RW	----xxxx	26
R2D	Video Acquisition	Acquisition Horizontal Scale	2Dh	RW	--xxxxxx	27
R2E	Video Acquisition	Acquisition Vertical Scale	2Eh	RW	-xxxxxxx	27
R2F	Video Acquisition	Scaling Field Adjust	2Fh	RW	-xxxxxxx	27
R30	Video Acquisition	Input Video Start	30h	RW	--xxxxxx	27
R38	Video Acquisition	Scaling Control	38h	RW	00000000	28
R40	Display Window	Display Area Control	40h	RW	00000000	28
R41	Display Window	Window X-Start, Low	41h	RW	xxxxxxxx	29
R42	Display Window	Window X-Start, High	42h	RW	------xx	29
R43	Display Window	Window Y-Start, Low	43h	RW	xxxxxxxx	29
R44	Display Window	Window Y-Start, High	44h	RW	------xx	29
R45	Display Window	Window X-End, Low	45h	RW	xxxxxxxx	30
R46	Display Window	Window X-End, High	46h	RW	------xx	30
R47	Display Window	Window Y-End, Low	47h	RW	xxxxxxxx	30
R48	Display Window	Window Y-End, High	48h	RW	------xx	30
R49	Display Window	X-Panning, Low	49h	RW	xxxxxxxx	31
R4A	Display Window	Y-Panning, Low	4Ah	RW	xxxxxxxx	31
R4B	Display Window	X,Y-Panning, High	4Bh	RW	---x---x	31
R4C	Display Window	Shift Clock	4Ch	RW	-xxxxxxx	31
R4D	Display Window	Sync Polarity Register/Zoom	4Dh	RW	-0000000	32
R4E	Display Window	Color Compare	4Eh	RW	xxxxxxxx	32
R4F	Display Window	Color Mask	4Fh	RW	xxxxxxxx	32
R50	Display Window	Interlaced Output Control	50h	RW	---xxxxx	33
RFF	Misc	Global Enable / Version	FFh	R7: 4 W2: 0	0001-000	33

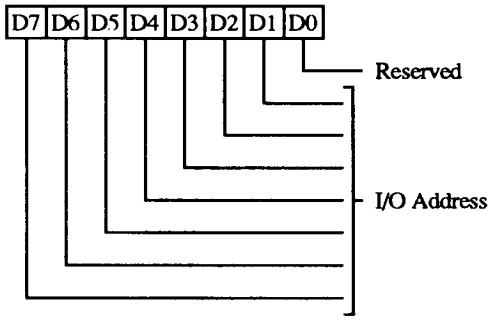
Note: Read and Write to all registers (except the Index and Global Enable Registers) is disabled until the Global Enable Bit is set. The Index and Global Enable Registers are Write only until the Global Enable Bit is set.
x = Undefined state on power-up.

INDEX REGISTER (RX)
Read/Write



7-0 Index value used to access the control registers.

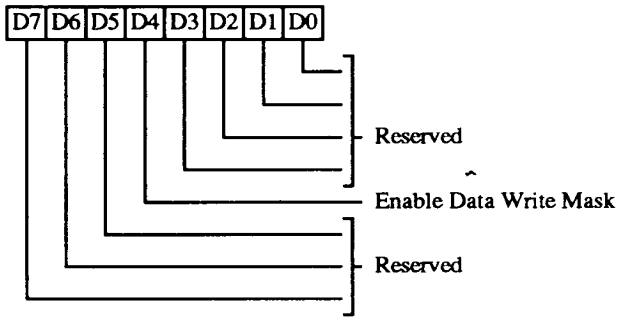
I/O ADDRESS REGISTER (R00)
Read/Write
Index 00h



0 Reserved (0)

7-1 These bits are compared with the address inputs, A7:1, to detect a valid I/O address. If CS/ is low on RESET, this register is initialized to D6h. If CS is high on RESET, this register is loaded with the value present on the data inputs (D7:1) during the first I/O write to the chip (IOWR/=0 and CS/=0).

MEMORY ACCESS REGISTER (R01)
Read/Write
Index 01h



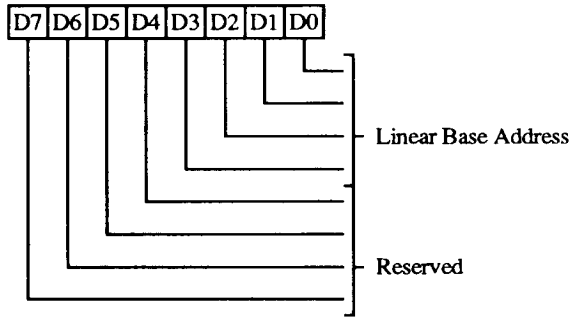
0-3 Reserved (0)

4 Enable VRAM Write Mask

0 Disabled
1 Enabled

5-7 Reserved (0)

LINEAR MEMORY BASE ADDRESS REGISTER (R06)
Read /Write
Index 06h

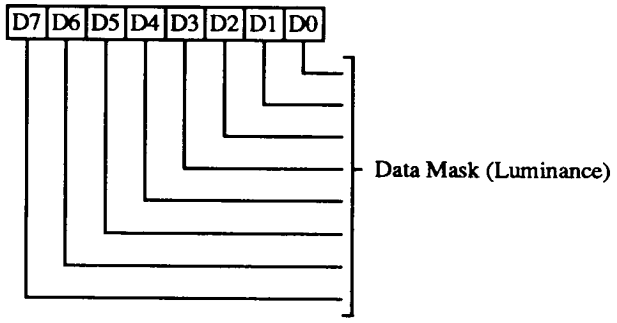


3-0 These bits define the starting address for the linear memory space. The address resolution is 1 Meg.

4-7 Reserved (Bit 4 should be set to '1')

DATA MASK REGISTER, LUMINANCE DATA (R07)

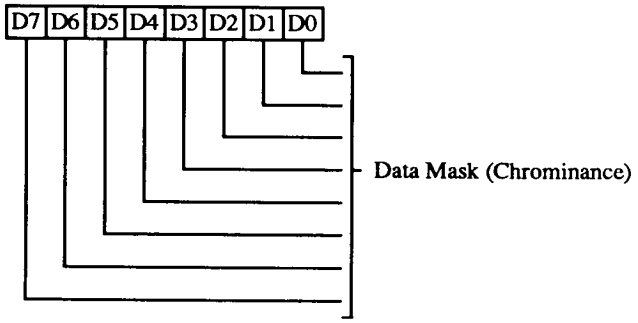
Read /Write
Index 07h



7-0 These bits control the "Write per bit" feature of the VRAMs on the luminance data. A '0' in a bit position prevents the data in that bit position from being modified during video data acquisition. This register is enabled by R01 bit-4.

DATA MASK REGISTER, CHROMINANCE DATA (R08)

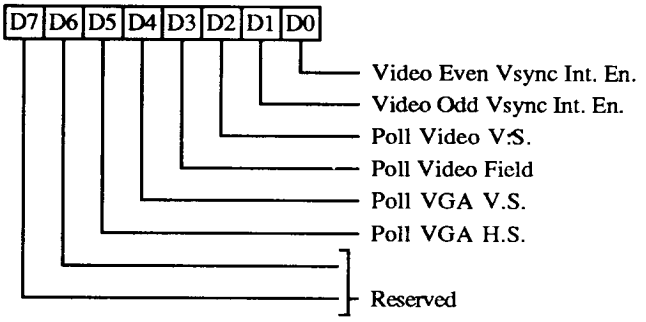
Read /Write
Index 08h



7-0 These bits control the "Write per bit" feature of the VRAMs on the chrominance data. A '0' in a bit position prevents the data in that bit position from being modified during video data acquisition. This register is enabled by R01 bit-4.

INTERRUPT MASK REGISTER (R09)

Read /Write
Index 09h



0 Video Even Vsync Interrupt Enable.

- 0 Disabled
- 1 Enabled

1 Video Odd VSync Interrupt Enable.

- 0 Disable
- 1 Enable

2-5 These bits can be polled to monitor the status of the signals listed below.

- 2 Poll Video VSync
- 3 Poll Video Field (0=Even; 1=Odd)
- 4 Poll VGA VSync
- 5 Poll VGA HSync

7-6 Reserved (0)

GENERAL PURPOSE I/O REGISTER 0 (R10)
I/O at Index 10h

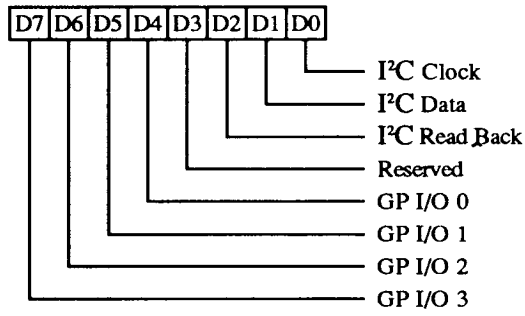
GENERAL PURPOSE I/O REGISTER 1 (R11)
I/O at Index 11h

GENERAL PURPOSE I/O REGISTER 2 (R12)
I/O at Index 12h

GENERAL PURPOSE I/O REGISTER 3 (R13)
I/O at Index 13h

These four registers are implemented through external latches and/or buffers. If enabled through the General Purpose I/O Control register, a strobe is generated on the appropriate GP I/O pin when a read or write occurs to that register. The external logic is responsible for latching the data from or driving to the system bus as needed. The data transceiver control signals are active for these I/O cycles.

GENERAL PURPOSE I/O CONTROL REGISTER (R18)
Read /Write
Index 18h



0 I²C Bus Clock

1 I²C Bus Data

Bits 0 and 1 are designed to control the I²C bus. They are connected to their respective I²C output pins. These outputs are open collector signals.

2 I²C bus read back input pin I2CI. This pin should be tied to I2CO. This bit reflects status of I2CI pin when I2CK pin goes from '0' to '1'.

3 Reserved (0)

4 General Purpose I/O 0

0 Output decode of R10 on GPIO0
1 Reserved

5 General Purpose I/O 1

0 Output "PLLHREF" on GPIO1
1 Output decode of R11 on GPIO1

6 General Purpose I/O 2

0 Output decode of R12 on GPIO2
1 Reserved

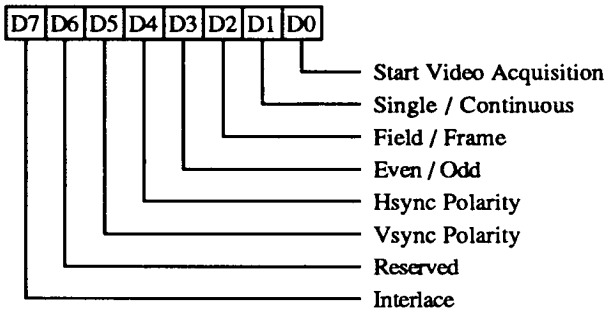
7 General Purpose I/O 3

0 Output decode of R13 on GPIO3
1 Reserved

Note: Bits 4, 6, and 7 should be programmed to 0 for correct operation.

VIDEO ACQUISITION MODE REGISTER (R20)

Read /Write
Index 20h



0 Start Video Acquisition
- 0 Stop Video Acquisition and allow CPU access to the frame buffer.
- 1 Start Video Acquisition. The type of acquisition, continuous/single frame, interlaced, etc. is determined by bits 1-3 of this register.

This bit is updated by hardware at the end of the video Vsync period. Software must read back this bit as a 0 to ensure access to the frame buffer after stopping video acquisition.

1 Single / Continuous
- 0 Continuous video acquisition
- 1 Acquire a single field or frame (as determined by bits 2&3). Bit-0 of this register is cleared at the end of a field or frame.

2 Field / Frame
- 0 Acquire input video frame
- 1 Acquire input video field (interlaced mode only)

3 Even / odd
- 0 Acquire a even (first) field
- 1 Acquire a odd (second) field

4 Hsync Polarity
- 0 Video Hsync input is active low
- 1 Video Hsync input is active high

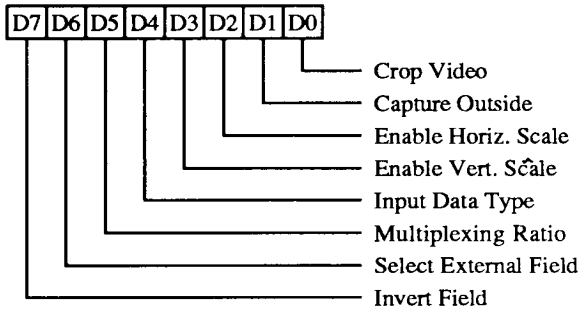
5 Vsync Polarity
- 0 Video Vsync input is active low
- 1 Video Vsync input is active high

6 Reserved (0)

7 Interlace
- 0 Input video is interlaced
- 1 Input video is non-interlaced

ACQUISITION WINDOW CONTROL REGISTER (R21)

Read /Write
Index 20h



0 Video Input Cropping
- 0 Disabled
- 1 Enabled

1 Video Capture
- 0 Capture video inside cropping window
- 1 Capture video outside cropping window

2 Video Input Scaling, Horizontal
- 0 Disabled
- 1 Enabled

3 Video Input Scaling, Vertical
- 0 Disabled
- 1 Enabled

4 Video Input Data Multiplexing. This bit determines whether input data is multiplexed or non-multiplexed, ie. YUV or RGB.
- 0 Multiplexed (YUV)
- 1 Non-multiplexed (RGB)

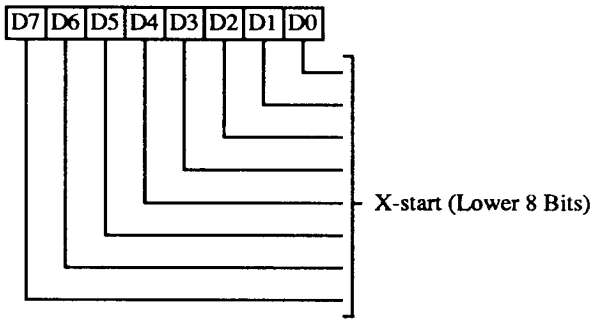
5 Multiplexing Ratio. This bit determines the multiplexing ratio for the luma and chroma input data. It is active only if bit-4 is '0'.
- 0 4:1:1 / 2:1:1
- 1 4:2:2

6 Select External Field
- 0 Internal Field. The field is detected one XCLK after the trailing edge of the XVSYNC input pin.
- 1 Field bit is input through the XFLD pin, and reclocked by XCLK before XFLD use. XFLD input should transition after the trailing edge of XVSYNC. A '0' on XFLD indicates the "even field" and '1' indicates "odd field".

7 Invert Field. Inverts the polarity of either internally or externally generated field bit.
- 0 Field bit unmodified
- 1 Field polarity inverted

ACQUISITION WINDOW, X-START LOW BYTE REGISTER (R22)

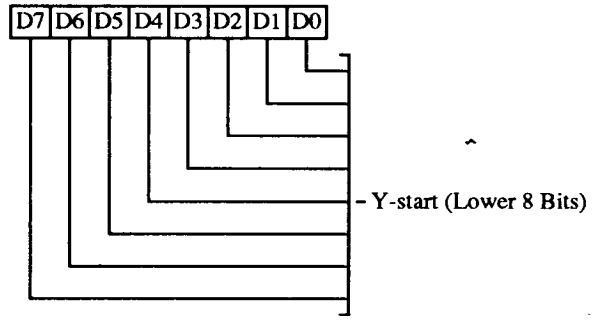
Read /Write
Index 22h



7-0 The eight low order bits of a 10-bit register. This value defines the start of the horizontal video acquisition window. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

ACQUISITION WINDOW, Y-START LOW BYTE REGISTER (R24)

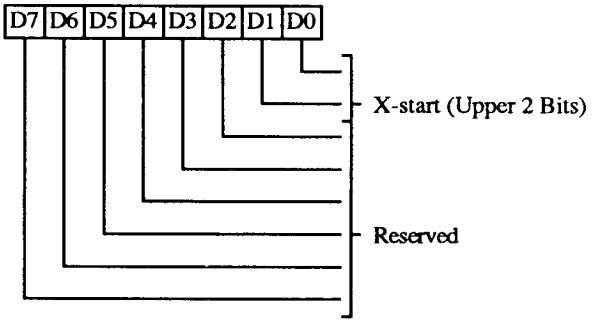
Read /Write
Index 24h



7-0 The eight low order bits of a 10-bit register. This value defines the start of the vertical video acquisition window. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

ACQUISITION WINDOW, X-START HIGH BYTE REGISTER (R23)

Read /Write
Index 23h

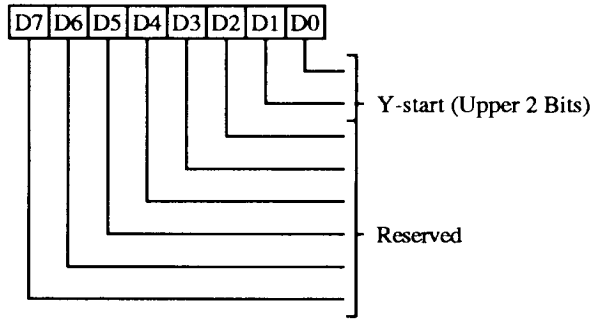


1-0 The two high order bits of a 10-bit register. This value defines the start of the horizontal video acquisition window. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

7-2 Reserved (0)

ACQUISITION WINDOW, Y-START HIGH BYTE REGISTER (R25)

Read /Write
Index 25h

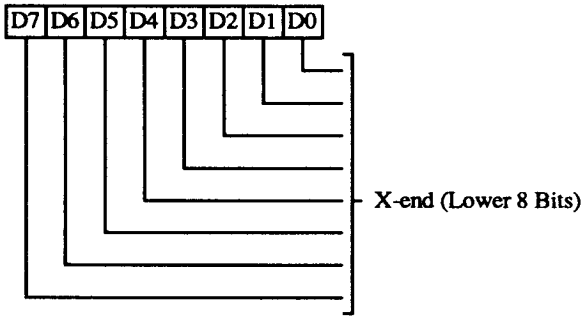


1-0 The two high order bits of a 10-bit register. This value defines the start of the vertical video acquisition window. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

7-2 Reserved (0)

ACQUISITION WINDOW, X-END LOW BYTE REGISTER (R26)

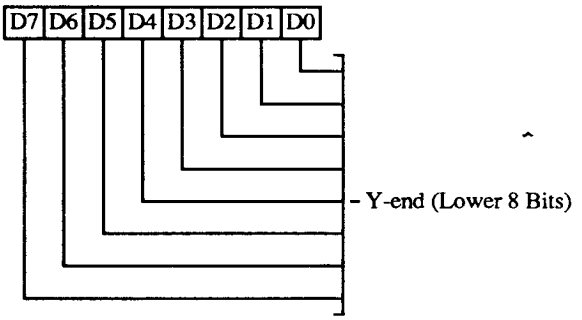
Read /Write
Index 26h



7-0 The eight low order bits of a 10-bit register. This value defines the end of the horizontal video acquisition window. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

ACQUISITION WINDOW, Y-END LOW BYTE REGISTER (R28)

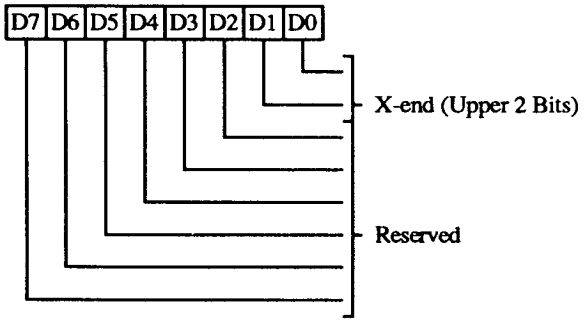
Read /Write
Index 28h



7-0 The eight low order bits of a 10-bit register. This value defines the end of the vertical video acquisition window. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

ACQUISITION WINDOW, X-END HIGH BYTE REGISTER (R27)

Read /Write
Index 27h

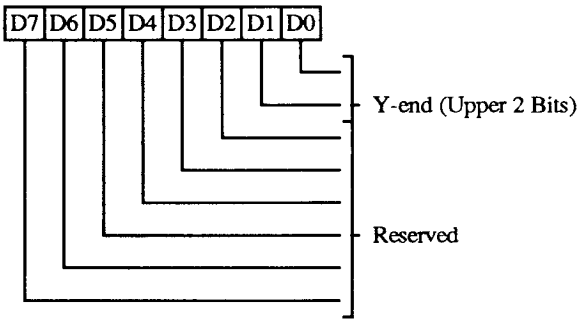


1-0 The two high order bits of a 10-bit register. This value defines the end of the horizontal video acquisition window. This value is measured in input pixel clocks and is referenced to the trailing edge of the video Hsync.

7-2 Reserved (0)

ACQUISITION WINDOW, Y-END HIGH BYTE REGISTER (R29)

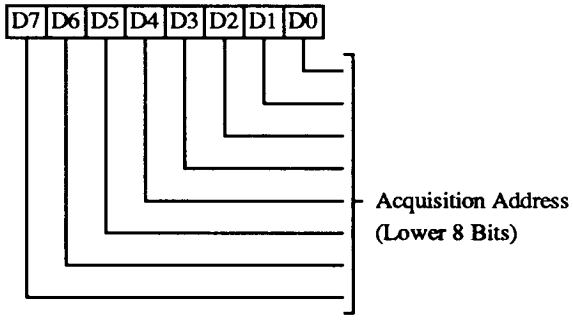
Read /Write
Index 29h



1-0 The two high order bits of a 10-bit register. This value defines the end of the vertical video acquisition window. This value is measured in input lines and is referenced to the trailing edge of the video Vsync + V Start Adjust (R30).

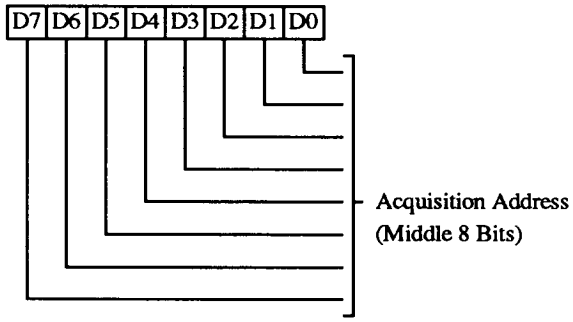
7-2 Reserved (0)

ACQUISITION ADDRESS LOW REGISTER (R2A)
Read /Write
Index 2Ah



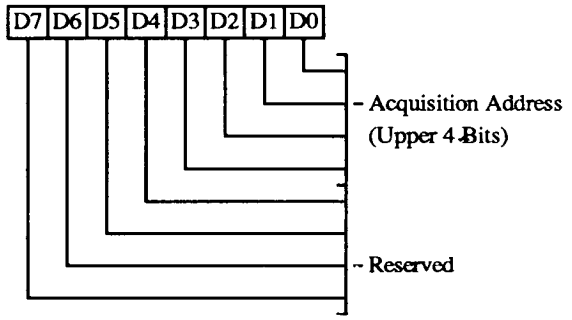
7-0 The eight low order bits of a 20-bit pointer. This value points to the frame memory location where video acquisition starts. This is a linear address. At the end of a video line, the address is reset to the beginning of the line and an offset of 1024 bytes is added to form the start address for the next line.

ACQUISITION ADDRESS MIDDLE REGISTER (R2B)
Read /Write
Index 2Bh



7-0 The eight middle bits of a 20-bit pointer. This value points to the frame memory location where video acquisition starts. This is a linear address. At the end of a video line, the address is reset to the beginning of the line and an offset of 1024 bytes is added to form the start address for the next line.

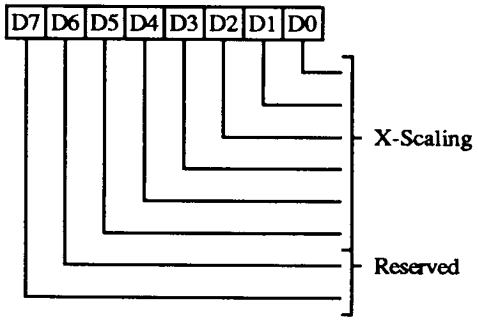
ACQUISITION ADDRESS UPPER REGISTER (R2C)
Read /Write
Index 2Ch



7-0 The four upper order bits of a 20-bit pointer. This value points to the frame memory location where video acquisition starts. This is a linear address. At the end of a video line, the address is reset to the beginning of the line and an offset of 1024 bytes is added to form the start address for the next line.

ACQUISITION HORIZONTAL-SCALING REGISTER (R2D)

Read /Write
Index 2Dh

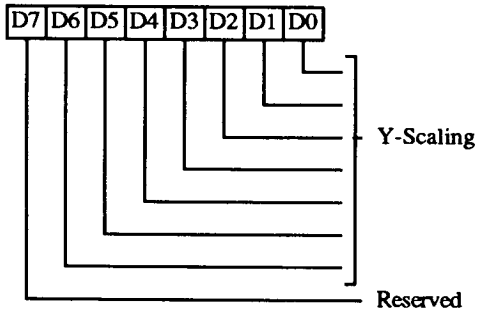


5-0 These bits define the number of pixels written per 64 input pixels. Valid values are 1-63. Horizontal scaling is disabled through R21 bit 2.

7-6 Reserved (0)

ACQUISITION VERTICAL-SCALING REGISTER (R2E)

Read /Write
Index 2Eh

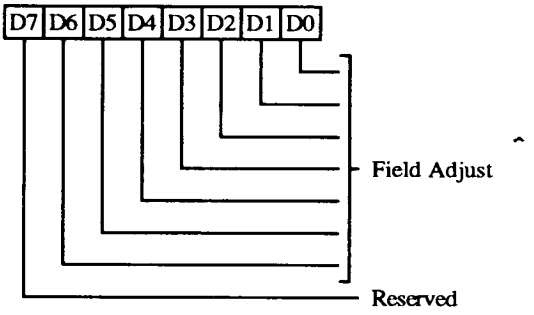


6-0 These bits define the number of lines written per 64 input lines. Valid values are 1-63. Vertical scaling is disabled through R21 bit 3.

7 Reserved (0)

SCALING FIELD ADJUST REGISTER (R2F)

Read /Write
Index 2Fh

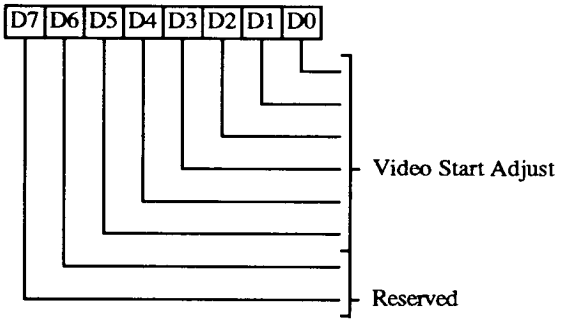


6-0 Modifies scaling value for odd field during acquisition. This is a diagnostic register and should be set to the same value as the Y-scaling register R2E for normal operation.

7 Reserved

INPUT VIDEO START ADJUST (R30)

Read /Write
Index 30h

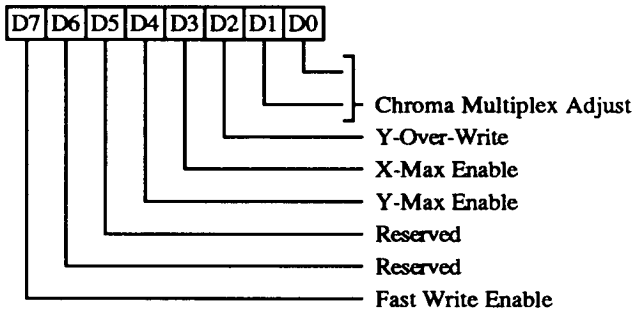


5-0 This register specifies the number of scan lines from the trailing edge of video Vsync to the start of active video frame. This register should always be programmed with a non-zero value.

7-6 Reserved

SCALING CONTROL REGISTER (R38)

Read /Write
Index 38h



1-0 Chroma Multiplex Adjust Bits. These two bits provide adjustments to maintain luma/chroma alignment.

2 Y-Over-Write Mode. This bit is used with vertical scaling of less than 1/2 to reduce the motion artifacts caused by moving images with interfield movement. When scaling by less than 1/2, both the Field Grab bit and this bit should be set to '1'. This results in writing a scaled image from only one of the video fields.

0 Normal scaling
1 Modifed scaling

3 X-Max Enable. This bit prevents wrap around of memory X-address.

0 Disabled
1 Enabled

4 Y-Max Enable. This bit prevents wrap around of memory Y-address. This bit should be enabled for PAL video data.

0 Disabled
1 Enabled

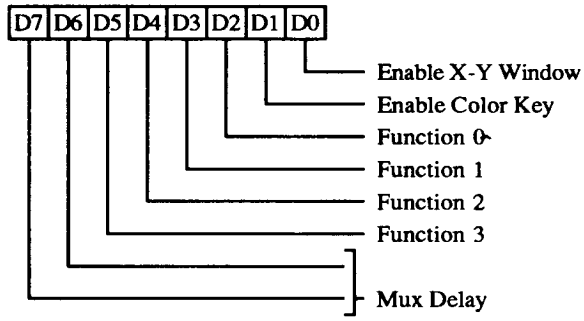
5 Reserved. Should be set to '0' for normal operation.

6 Reserved. Should be set to '0' for normal operation.

7 Fast Write Enable. When this bit is set to '1', CPURDY is asserted one clock earlier to improve the CPU memory write cycle speed. This bit defaults to '0' on RESET.

DISPLAY AREA CONTROL REGISTER (R40)

Read /Write
Index 40h



0 Overlay Window using an X-Y Window

0 Disabled
1 Enabled

1 Overlay Window using Color Keying

0 Disabled
1 Enabled

2 Non-color key or X-Y Window area (Function 0).

0 Display VGA
1 Display Frame Buffer Data

3 X-Y Window only area. (Function 1) This area does not exist if bit-0 of this register is '0'.

0 Display VGA
1 Display Frame Buffer Data

4 Color Key only area. (Function 2) This area does not exist if bit-1 of this register is '0'.

0 Display VGA
1 Display Frame Buffer Data

5 Both X-Y Window and Color Key area. (Function 3) This area does not exist if either bits 0 or 1 of this register are '0'.

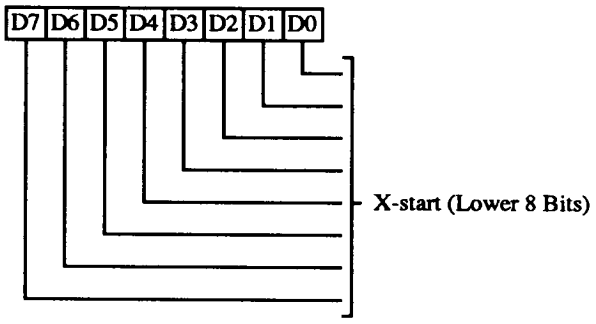
0 Display VGA
1 Display Frame Buffer Data

7-6 These bits define the skew between the VGA data input and the multiplexer control output in VGA clocks.

00 2 VGA clock delay
01 3 VGA clock delay
10 4 VGA clock delay
11 5 VGA clock delay

DISPLAY WINDOW, X-START LOW BYTE REGISTER (R41)

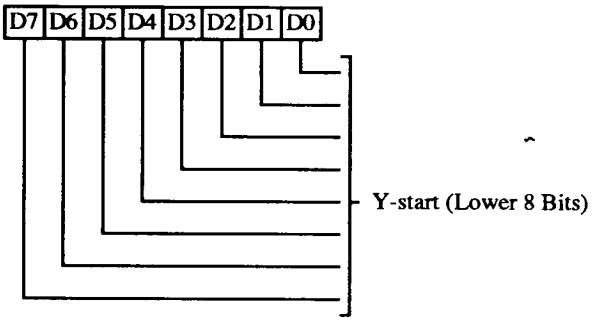
Read /Write
Index 41h



7-0 The eight low order bits of a 11-bit register. This value defines the start of the horizontal display window. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

DISPLAY WINDOW, Y-START LOW BYTE REGISTER (R43)

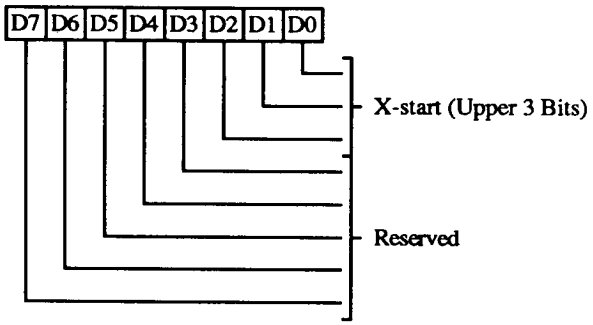
Read /Write
Index 43h



7-0 The eight low order bits of a 10-bit register. This value defines the start of the vertical display window. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

DISPLAY WINDOW, X-START HIGH BYTE REGISTER (R42)

Read /Write
Index 42h

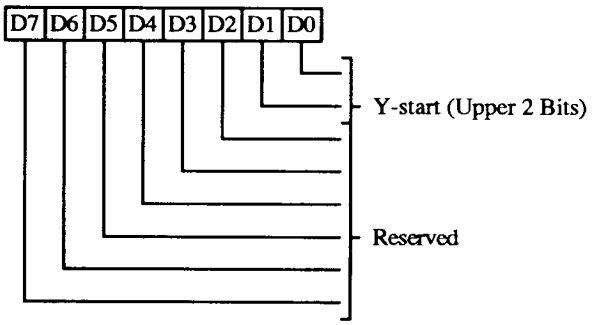


2-0 The two high order bits of a 11-bit register. This value defines the start of the horizontal display window. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

7-3 Reserved (0)

DISPLAY WINDOW, Y-START HIGH BYTE REGISTER (R44)

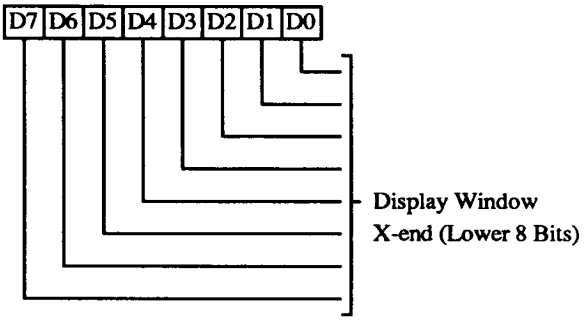
Read /Write
Index 44h



1-0 The two high order bits of a 10-bit register. This value defines the start of the vertical display window. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

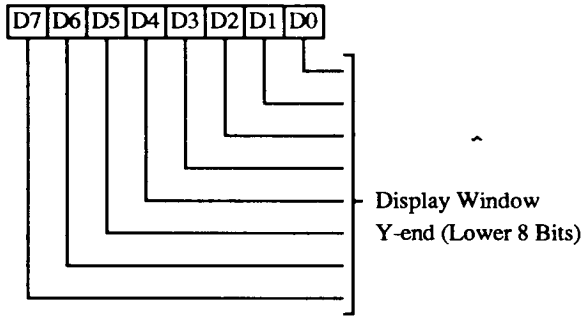
7-2 Reserved (0)

DISPLAY WINDOW,
X-END LOW BYTE REGISTER (R45)
Read /Write
Index 45h



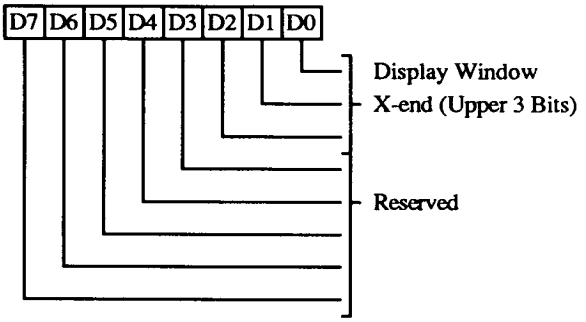
7-0 The eight low order bits of a 11-bit register. This value defines the end of the horizontal display window. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

DISPLAY WINDOW,
Y-END LOW BYTE REGISTER (R47)
Read /Write
Index 47h



7-0 The eight low order bits of a 10-bit register. This value defines the end of the vertical display window. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

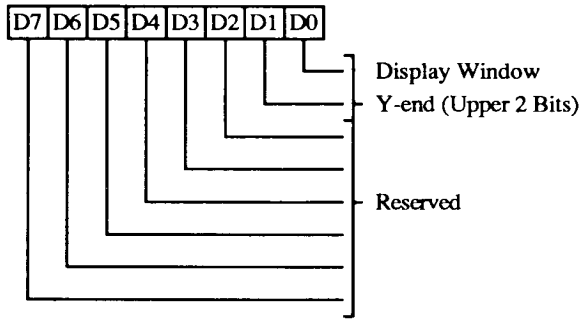
DISPLAY WINDOW,
X-END HIGH BYTE REGISTER (R46)
Read /Write
Index 46h



2-0 The two high order bits of a 11-bit register. This value defines the end of the horizontal display window. This value is measured in VGA pixel clocks and is referenced to the trailing edge of the VGA Hsync.

7-3 Reserved (0)

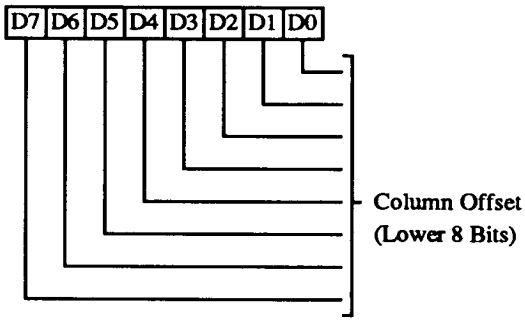
DISPLAY WINDOW,
Y-END HIGH BYTE REGISTER (R48)
Read /Write
Index 48h



1-0 The two high order bits of a 10-bit register. This value defines the end of the vertical display window. This value is measured in VGA lines and is referenced to the trailing edge of the VGA Vsync.

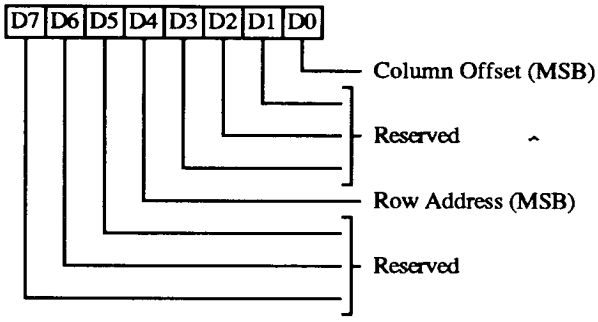
7-2 Reserved (0)

X-PANNING, LOW REGISTER (R49)
Read /Write
Index 49h



7-0 The eight low order bits of a 9-bit offset. This value defines the display buffer column address times 2 which is loaded during the data transfer cycle in the VRAMs. For 4:1:1 encoding, bit-0 of this register should be set to '0'.

X, Y - PANNING, HIGH REGISTER (R4B)
Read /Write
Index 4Bh



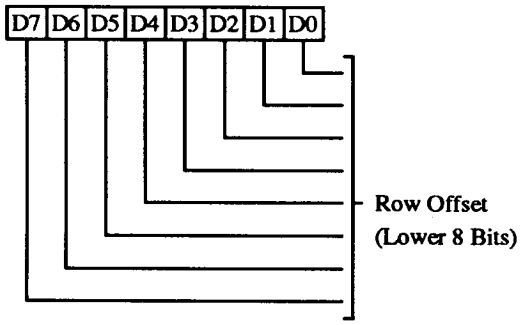
0 The MSB of the Column offset. See R49.

3-1 Reserved (0)

4 The MSB of the Row offset. See R4A.

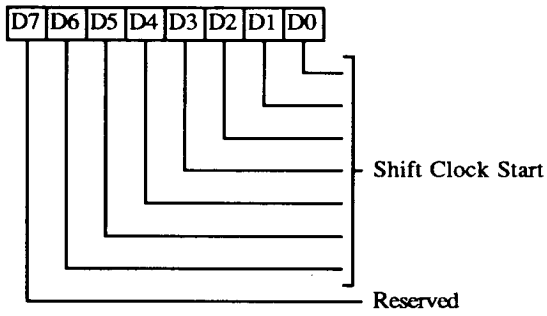
7-5 Reserved (0)

Y-PANNING, LOW REGISTER (R4A)
Read /Write
Index 4Ah



7-0 The eight low order bits of a 9-bit offset. This value defines the display buffer row which is loaded for the first active display line.

SHIFT CLOCK START REGISTER (R4C)
Read /Write
Index 4Ch

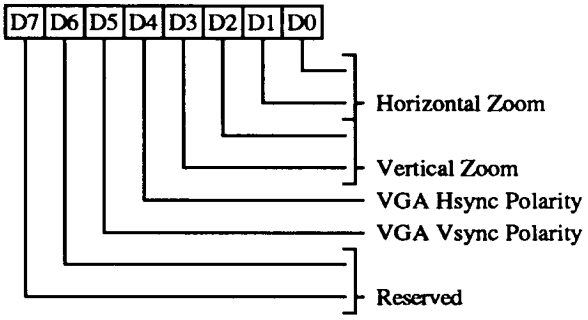


6-0 These bits define the end of the display blank relative to the VGA Hsync trailing edge. The shift clock skew is handled internally.

7 Reserved (0)

SYNC POLARITY REGISTER (R4D)

Read /Write
Index 4Dh



1-0 Horizontal Zoom

00 No Zoom
01 2X
10 4X
11 8X

3-2 Vertical Zoom

00 No Zoom
01 2X
10 4X
11 8X

4 VGA Hsync polarity

0 The VGA Hsync is active low
1 The VGA Hsync is active high

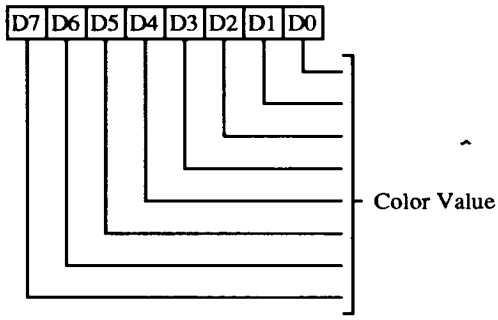
5 VGA Vsync polarity

0 The VGA Vsync is active low
1 The VGA Vsync is active high

7-6 Reserved (0)

COLOR COMPARE REGISTER (R4E)

Read /Write
Index 4Eh

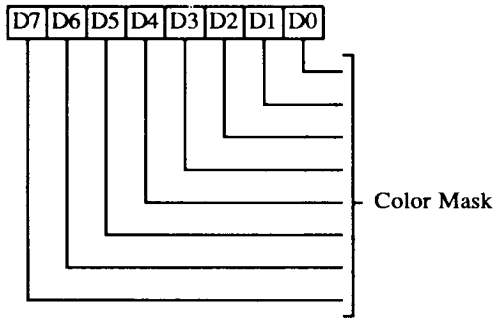


7-0 These bits define the values the VGA data must have for a color match to occur.

0 VGA data must be '0'
1 VGA data must be '1'

COLOR MASK REGISTER (R4F)

Read /Write
Index 4Fh

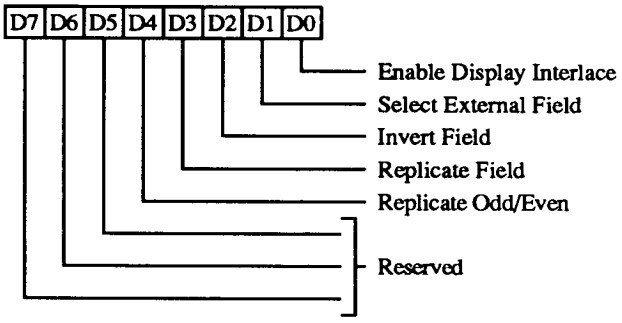


7-0 These bits define the bit position where the VGA and the color value that must match.

0 This bit position in the VGA data must match the color value.
1 This bit position in the VGA data is "don't care".

DISPLAY WINDOW INTERLACE CONTROL

Read /Write
Index 50h



0 Enable Display Interlace

- 0 Display Window is non-interlaced
- 1 Display Window is interlaced

1 Select External Field

- 0 Use internally generated field signal for display window
- 1 Select VFLD input for display window field signal

2 Invert Field

- 0 Do not modify field signal polarity
- 1 Invert display window field signal polarity

3 Replicate Field

- 0 Do not replicate field
- 1 Replicate even or odd field depending on bit-4

4 Replicate Odd/Even

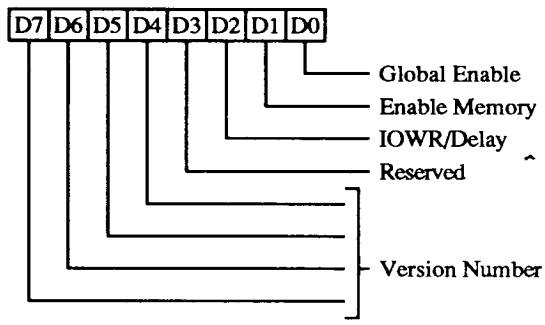
- 0 Replicate even field if bit-3 is set
- 1 Replicate odd field if bit-3 is set

7-5 Reserved (0)

Note: Bits 1-2 effective only if Bit 0 = '1'. If Bit 1 is '0' then internal logic will determine the field by sampling HSYNC level 4 PCLKs after the leading edge of VSYNC - Even field if HSYNC is low, Odd field if HSYNC is high.

CHIPS VERSION/ENABLE REGISTER (RFF)

Read /Write
Index FFh



0 PC Video Global Enable. This bit must be set for access to any other PC Video registers. This bit is not readable.

- 0 All registers, except the Index and Global Enable registers, are disabled. The Index and Global Enabled registers are write only.
- 1 All registers, including the Index and Global Enable registers, are enabled for both read and write. This bit is not readable.

1 Enable Memory. This bit is not readable.

2 IOWR/ Delay. This bit is not readable.

- 0 IOWR/ input is delayed inside chip by 2 XCLK cycles.
- 1 IOWR/ input is not delayed.

3 Reserved (0)

7-4 These bits contain the version number for PC Video. Values start at 0 and are incremented for every silicon step.

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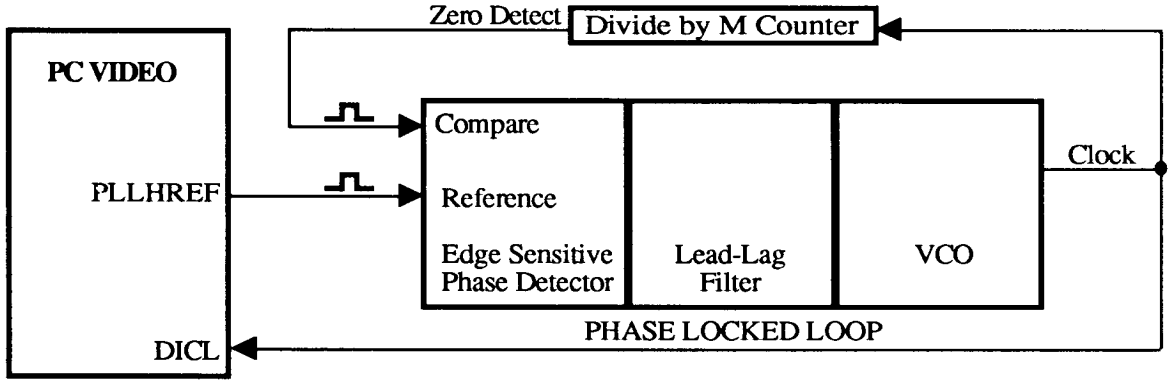
Design Considerations

Connecting PCVideo to a Phase Locked Loop

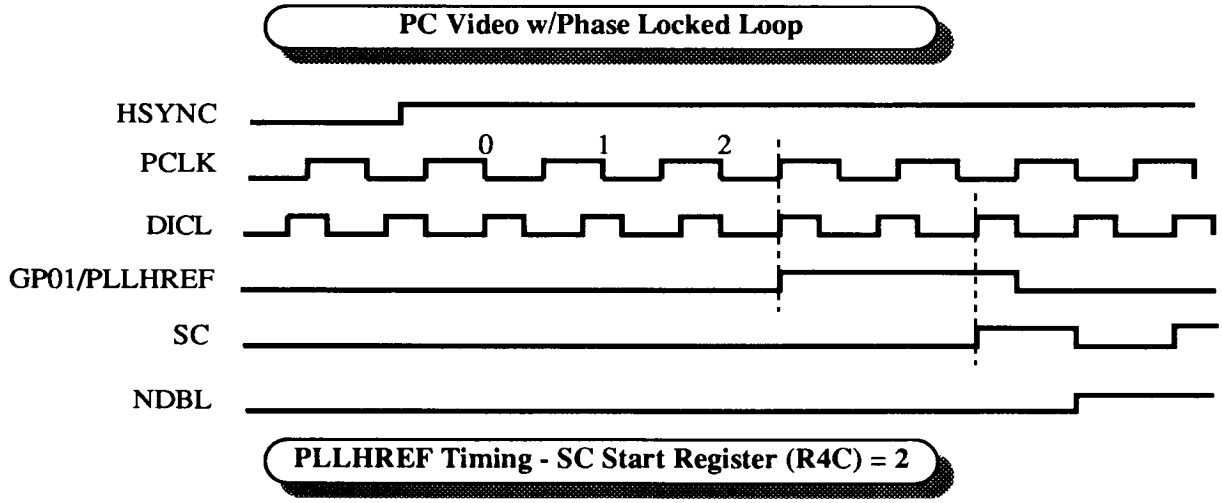
PC Video provides 4 clock inputs; XCLK, PCX2, PCLK and DICL. The XCLK clock is used to latch the input video data. PCX2 runs at twice this rate. PCLK comes from the VGA and is used to determine the position of the video window on the VGA screen. DICL (display clock) is used to output the video data inside the window. If the output video pixel is the same size as the VGA pixel, then DICL can be connected to PCLK. In some cases, however, these clocks may run at different frequencies. For example, the SAA9051 DMSD chip will generate 720 horizontal pixels. To fit 720 horizontal pixels on a 640 by 480 VGA screen, DICL should run 720/640 faster than PCLK and must be phase locked to PCLK. The block diagram below shows a method of generating the DICL clock.

PLLHREF Timing

After the trailing edge of VGA HSync, the value in the SC Start register (R4C) will be counted down and then a positive pulse will be output on the PLLHREF/GP01 pin. This output is used as the horizontal reference in the Phase Locked Loop. One DICL clock later, the SC output will start the shifting of data out of the VRAMs. The timing relationships between these signals is shown below. DICL Rising Edge should come before or coincident with PCLK. If DICL rises after PCLK, the SC timing may change.



Note: $F_{DICL} = F_{PCLK} \times M / (\text{Total number of VGA\_Pixels\_Active} + \text{VGA\_Pixels\_Blank})$



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Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1	W
V_{CC}	Supply Voltage	–0.5	7	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	85	°C
T_{STG}	Storage Temperature	–40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Ambient Temperature	0	55	°C

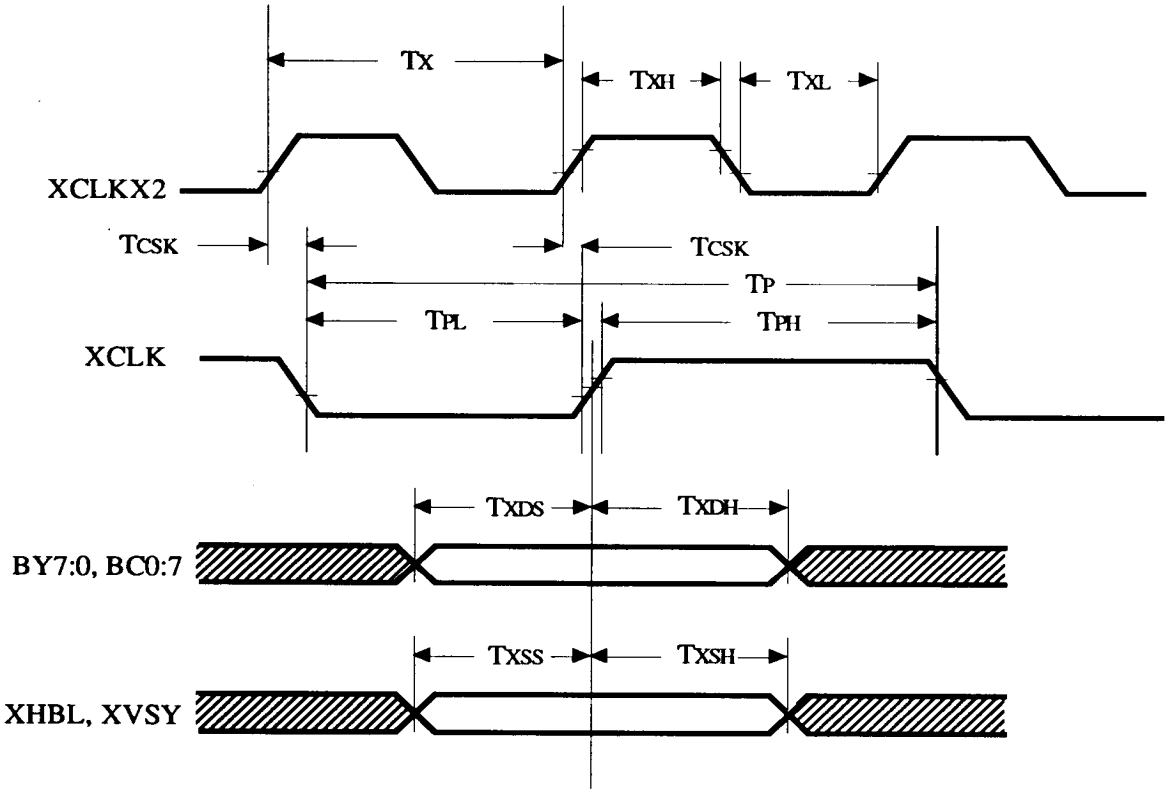
DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	@27 MHz CLK, 0°C, 5.25V	–	100	mA
I_{IL}	Input Leakage Current		–10	+10	uA
I_{OZ}	Output Leakage Current	High Impedance	–10	+10	uA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL}=18mA (RDY, MEMCS16/)	–	0.45	V
		I_{OL} = 13.5 mA (I2CK, I2CO)	–	0.45	V
		I_{OL} = 9 mA (all other signals)	–	0.45	V
V_{OH}	Output High Voltage	I_{OH}=10mA (RDY, MEMSC16/)	2.4	–	V
V_{OH}	Output High Voltage	I_{OH} = 5.0 mA (all other signals)	2.4	–	V

AC TIMING CHARACTERISTICS - INPUT VIDEO TIMING

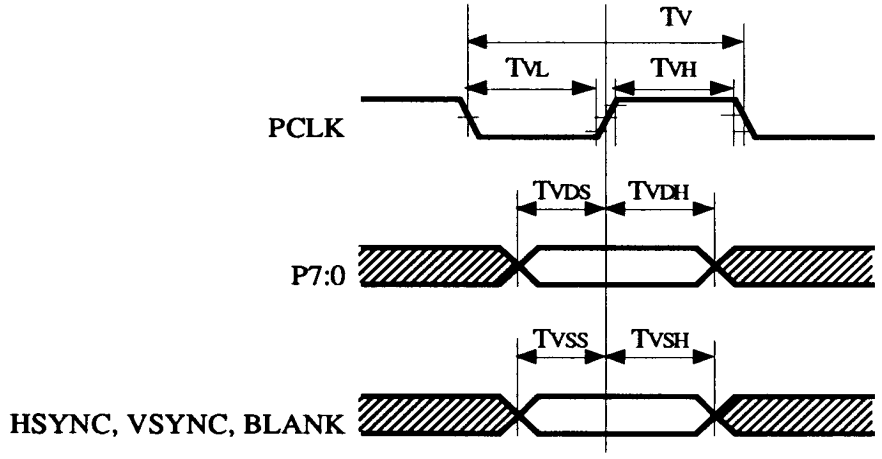
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_P	XCLK Period	13.5 MHz Typ	66	74	80	nS
T_{PH}	XCLK High Time		$0.45T_P$	–	$0.55T_P$	nS
T_{PL}	XCLK Low Time		$0.45T_P$	–	$0.55T_P$	nS
T_X	PCX2 Period	27.0 MHz Typ	T_P / 2	37	T_P / 2	nS
T_{XH}	PCX2 High Time		$0.45T_X$	–	$0.55T_X$	nS
T_{XL}	PCX2 Low Time		$0.45T_X$	–	$0.55T_X$	nS
T_{XSS}	XVSY, XHBL setup to XCLK rising edge		12	–	–	nS
T_{XSH}	XVSY, XHBL hold from XCLK rising edge		0	–	–	nS
T_{XDS}	BY 7:0, BC 7:0 setup to XCLK rising edge		10	–	–	nS
T_{XDH}	BY 7:0, BC 7:0 setup to XCLK rising edge		0	–	–	nS
T_{CSK}	PCX2 to XCLK skew required		0	–	10	nS
T_{RST}	Reset Pulse Width		$64T_X$	–	–	nS



PC Video Input Video Timing

AC TIMING CHARACTERISTICS - VGA INPUT TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_V	PCLK Period	–	–	45	Mhz
T_{VH}	PCLK High Time	$0.45T_V$	–	$0.55T_V$	nS
T_{VL}	PCLK Low Time	$0.45T_V$	–	$0.55T_V$	nS
T_{VSS}	HSYNC, VSYNC, BLANK setup to PCLK rising edge	2	–	–	nS
T_{VSH}	HSYNC, VSYNC, BLANK hold from PCLK rising edge	3	–	–	nS
T_{VDS}	P7:0 setup to PCLK rising edge	2	–	–	nS
T_{VDH}	P7:0 hold from PCLK rising edge	4	–	–	nS
F vhmax	Maximum VGA HYSNC rate for stable NTSC Source	–	–	48	kHz
F vhmax	Maximum VGA HSYNC rate for stable PAL Source	–	–	47	kHz

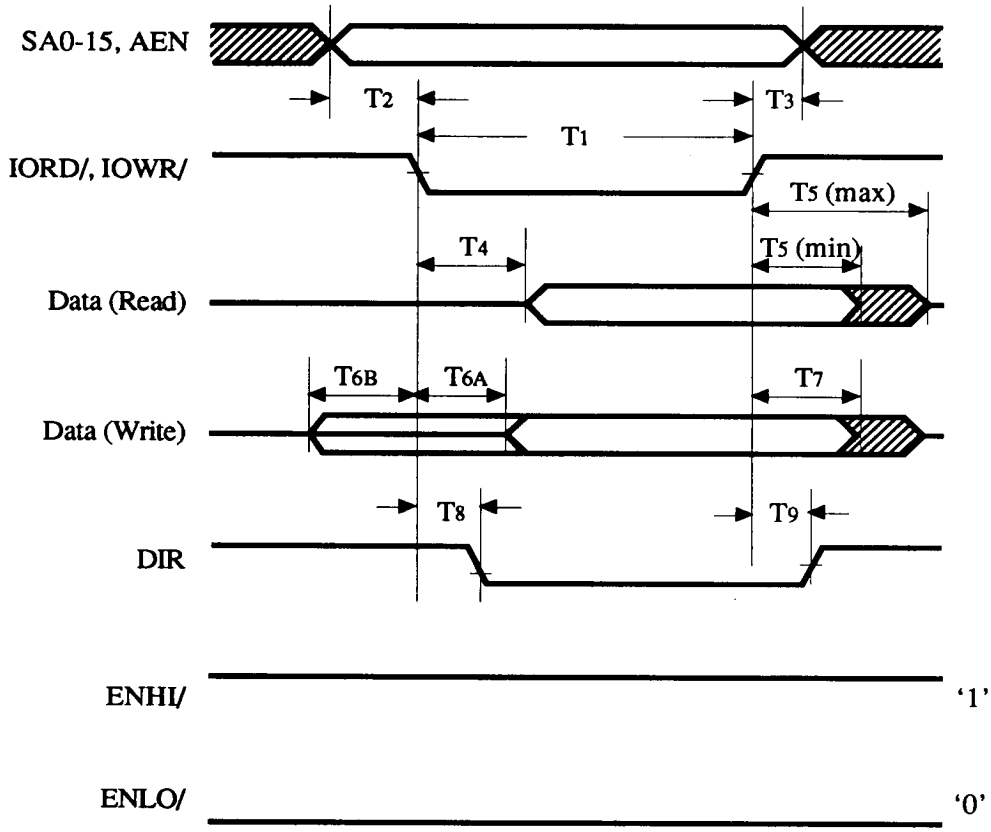


PC Video VGA Input Timing

TIMING CHARACTERISTICS - ISA BUS I/O TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{1A}	IORD/, IOWR/ Pulse Width, Reg FF Bit 2 = '0'	Note 1	2Tp + 20ns	–	–	nS
T_{1B}	IORD/, IOWR/ Pulse Width, Reg FF Bit 2 = '1'	Note 1	175	–	–	nS
T_2	Address setup to IORD, IOWR/		90	–	–	nS
T_3	Address hold from IORD, IOWR/		0	–	–	nS
T_4	I/O Read Data Delay from IORD/		–	–	50	nS
T_5	I/O Read Data hold from IORD/		0	–	30	nS
T_{6A}	I/O Write Data setup to IOWR/ Reg FF Bit 2='0'	Note 1	2Tp	–	–	nS
T_{6B}	I/O Write Data setup to IOWR/ Reg FF Bit 2='1'	Note 1	22	–	–	nS
T_7	I/O Write Data hold from IOWR/		0	–	–	nS
T_8	IORD/ falling to DIR valid		–	–	10	nS
T_9	IORD/ rising to DIR invalid		–	–	10	nS

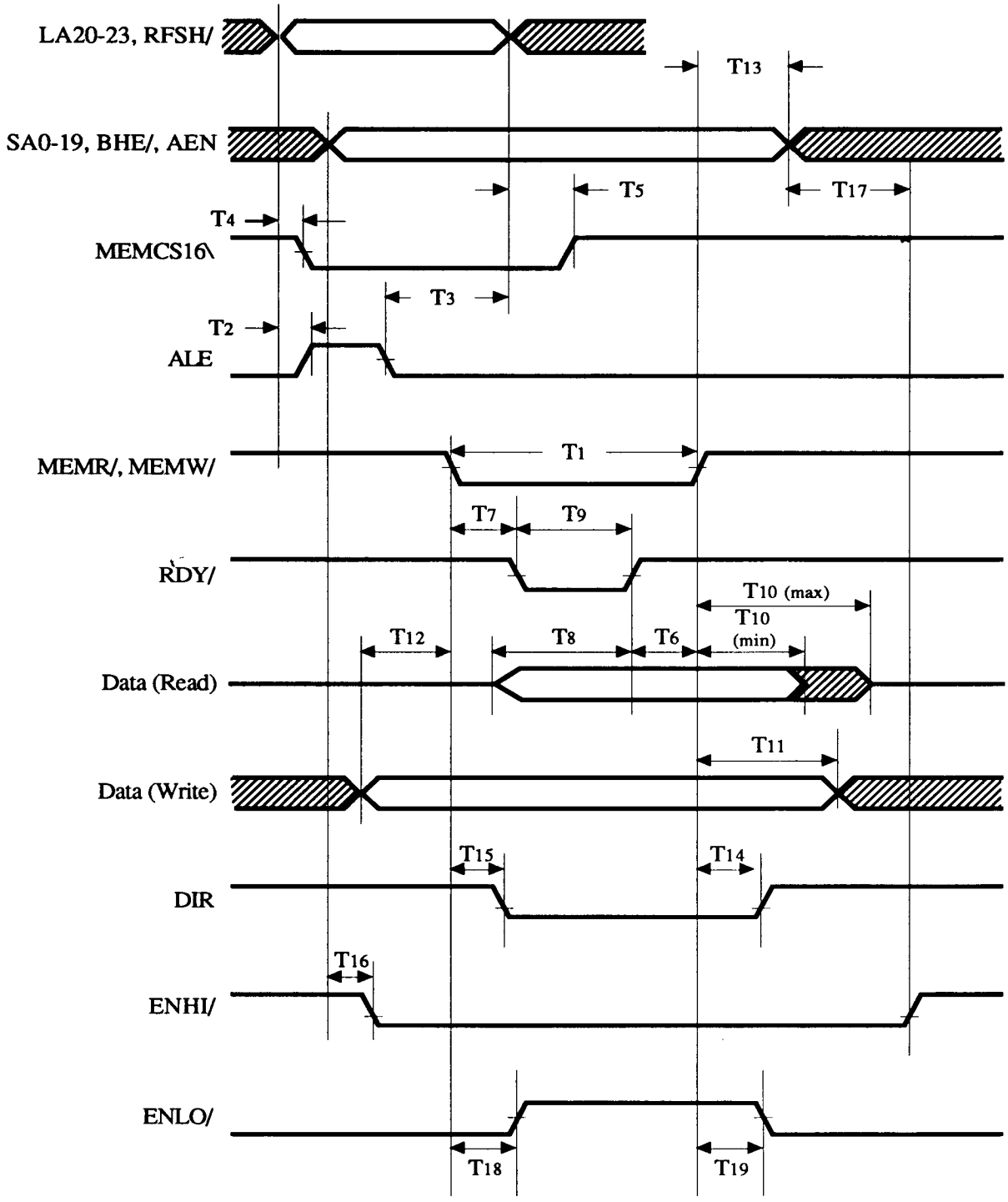
Note 1: See Register FF description



ISA Bus I/O Cycle Timing

AC TIMING CHARACTERISTICS - ISA BUS TIMING

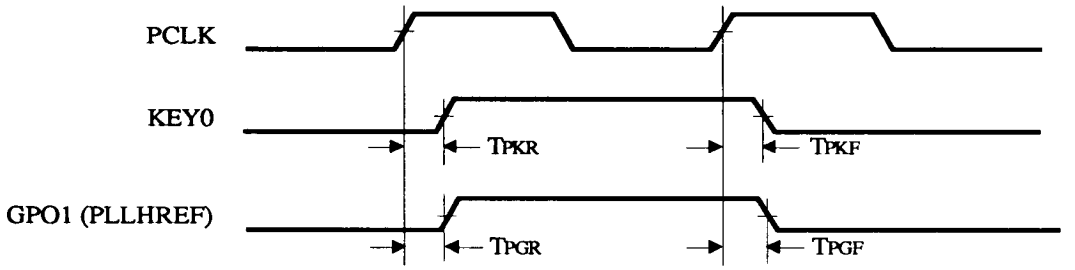
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_1	MEMR/, MEMW/ Pulse Width		175	–	–	nS
T_2	Address setup to ALE		20	–	–	nS
T_3	Address hold from ALE		0	–	–	nS
T_6	MEMR/, MEMW/ hold from RDY (Memory)		0	–	–	nS
T_{10}	Memory Read Data Hold from MEMR/		10	–	35	nS
T_{11}	Memory Write Data Hold from MEMR/		0	–	–	nS
T_7	MEMR/, MEMW/ to RDY Low Delay		-	–	25	nS
T_8	Memory Read Data setup to RDY		25	–	–	nS
T_9	RDY width		8 T_X	–	24 T_X	nS
T_4	LA valid to MEMCS16 Low Delay		–	–	20	nS
T_5	LA invalid to MEMCS16 High Delay		–	–	20	nS
T_{12}	Memory Write Data Setup to MEMW/		-40	–	–	nS
T_{13}	SA Hold from MEmr/, MEMW/		20	–	–	nS
T_{14}	MEMR/ falling to DIR valid		–	–	10	nS
T_{15}	MEMR/ rising to DIR invalid		–	–	10	nS
T_{16}	BHE falling to ENHI/ valid		–	–	10	nS
T_{17}	BHE rising to ENHI/ invalid		–	–	10	nS
T_{18}	MEMR/, MEMW/ to ENLO/ valid		–	–	10	nS
T_{19}	MEMR/, MEMW/ to ENLO/ invalid		–	–	10	nS



ISA Bus Timing

AC TIMING CHARACTERISTICS - VGA PIXEL CLOCK TO KEYO TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{PKR}	PCLK to KEYO Rising Delay		–	–	13	nS
T_{PKF}	PCLK to KEYO Falling Delay		–	–	17	nS
T_{PGR}	PCLK to GPO1 (PLLHREF) Rising Delay		–	–	10	nS
T_{PGF}	PCLK to GPO1 (PLLHREF) Falling Delay		–	–	9	nS

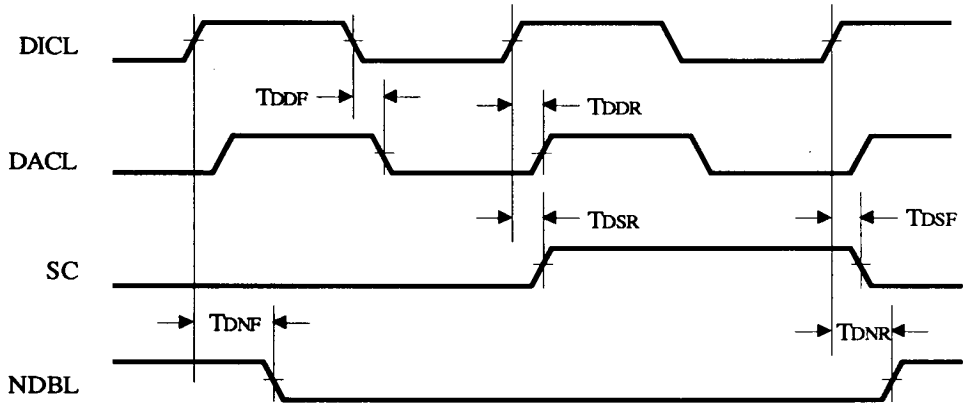


VGA Pixel KEYO (Analog Mux Control Timing)

AC TIMING CHARACTERISTICS - DISPLAY CLOCK TO DAC CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{DDR}	DICL to DACL Rising Delay		–	–	12	nS
T_{DDF}	DICL to DACL Falling Delay		–	–	12	nS
T_{DSR}	DICL to SC Rising Delay		–	–	14	nS
T_{DSF}	DICL to SC Falling Delay		–	–	14	nS
T_{DNR}	DICL to NDBL Rising		–	–	25	nS
T_{DNF}	DICL to NDBL Falling		–	–	25	nS

Note: All max values will increase by 2nS if horizontal zoom is enabled.



DISPLAY Clock to DAC Clock, DAC Blank and VRAM Shift Clock Timing

AC TIMING CHARACTERISTICS - MEMORY CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_X	PCX2 (Note 1)	Note 1	–	T_P / 2	–	nS

Note 1: The 2 x Video Pixel Clock (PCX2) is used for memory timing. PCX2 is equal to twice the pixel input clock (XCLK). This clock is also used to generate timing for the random access port. DICL is used to generate the Shift Clock (SC).

PC Video AC TIMING CHARACTERISTICS - VRAM ACCESS REQUIREMENTS

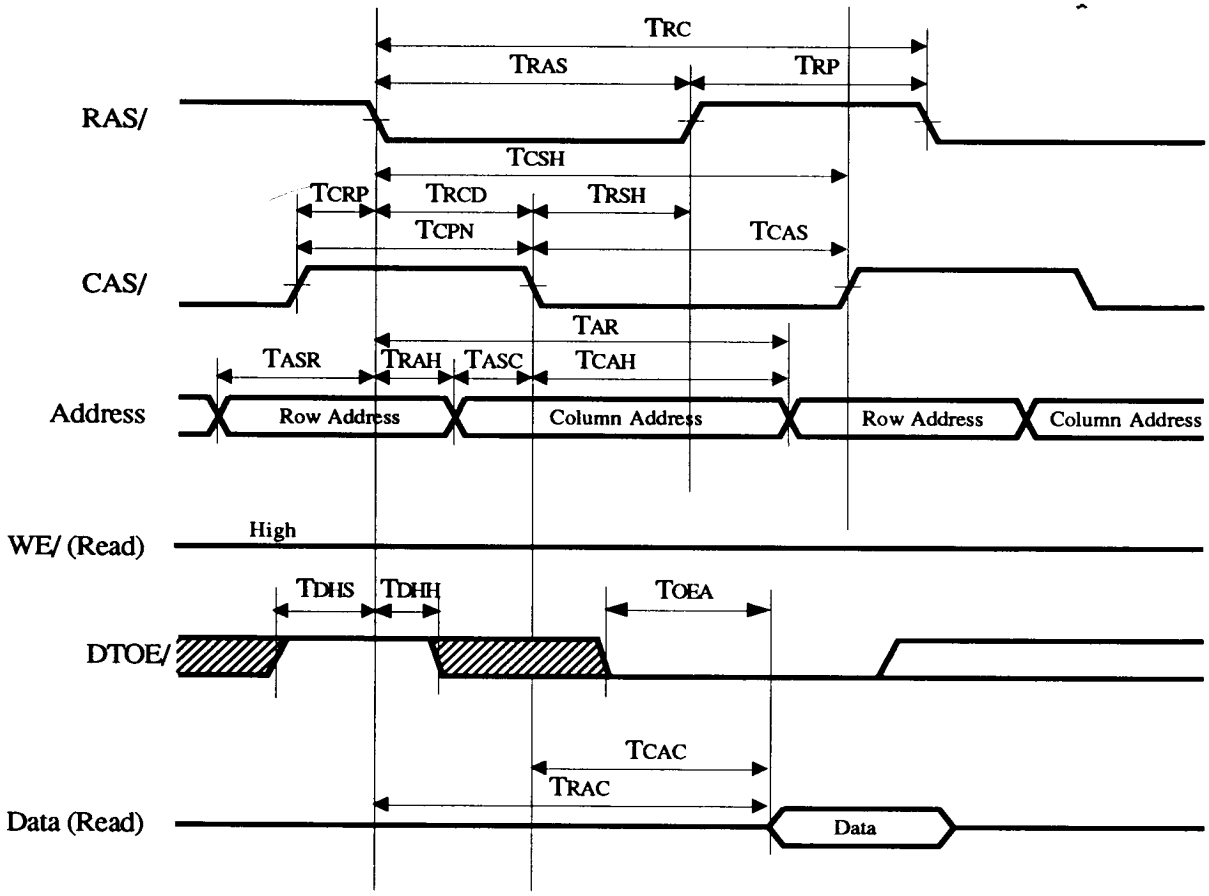
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RAC}	Data Access Time from RAS/		–	–	4 T_X	nS
T_{CAC}	Data Access Time from CAS/		–	–	T_X	nS

TIMING CHARACTERISTICS - VRAM TIMING

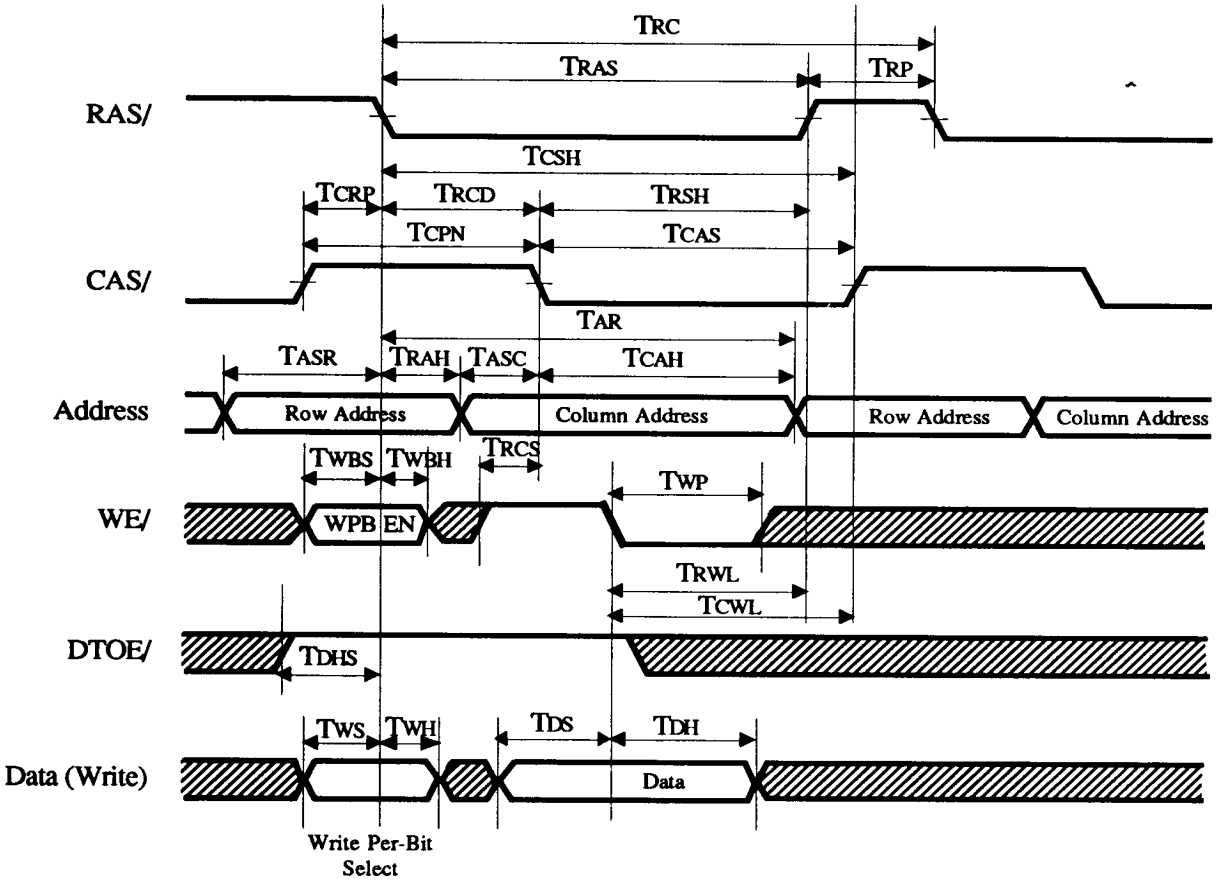
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RC}	Random read or write cycle time		$7T_X$	–	–	nS
T_{PC}	Fast-page cycle time		$4T_X$	–	–	nS
T_{RP}	RAS/ precharge		$3T_X$	–	–	nS
T_{RAS}	RAS/ pulse width		$4T_X$	–	–	nS
T_{RASP}	Fast-page RAS/ pulse width		$4T_X$	–	–	nS
T_{RSH}	RAS/ hold from CAS/		$2T_X$	–	–	nS
T_{CPN}	CAS/ precharge		$4T_X$	–	–	nS
T_{CP}	Fast-page CAS/ precharge time		$1T_X$	–	–	nS
T_{CAS}	CAS/ pulse width		$3T_X$	–	–	nS
T_{CAS1}	CAS/ pulse width (Fast Page Cycle)		$3T_X$	–	–	nS
T_{CAS2}	CAS/ pulse width (Fast Page Cycle)		$3T_X$	–	–	nS
T_{CSH}	CAS/ hold from RAS/		$5T_X$	–	–	nS
T_{RCD}	RAS/ to CAS/ delay		$1T_X$	–	–	nS
T_{CRP}	CAS/ high to RAS/ low precharge		$3T_X$	–	–	nS
T_{ASR}	Row Address setup time		$2T_X$	–	–	nS
T_{RAH}	Row Address hold time		$1T_X$	–	–	nS
T_{ASC}	Column Address setup to CAS/		$1T_X$	–	–	nS
T_{CAH}	Column Address hold time		$2T_X$	–	–	nS
T_{RAD}	RAS/ to Column Address delay time		$1T_X$	–	–	nS
T_{RAL}	Column Address to RAS/ lead time		$3T_X$	–	–	nS
T_{RCS}	Read command setup time		$5T_X$	–	–	nS
T_{WP1}	Write command pulse width(Fast Page Cycle)		$2T_X$	–	–	nS

AC TIMING CHARACTERISTICS - VRAM TIMING (Continued)

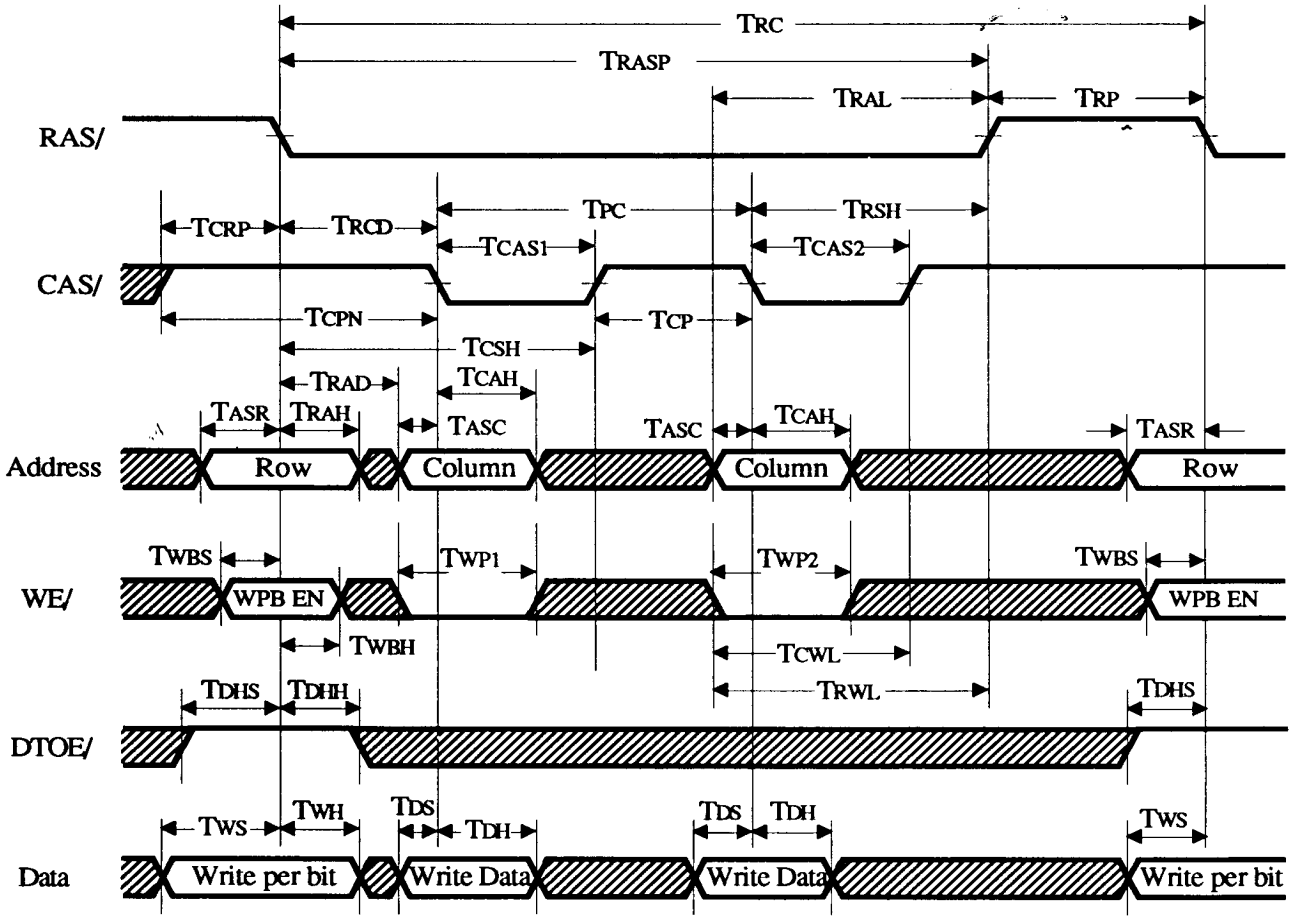
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{WP2}	Write command pulse width(Fast Page Cycle)		2 T_X	–	–	nS
T_{WP}	Write command pulse width		3 T_X	–	–	nS
T_{RWL}	Write command to RAS/ lead time		2 T_X	–	–	nS
T_{CWL}	Write command to CAS/ lead time		2 T_X	–	–	nS
T_{DS}	Data-in setup time		0.5 T_X	–	–	nS
T_{DH}	Data-in hold time		1 T_X	–	–	nS
T_{RPC}	RAS/ high to CAS/ low precharge time		5T_X	–	–	nS
T_{DLS}	DT/ low setup time		1 T_X	–	–	nS
T_{RDH}	DT/ low hold time after RAS/ low		3 T_X	–	–	nS
T_{CDH}	DT/ low hold time after CAS/ low		1 T_X	–	–	nS
T_{DHS}	DT/ high setup time		1 T_X	–	–	nS
T_{DHH}	DT/ high hold time		1 T_X	–	–	nS
T_{DTR}	DT/ high to RAS/ high delay		0	–	–	nS
T_{DTC}	DT/ high to CAS/ high delay		1 T_X	–	–	nS
T_{WBS}	Write-per-bit setup time		0.5 T_X	–	–	nS
T_{WBH}	Write-per-bit hold time		1 T_X	–	–	nS
T_{WS}	Write bit selection setup time		0.5 T_X	–	–	nS
T_{WH}	Write bit selection hold time		1 T_X	–	–	nS
T_{DTH}	DT/ high hold time after RAS/ high		2 T_X	–	–	nS



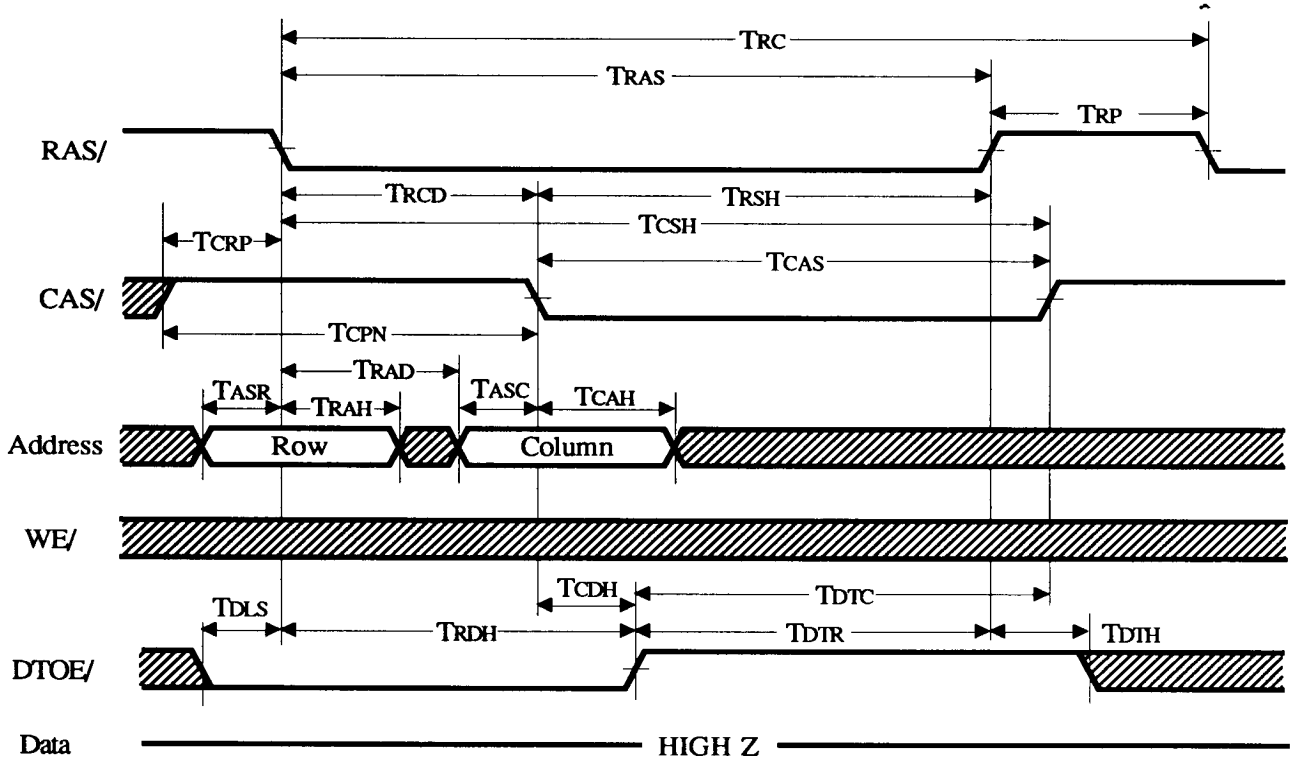
VRAM Random Read Cycle Timing



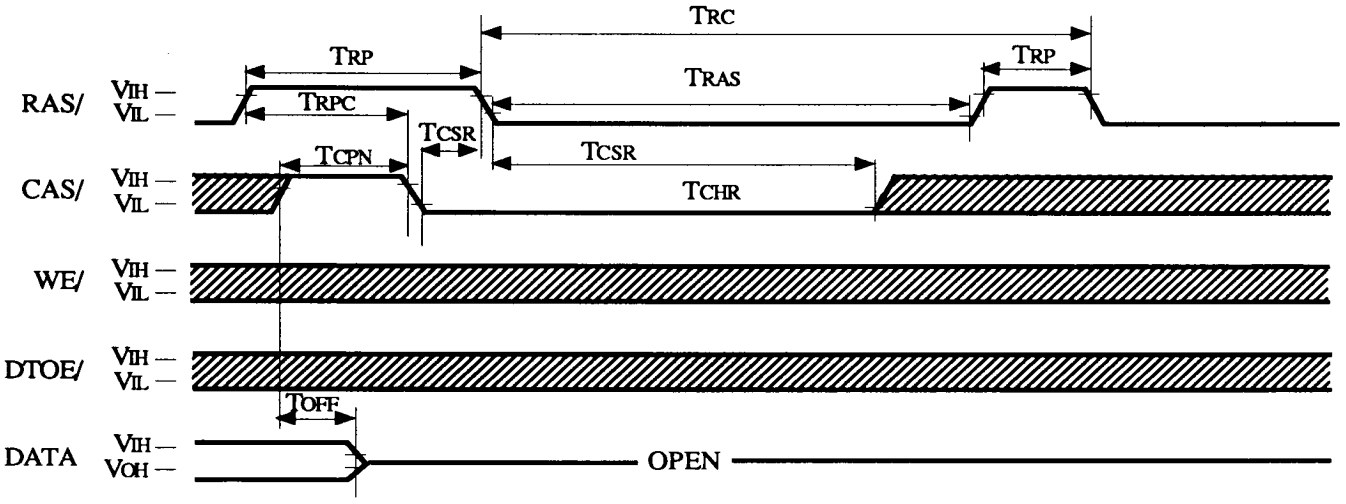
VRAM Random Write Cycle Timing



VRAM Fast-page Write Cycle Timing



VRAM Data Transfer Cycle Timing



VRAM Refresh Cycle Timing

Mechanical Specifications