National Semiconductor

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F9450 High-Performance 16-Bit Bipolar Microprocessor

General Description

The National F9450 microprocessor is the nucleus of a family of high-performance devices intended for commercial and military applications requiring sophisticated, high-speed, real-time processing. It has, on-chip, all of the functions necessary to perform floating-point operations without the use of a coprocessor. Other on-chip capabilities allow addressing of up to 2M words of memory and, with the addition of the optional F9451 Memory Management Unit (MMU), up to 16M words of memory.

Real-time processing is achieved through advanced architecture that incorporates two programmable timers, user-accessible general-purpose registers, a complete 16-level interrupt processor, and a comprehensive fault handler on the chip. Multiprocessing is supported by a flexible bus arbitration scheme, as well as process synchronization (test and set) instructions.

The F9450 instruction set is optimized for complex real-time applications. It implements the complete MIL-STD-1750A instruction set architecture (ISA) and its floating-point standard on a single chip.

The F9450 family of support circuits and systems provides additional capabilities, including memory-mapped expansion with the F9451 MMU.

Comprehensive software support for the F9450, including assemblers, loaders, simulators, and compilers, is provided by National and other sources. Software development for the F9450 can be performed using the VAX-11/7XX™ computers using the VMS™ operating system.

For complete information on available support circuits and software, contact your local National Sales Office or the Microcontroller Division.

Features

- Single-chip 16-bit microprocessor with 32- and 48-bit floating-point arithmetic on-chip
- Real-time processing: Two programmable timers, 16 levels of vectored interrupt
- Address space of up to 2M words, expandable to 16M words with optional F9451
- Instruction set optimized for real-time applications (MIL-STD-1750A ISA)
- Built-in self-test, fault handling, and abort
- Twenty-four user-accessible registers
- Built-in multiprocessor capabilities
- Single- and double-precision integer arithmetic
- Built-in console operations
- Complete high-level language and design development support available
- Static operation with single clock: 0 MHz–20 MHz
- TTL inputs and outputs with 8 mA drive capability
- Small size 64-pin DIP or surface-mount packages
- Full performance over −55°C to +125°C operating temperature range
- Bipolar I^3L® technology

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 TL/DD/10103

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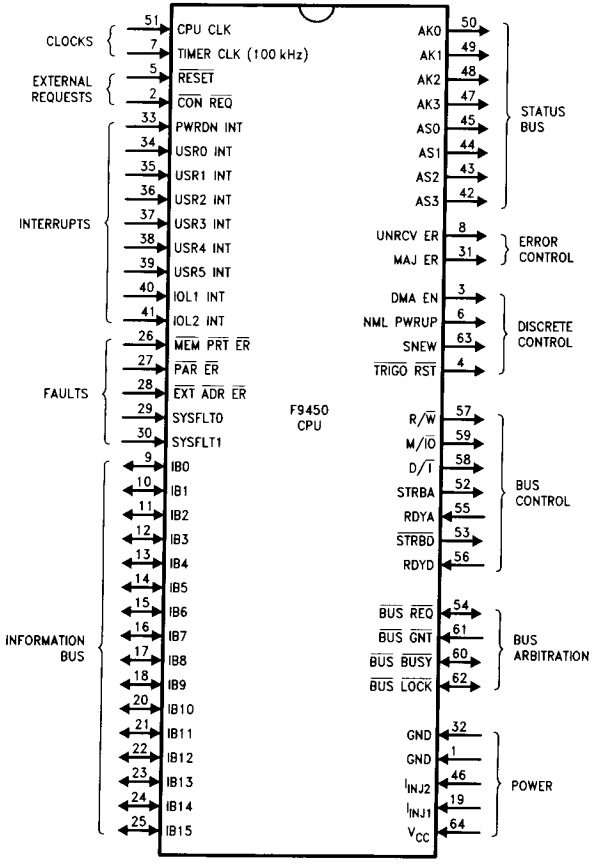

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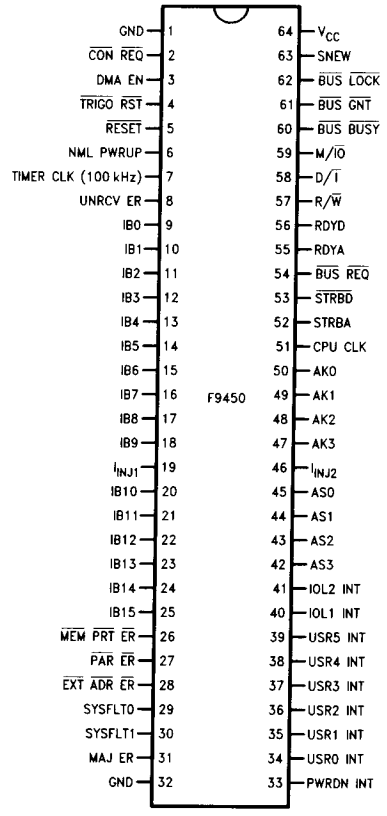
Connection Diagram



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F9450 System Architecture

The F9450 instruction set has been designed for demanding real-time applications. Such operations as single- and double-precision integer arithmetic, including multiply and divide, floating-point arithmetic, bit operations, fault and error handling, interrupt processing, and direct memory access (DMA) are available. Memory management and protection can be accomplished using the F9451 MMU peripheral. Console commands permit direct interaction with the user.

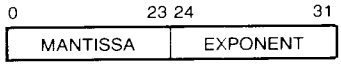
Data Types

The F9450 processes six data types:

— Bits
— Bytes (8 bits)
— Words (16 bits)
— Double words (32 bits)
— Single-precision floating-point numbers (32 bits)
— Extended-precision floating-point numbers (48 bits)

The floating-point numbers are represented by a fractional-twos-complement mantissa (24 bits for single-precision and 40 bits for extended-precision) and an 8-bit twos-complement exponent, as shown in *Figure 1*. These floating-point data formats are specified by MIL-STD-1750A.

Single Precision



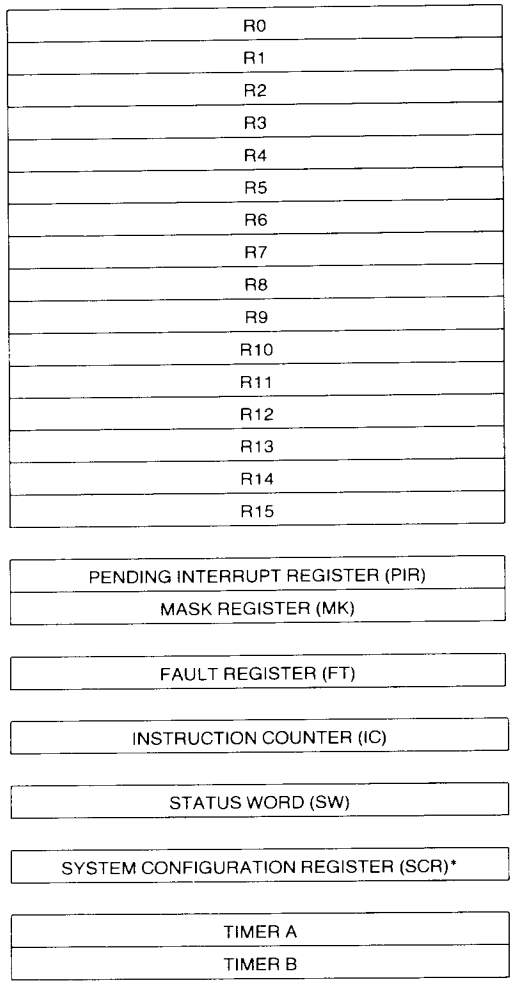
Double Precision

FIGURE 1. F9450 Floating-Point Formats

Register Set

The F9450 contains 24 user-accessible registers. A model of these registers is shown in *Figure 2*. There are 16 program-accessible general-purpose registers (R0 to R15), a Pending Interrupt Register (PIR), Mask Register (MK), Fault Register (FT), Instruction Counter (IC), Status Word Register (SW), System Configuration Register (SCR), and two Timers (A and B). The PIR, MK and FT are described in the "Interrupts" section. The 16-bit IC contains the address of the instruction currently being executed.

The F9450 register set also includes six temporary registers, A1, A2, DO1, DO2, Q1, and Q2, that are internal to the operation of the F9450 and accessible only from the console. These, therefore, are not included in the programmer's model.



*The SCR is 5 bits only, and is not available to the programmer.

FIGURE 2. F9450 Programmer's Register Model

Status Word Register (SW)

The Status Word Register is 16 bits wide, defined as:

0			3	4	7	8	11	12	15
C	P	Z	N	RESERVED		AK (PS)		AS	

C Carry
P Positive
Z Zero
N Negative

Results of the most recent arithmetic operation.

Reserved These bits will be 0

AK(PS) Access Key/Processor State bits serve two functions:

1. Determine the legal/illegal criteria for privileged instructions. A priviledged instruction is executed with PS = 0 only. An attempt to execute a privileged instruction with PS ≠ 0 causes a Major Error, sets bit 10 in the Fault Register, and causes an instruction abort.
2. Define the Access Key that is used in systems with an MMU to match an Access Lock.

AS Address State defines a page register group in the MMU. For configurations without an MMU, an Address State fault is generated (bit 11 in the Fault Register is set) for any operations attempting to modify the AS field to a nonzero value. Note that this condition is also tested during interrupt processing (i.e., an interrupt service status word with AS ≠ 0 will be aborted).

All usable bits of the status word can be modified under program control or from the console (for details, refer to the F9451 MMU datasheet).

System Configuration Register (SCR)

The SCR defines to the F9450 control circuitry the configuration of the external system connected to the CPU.

The 5-bit wide SCR is defined as:

0	1	2	3	4	5	15
M	B	C	P	I	Not Use	

M MMU Present = 1 if an MMU is connected in the system. This must be set if the application ever requires AS ≠ 0.

B BPU Present = 1 if a BPU is connected in the system.

C Console Present = 1 if a console is connected in the system.

P Coprocessor = 1 if a coprocessor is connected in the system. If this bit is not set, the BIF instruction (see the "Built-In Function Implementation" section) will be considered an illegal instruction.

I Interrupt Mode = Selects the interrupt mode for the PWRDN INT and USR_0 INT-USR_5 INT signals: 1 is level-sensitive, 0 is edge-sensitive (low to high).

To load the SCR, external hardware is required to respond to an I/O Read request at I/O address 8410 (Hex). The internal SCR is not program-accessible, but is automatically loaded from the external hardware via the I/O Read from 8410, which is initiated by the F9450 during either the Reset initialization or the execution of the breakpoint instruction (BPT).

Timer A and Timer B

The two 16-bit-wide timers are started, halted, loaded, and read under software control. Timer A is controlled by the timer clock (100 kHz) and Timer B is controlled by the timer clock divided by 10.

When Timer A and Timer B reach their terminal counts, they set the corresponding bits in the PIR. Both are halted when the CPU is in the console mode and continue on the resumption of program execution.

Instruction Set

The instruction set of the F9450 is optimized for real-time applications in accordance with the MIL-STD-1750A ISA. Table I shows addressing modes and related instruction word formats, Derived Address (DA), and Derived Operand (DO). Not all instructions use all the addressing modes; therefore, acceptable addressing modes should be confirmed for each instruction. Table II provides the instruction set with applicable addressing modes and Table III gives the dedicated I/O addresses.

MIL-STD-1750A Description

For a complete description of the instruction set, refer to MIL-STD-1750A ISA. The military standard is available from the Department of the Navy, Naval Publications and Forms Center, 5801 Tabor Ave., Philadelphia, PA 19120, telephone (603) 121-3202.

Addressing Modes

There are ten addressing modes. The smallest addressable memory word is 16 bits. Therefore, the 16-bit address field allows direct addressing of 64k words. There is no restriction on the location of double-word operands in memory.

1. **Register Direct (R):** The instruction-specified register contains the required operand. With the exception of this mode, the Derived Address (DA) denotes a memory address.
2. **Memory Direct (D):** In this mode, the instruction contains the memory address of the operand.
3. **Memory Direct—Indexed (DX):** The memory address of the required operand is specified by the sum of the contents of an index register and the instruction address field. Registers R1 through R15 may be specified for indexing.
4. **Memory Indirect (I):** The instruction-specified memory address contains the address of the required operand.

Addressing Modes (Continued)

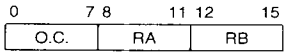
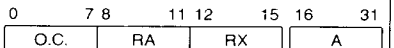
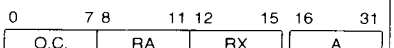
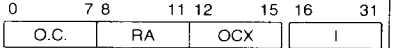
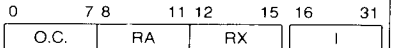
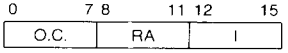
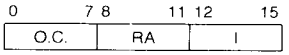
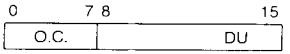
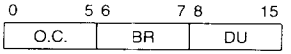
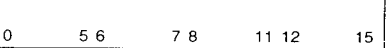
5. **Memory Indirect with Pre-Indexing (IX):** The sum of the contents of a specified index register and the instruction address field specify the address of a memory location containing the address of the required operand. Registers R1 through R15 may be specified for pre-indexing.
6. **Immediate Long (IM):** One method of Immediate Long addressing allows indexing and one does not. The indexable form of immediate addressing is shown in Table III. If the specified index register, RX, is $\neq 0$, the contents of RX is added to the immediate field to form the required operand; otherwise, the immediate field contains the required operand.
7. **Immediate Short(IS):** The required 4-bit operand is contained within the 16-bit instruction. One method of Immediate Short addressing interprets the contents of the immediate field as positive data and another method interprets the contents of the immediate field as negative data.
   a. **Immediate Short Positive (ISP):** The immediate operand is treated as a positive integer between 1 and 16.
   b. **Immediate Short Negative (ISN):** The immediate operand is treated as a negative integer between 1 and 16. Its internal form is a twos-complement, sign-extended 16-bit number.
8. **Instruction Counter Relative (ICR):** This mode is used for 16-bit branch instructions. The contents of the instruction counter minus one (i.e., the address of the current instruction) are added to the sign-extended 8-bit displacement field of the instruction. The sum points to the memory address to which control may be transferred if a branch is executed. This mode allows addressing within a memory region of -128 to $+127$ words, relative to the address of the current instruction.
9. **Base Relative (B):** The contents of an instruction-specified base register are added to the 8-bit displacement field of the 16-bit instruction. The displacement field is taken to be a positive number between 0 and 255. The sum points to the memory address of the required operand. This mode allows addressing within a memory region of 256 words, beginning at the address pointed to by the base register.
10. **Base Relative-Indexed (BX):** The sum of the contents of a specified index register and a specified base register is the address of the required operand. Registers R1 through R15 may be specified for indexing.

Table II shows execution time as a function of clock cycles for the instruction set of the F9450. This information is based on the microprogram of the F9450 and is subject to change for future design iterations.

Note that many instructions, including all floating-point operations, are data-dependent. This information is given as a guide to the user and includes a great number of these data dependencies. Such error conditions as overflows or underflows are not included in this table. Care should be taken to verify these times on a device with actual data for time-critical applications.

Addressing Modes (Continued)

TABLE I. F9450 Addressing Modes and Instruction Formats

Mode	Format	Derived Operand (DO)		Derived Address (DA)	
		Single-Precision	Floating-Point and Double Precision	Single-Precision	Floating-Point and Double Precision
1. Register Direct					
"R"		(RB)	(RB, RB + 1)	RB	RB, RB + 1
2. Memory Direct					
"D"	RX = 0 (Non-Indexed)	[A]	[A, A + 1]	A	A, A + 1
"DX"	RX ≠ 0 (Indexed)	[A + (RX)]	[A + (RX), A + 1 + (RX)]	A + (RX)	A + (RX), A + 1 + (RX)
3. Memory Indirect					
"I"	RX = 0 (Non-Indexed)	[|A|]	[|A|, |A| + 1]	[A]	[A], [A] + 1
"IX"	RX ≠ 0 (Indexed)	[|A + (RX)|]	[|A + (RX)|, |A + (RX)| + 1]	[A + (RX)]	[A + (RX)], [A + (RX)] + 1
4. Immediate Long					
a. Not Indexable					
"IM"		I			
b. Indexable					
"IM"	RX = 0 (Non-Indexed)	I			
"IMX"	RX = 0 (Indexed)	I + (RX)			
5. Immediate Short					
a. Positive					
"ISP"		+ (I + 1)			
b. Negative					
"ISN"		− (I + 1)			
6. IC Relative (Note 1)					
"ICR"				DU + (IC − 1)	
7. Base Relative (Note 2)					
a. Not Indexable (Note 3)					
"B"	BR = BR + 12	[DU + (BR)]	[DU + (BR), DU + 1 + (BR)]	DU + (BR)	DU + (BR), DU + 1 + (BR)
b. Indexable					
"B"	RX = 0 (Non-Indexed)	[(BR)]	[(BR), (RR) + 1]	(BR)	(BR), (BR) + 1
"BX"	RX ≠ 0 (Indexed)	[(BR) + (RX)]	[(BR) + (RX), (BR) + 1 + (RX)]	(BR) + (RX)	(BR) + (RX), (BR) + 1 + (RX)

Note 1: $-128 \leq DU \leq 127$.

Note 2: Base registers: BR = R12, R13, R14 and R15.

Note 3: $0 \leq DU \leq 255$.

Note 4: Extended-precision floating-point instructions require addressing of three operands located at DA, DA + 1 and DA + 2.

Instruction Execution Times

TABLE II. F9450 Instruction Execution Times

Group	Instruction	Mode	Nf	No	Nc	Notes
INTEGER ARITHMETIC/LOGIC						
Single-Precision Add	A	R	1	0	5	Nf/N6
	A	B	1	1	12	Nf/N6
	A	BX	1	1	12	Nf/N6
	A	ISP	1	0	8	Nf/N6
	A	D	2	1	13	Nf/N6
	A	DX	2	1	13	Nf/N6
	A	IM	2	0	12	Nf/N6
Double-Precision Add	DA	R	1	0	18	
	DA	D	2	2	24	
	DA	DX	2	2	24	
Increment Memory by	INCM	D	2	2	17	Nf/N6 Bus Lock
Positive Integer	INCM	DX	2	2	17	Nf/N6 Bus Lock
Single-Precision	ABS	R	1	0	5	Nf/N6, Pos. #
Absolute Value	ABS	R	1	0	10	Nf/N6, Neg. #
Double-Precision	DABS	R	1	0	13	Pos. #
Absolute Value	DABS	R	1	0	21	Neg. #
Single-Precision Subtract	S	R	1	0	5	Nf/N6
	S	B	1	1	12	Nf/N6
	S	BX	1	1	12	Nf/N6
	S	ISP	1	0	8	Nf/N6
	S	D	2	1	13	Nf/N6
	S	DX	2	1	13	Nf/N6
	S	IM	2	0	12	Nf/N6
Double-Precision Subtract	DS	R	1	0	18	
	DS	D	2	2	24	
	DS	DX	2	2	24	
Decrement Memory by	DECM	D	2	2	17	Nf/N6 Bus Lock
Positive Integer	DECM	DX	2	2	17	Nf/N6 Bus Lock
Single-Precision Negate	NEG	R	1	0	5	Nf/N6
Double-Precision Negate	DNEG	R	1	0	18	
Single-Precision Multiply	MS	R	1	0	44	
16-Bit Product	MS	ISP	1	0	47	
	MS	ISN	1	0	47	
	MS	D	2	1	52	
	MS	DX	2	1	52	
	MS	IM	2	0	51	
			0	0	(30)	+ Zero Multiplicand
Single-Precision Multiply	M	R	1	0	42	
32-Bit Product	M	B	1	1	49	
	M	BX	1	1	49	
	M	D	2	1	50	
	M	DX	2	1	50	
	M	IM	2	0	49	
			0	0	5	+ Zero MSW of Multiplicand
			0	0	(25)	+ Zero Multiplicand
Double-Precision Multiply	DM	R	1	0	130	
	DM	D	2	2	136	
	DM	DX	2	2	136	
Single-Precision Divide	DV	R	1	0	100	Nf/N6
16-Bit Dividend	DV	ISP	1	0	100	Nf/N6
	DV	ISN	1	0	100	Nf/N6

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
INTEGER ARITHMETIC/LOGIC (Continued)						
	DV	D	2	1	105	Nf/N6
	DV	DX	2	1	105	Nf/N6
	DV	IM	2	0	104	Nf/N6
			0	0	5	Add for Dividend = 8000(H)
			0	0	6	Add for Negative Dividend
			0	0	3	Add for Negative Divisor
			0	0	3	Add for Remainder Correction
Single-Precision Divide	D	R	1	0	101	Nf/N6
32-Bit Dividend	D	B	1	1	105	Nf/N6
	D	BX	1	1	105	Nf/N6
	D	D	2	1	106	Nf/N6
	D	DX	2	1	106	Nf/N6
	D	IM	2	0	105	Nf/N6
			0	0	6	Add for RA ≥ Divisor
			0	0	9	Add for Negative Dividend
			0	0	5	Add for Negative Divisor
			0	0	3	Add for Remainder Correction
Double-Precision Divide	DD	R	1	0	241	
	DD	D	2	2	247	
	DD	DX	2	2	247	
			0	0	6	Add for Negative Dividend
			0	0	6	Add for Negative Divisor
			0	0	7	Add for Negative Result
			0	0	5	Add for MSW of Dividend = 8000(H)
			0	0	5	Add for Dividend = 8000 0000(H)
			0	0	5	Add Above + LSW of Dividend = −1
Single-Precision Compare	C	R	1	0	8	Nf/N6
	C	B	1	1	15	Nf/N6
	C	BX	1	1	15	Nf/N6
	C	ISP	1	0	11	Nf/N6
	C	ISN	1	0	11	Nf/N6
	C	D	2	1	16	Nf/N6
	C	DX	2	1	16	Nf/N6
	C	IM	2	0	15	Nf/N6
Compare Between Limits	CBL	D	2	2	30	Nf/N6 (RA < DO1)
			2	2	43	Nf/N6 (DO1 ≤ RA ≤ DO2)
			2	2	40	Nf/N6 (RA > DO2)
	CBL	DX	2	2	30	Nf/N6 (RA < DO1)
			2	2	43	Nf/N6 (DO1 ≤ RA ≤ DO2)
			2	2	40	Nf/N6 (RA > DO2)
Double-Precision Compare	DC	R	1	0	21	
	DC	D	2	2	27	
	DC	DX	2	2	27	
Inclusive-OR	OR	R	1	0	4	
	OR	B	1	1	11	
	OR	BX	1	1	11	
	OR	D	2	1	12	
	OR	DX	2	1	12	
	OR	IM	2	0	11	
AND	AND	R	1	0	4	
	AND	B	1	1	11	
	AND	BX	1	1	11	

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
INTEGER ARITHMETIC/LOGIC (Continued)						
	AND	D	2	1	12	
	AND	DX	2	1	12	
	AND	IM	2	0	11	
Exclusive-OR	XOR	R	1	0	4	
	XOR	D	2	1	12	
	XOR	DX	2	1	12	
	XOR	IM	2	0	11	
NAND	NAND	R	1	0	9	
	NAND	D	2	1	17	
	NAND	DX	2	1	17	
	NAND	IM	2	0	16	
FLOATING POINT						
Floating-Point Add	FA	R	1	0	91	(Note 3) No Shifts in
			1	0	70	(Note 2) Exponent Adjust
	FA	B	1	2	96	(Note 3) And in
			1	2	75	(Note 2) Normalization
	FA	BX	1	2	96	(Note 3)
			1	2	75	(Note 2)
	FA	D	2	2	97	(Note 3)
			2	2	76	(Note 2)
	FA	DX	2	2	97	(Note 3)
			2	2	76	(Note 2)
	FA	ALL	0	0	(15)	+ RA = 0
			0	0	(67)	(Note 3) + D0 = 0
			0	0	(46)	(Note 2)
			0	0	14	+ Addition Overflow
			0	0	8	+ Scale RA
			0	0	6	Incremental
			0	0	6	+ Scale D0
			0	0	6	Incremental
			0	0	5	+ Normalize
			0	0	13	Incremental
			0	0	5	Unnormalized Mantissa = 0
			0	0	10	Result = 0
Extended-Precision Floating-Point Add	EFA	R	1	0	106	(Note 3)
			1	0	85	(Note 2)
	EFA	D	2	3	113	(Note 3)
			2	3	92	(Note 2)
	EFA	DX	2	3	113	(Note 3)
			2	3	92	(Note 2)
	EFA	ALL	0	0	(15)	+ RA = 0
			0	0	(76)	(Note 3) + D0 = 0
			0	0	(55)	(Note 2)
			0	0	17	+ Addition Overflow
			0	0	8	+ Scale RA
			0	0	9	Incremental
			0	0	6	+ Scale D0
			0	0	9	Incremental
			0	0	8	+ Normalize
			0	0	16	Incremental
			0	0	2	MSH of Mantissa = 0

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
FLOATING POINT (Continued)						
			0	0	7	Unormalized Mantissa = 0
			0	0	20	Result = 0
Floating-Point	FABS	R	1	0	16	Pos. #
Absolute Value	FABS	R	1	0	71	Neg. #
Floating-Point Subtract	FS	R	1	0	91	(Note 3)
			1	0	70	(Note 2)
	FS	B	1	2	96	(Note 3)
			1	2	75	(Note 2)
	FS	BX	1	2	96	(Note 3)
			1	2	75	(Note 2)
	FS	D	2	2	97	(Note 3)
			2	2	76	(Note 2)
	FS	DX	2	2	97	(Note 3)
			2	2	76	(Note 2)
	FS	ALL	0	0	(15)	+ RA = 0
			0	0	(67)	+ D0 = 0 (Note 3)
			0	0	(46)	(Note 2)
			0	0	14	+ Addition Overflow (Note 3)
			0	0	17	(Note 2)
			0	0	8	+ Scale RA
			0	0	6	Incremental
			0	0	6	+ Scale D0
			0	0	6	Incremental
			0	0	5	+ Normalize
			0	0	13	Incremental
			0	0	5	Unnormalized Mantissa = 0
			0	0	10	Result = 0
Extended-Precision	EFS	R	1	0	106	(Note 3)
Floating-Point Subtract			1	0	85	(Note 2)
	EFS	D	2	3	113	(Note 3)
			2	3	92	(Note 2)
	EFS	DX	2	3	113	(Note 3)
			2	3	92	(Note 2)
	EFS	ALL	0	0	(15)	+RA = 0
			0	0	(76)	+ D0 = 0 (Note 3)
			0	0	5	(Note 2)
			0	0	17	+ Addition Overflow
			0	0	8	+ Scale RA
			0	0	9	Incremental
			0	0	6	+ Scale D0
			0	0	9	Incremental
			0	0	8	+ Normalize
			0	0	16	Incremental
			0	0	2	MSH of Mantissa = 0
			0	0	7	Unnormalized Mantissa = 0
			0	0	20	Result = 0
Floating-Point Negate	FNEG	R	1	0	61	POS #
			1	0	65	NEG #
Floating-Point Multiply	FM	R	1	0	120	
	FM	B	1	2	125	
	FM	BX	1	2	125	
	FM	D	2	2	126	

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
FLOATING POINT (Continued)						
	FM	DX	2	2	126	
			0	0	18	+ Normalize
			0	0	6	+ 8000 00XX * 8000 00XX
Extended-Precision	EFM	R	1	0	243	
Floating-Point Multiply	EFM	D	2	3	250	
	EFM	DX	2	3	250	
			0	0	24	+ Normalize
			0	0	6	+ 8000 00XX 0000 * 8000 00XX 0000
Floating-Point Divide	FD	R	1	0	222	
	FD	B	1	2	227	
	FD	BX	1	2	227	
	FD	D	2	2	228	
	FD	DX	2	2	228	
	FD	ALL	0	0	18	+ Normalize
			0	0	14	+ MAN(RA) > MAN(DO)
			0	0	9	+ MAN(RA) = MAN(DO)
			0	0	(181)	+ Divisor = 0
			0	0	(195)	+ Dividend = 0
			0	0	6	+ Correction Required
Extended-Precision	EFD	R	1	0	462	
Floating-Point Divide	EFD	D	2	3	469	
	EFD	DX	2	3	469	
			0	0	24	+ Normalize
			0	0	17	+ MAN(RA) > MAN(DO)
			0	0	12	+ MAN(RA) = MAN(DO)
			0	0	(412)	+ Divisor = 0
			0	0	(435)	+ Dividend = 0
			0	0	3	+ Correction Required
Floating-Point Compare	FC	R	1	0	52	Nf/N6; RA < DO; RA > DO, A1 < >0
	FC	B	1	2	57	Nf/N6; RA < DO; RA > DO, A1 < >0
	FC	BX	1	2	57	Nf/N6; RA < DO; RA > DO, A1 < >0
	FC	D	2	2	58	Nf/N6; RA < DO; RA > DO, A1 < >0
	FC	DX	2	2	58	Nf/N6; RA < DO; RA > DO, A1 < >0
			0	0	(15)	+ RA = 0
			0	0	(28)	+ DO = 0
			0	0	14	+ Addition Overflow
			0	0	8	+ Scale RA
			0	0	6	Incremental
			0	0	3	+ Scale DO
			0	0	6	Incremental
			0	0	10	+ RA = DO; RA > DO, A1 = 0, A2 > 0
			0	0	13	+ RA > DO, A1 = 0, A2 < 0
Extended-Precision	EFC	R	1	0	55	Nf/N6; RA < DO; RA > DO, A1 < > 0
Floating-Point Compare	EFC	D	2	3	68	Nf/N6; RA < DO; RA > DO, A1 < > 0
	EFC	DX	2	3	68	Nf/N6; RA < DO; RA > DO, A1 < > 0
	EFC	ALL	0	0	(15)	+ RA = 0
			0	0	(31)	+ DO = 0
			0	0	9	+ Addition Overflow
			0	0	8	+ Scale RA
			0	0	9	Incremental
			0	0	3	+ Scale DO
			0	0	9	Incremental

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
FLOATING POINT (Continued)						
			0	0	15	+ RA = DO
			0	0	8	+ RA > DO, A1 = 0, A2 > 0
			0	0	13	+ RA > DO, A1 = 0, A2 < 0
			0	0	15	+ RA > DO, A1 = 0, A2 = 0, Q1 > 0
			0	0	18	+ RA > DO, A1 = 0, A2 = 0, Q1 < 0
Convert Floating-Point to 16-Bit Integer	FIX	R	1	0	28	Nf/N6, 0 < EXP(RB) < 15
			0	0	3	Incremental (14-EXP(RB) Times)
			1	0	10	Nf/N6, RB = 0
			1	0	25	Nf/N6, EXP(RB) = 15
			0	0	8	+ RB < 0, RB + 1 = 0
			0	0	10	+ RB < 0, RB + 1 < > 0
			1	0	13	Nf/N6, EXP(RB) < 0
			1	0	26	Nf/N6, EXP(RB) > 15
Convert 16-Bit Integer to Floating-Point	FLT	R	1	0	16	Nf/N6
			1	0	8	Nf/N6, DO = 0
			0	0	5	+ Normalization
			0	0	13	Incremental
Convert Extended-Precision Floating-Point to 32-Bit Integer	EFIX	R	1	0	44	0 < EXP (DO) < 31
			0	0	6	Incremental (30-EXP(DO) Times)
			1	0	21	RB = 0
			1	0	36	EXP(DO) = 31
			0	0	8	+ RB < 0, RB + 2 = 0
			0	0	15	+ RB < 0, RB + 2 < > 0
			1	0	24	EXP (DO) < 0
			1	0	39	EXP (DO) > 31
Convert 32-Bit Integer to Extended-Precision Floating-Point	EFLT	R	1	0	31	Nf/N6, RA < >0
			0	0	8	+ Normalization
			0	0	16	+ Normalization, Incremental
			0	0	2	+ RA = 0, RA < > 0
			1	0	22	Nf/N6, RA = 0, RA + 1 = 0
BIT OPERATIONS						
Set Bit	SB	R	1	0	7	
	SB	D	2	2	16	Bus Lock
	SB	DX	2	2	16	Bus Lock
	SB	I	2	3	20	Bus Lock
	SB	IX	2	3	20	Bus Lock
Reset Bit	RB	R	2	0	7	
	RB	D	2	2	16	Bus Lock
	RB	DX	2	2	16	Bus Lock
	RB	I	2	3	20	Bus Lock
	RB	IX	2	3	20	Bus Lock
Test Bit	TB	R	2	0	7	
	TB	D	2	1	15	
	TB	DX	2	1	15	
	TB	I	2	2	19	
	TB	IX	2	2	19	
Test and Set Bit	TSB	D	2	3	23	Bus Lock (2)
	TSB	DX	2	3	23	Bus Lock (2)
Set Variable Bit in Register	SVBR	R	1	0	7	
Reset Variable Bit in Register	RVBR	R	1	0	7	
Test Variable Bit in Register	TVBR	R	1	0	7	

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
SHIFT						
Shift Left Logical	SLL	R	1	0	7	One Shift
			0	0	3	Incremental
Shift Right Logical	SRL	R	1	0	7	One Shift
			0	0	3	Incremental
Shift Right Arithmetic	SRA	R	1	0	7	One Shift
			0	0	3	Incremental
Shift Left Cyclic	SLC	R	1	0	7	One Shift
			0	0	3	Incremental
Double Shift Left Logical	DSLL	R	1	0	16	One Shift
			0	0	6	Incremental
Double Shift Right Logical	DSRL	R	1	0	16	One Shift
			0	0	6	Incremental
Double Shift Right Arithmetic	DSRA	R	1	0	16	One Shift
			0	0	6	Incremental
Double Shift Left Cyclic	DSLC	R	1	0	19	One Shift
			0	0	9	Incremental
Shift Logical, Count in Register	SLR	R	1	0	8	Nf/N6, No Shift
			1	0	21	Nf/N6, Right
			0	0	3	Incremental
	SLR	R	1	0	38	Nf/N6, Left
			0	0	5	Incremental
Shift Arithmetic Count in Register	SAR	R	1	0	8	Nf/N6, No Shift
			1	0	21	Nf/N6, Right
			0	0	3	Incremental
	SAR	R	1	0	29	Nf/N6, Left
			0	0	5	Incremental
Shift Cyclic, Count in Register	SCR	R	1	0	8	Nf/N6, No Shift
			1	0	21	Nf/N6, Right
			0	0	3	Incremental
	SCR	R	1	0	24	Nf/N6, Left
			0	0	3	Incremental
Double Shift Logical, Count in Register	DSLR	R	1	0	11	Nf/N6, No Shift
			1	0	30	Nf/N6, Right
			0	0	6	Incremental
	DSLR	R	1	0	44	Nf/N6, Left
			0	0	8	Incremental
Double Shift Arithmetic, Count in Register	DSAR	R	1	0	11	Nf/N6, No Shift
			1	0	30	Nf/N6, Right
			0	0	6	Incremental
	DSAR	R	1	0	35	Nf/N6, Left
			0	0	8	Incremental
Double Shift Cyclic, Count in Register	DSCR	R	1	0	11	Nf/N6, No Shift
			1	0	33	Nf/N6, Right
			0	0	9	Incremental
	DSCR	R	1	0	33	Nf/N6, Left
			0	0	9	Incremental

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
LOAD/STORE/EXCHANGE						
Single-Precision Load	L	R	1	0	4	
	L	B	1	1	11	
	L	BX	1	1	11	
	L	ISP	1	0	7	
	L	ISN	1	0	7	
	L	D	2	1	12	
	L	DX	2	1	12	
	L	IM	2	0	11	
	L	IMX	2	0	14	
	L	I	2	2	16	
	L	IX	2	2	16	
Double-Precision Load	DL	R	1	0	16	
	DL	B	1	2	21	
	DL	BX	1	2	21	
	DL	D	2	2	22	
	DL	DX	2	2	22	
	DL	I	2	3	26	
	DL	IX	2	3	26	
Extended-Precision	EFL	D	2	3	26	
Floating-Point Load	EFL	DX	2	3	26	
Load from Upper Byte	LUB	D	2	1	15	
	LUB	DX	2	1	15	
	LUB	I	2	2	19	
	LUB	IX	2	2	19	
Load from Lower Byte	LLB	D	2	1	12	
	LLB	DX	2	1	12	
	LLB	I	2	2	16	
	LLB	IX	2	2	16	
Single-Precision Store	ST	B	1	1	11	
	ST	BX	1	1	11	
	ST	D	2	1	12	
	ST	DX	2	1	12	
	ST	I	2	2	16	
	ST	IX	2	2	16	
Store a Non-Negative Constant	STC	D	2	1	12	
	STC	DX	2	1	12	
	STC	I	2	2	16	
	STC	IX	2	2	16	
Double-Precision Store	DST	B	1	2	15	
	DST	BX	1	2	15	
	DST	D	2	2	16	
	DST	DX	2	2	16	
	DST	I	2	3	20	
	DST	IX	2	3	20	
Store Register through Mask	SRM	D	2	2	25	Bus Lock (1)
	SRM	DX	2	2	25	Bus Lock (1)
Extended-Precision	EFST	D	2	3	20	
Floating-Point Store	EFST	DX	2	3	20	
Store into Upper Byte	STUB	D	2	2	16	Bus Lock
	STUB	DX	2	2	16	Bus Lock
	STUB	I	2	3	20	Bus Lock
	STUB	IX	2	3	20	Bus Lock
Store into Lower Byte	STLB	D	2	2	16	Bus Lock
	STLB	DX	2	2	16	Bus Lock
	STLB	I	2	3	20	Bus Lock
	STLB	IX	2	3	20	Bus Lock
Exchange Bytes in Register	XBR	S	1	0	7	
Exchange Words in Registers	XWR	R	1	0	10	

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
MULTIPLE LOAD/STORE						
Push Multiple Registers onto the Stack	PSHM	S	1	1	16	One operation
			0	1	12	Incremental
Pop Multiple Registers off the Stack	POPM	S	1	1	20	Nf/N6
			0	1	16	Incremental
Load Multiple Registers	LM	D	2	1	16	
			0	1	8	Incremental
	LM	DX	2	1	16	
			0	1	8	Incremental
Store Multiple Registers	STM	D	2	1	17	
			0	1	9	Incremental
	STM	DX	2	1	17	
			0	1	9	Incremental
Move Multiple Words, Memory-to-Memory	MOV	S	1	0	9	No Move
			1	2	37	One Move
			0	2	13	Incremental
PROGRAM CONTROL						
Jump on Condition	JC	D	2	0	9	Nf/N6, No Jump
	JC	D	3	0	17	Nf/N6, Jump
	JC	DX	2	0	9	Nf/N6, No Jump
	JC	DX	3	0	17	Nf/N6, Jump
	JC	I	2	1	13	Nf/N6, No Jump
	JC	I	3	1	21	Nf/N6, Jump
	JC	IX	2	1	13	Nf/N6, No Jump
	JC	IX	3	1	21	Nf/N6, Jump
Jump to Subroutine	JS	D	3	0	12	
	JS	DX	3	0	12	
Subtract One and Jump	SOJ	D	2	0	13	No Jump
	SOJ	D	3	0	17	Jump
	SOJ	DX	2	0	13	No Jump
	SOJ	DX	3	0	17	Jump
Branch Unconditionally	BR	ICR	2	0	14	
Branch if Equal to (Zero)	BEZ	ICR	1	0	4	No Branch
	BEZ	ICR	3	0	15	Branch
Branch if Less than (Zero)	BLT	ICR	1	0	4	No Branch
	BLT	ICR	3	0	15	Branch
Branch if Less than or Equal to (Zero)	BLE	ICR	1	0	4	No Branch
	BLE	ICR	3	0	15	Branch
Branch if Greater than (Zero)	BGT	ICR	1	0	4	No Branch
	BGT	ICR	3	0	15	Branch
Branch if Not Equal to (Zero)	BNZ	ICR	1	0	4	No Branch
	BNZ	ICR	3	0	15	Branch
Branch if Greater than or Equal to (Zero)	BGE	ICR	1	0	4	No Branch
	BGE	ICR	3	0	15	Branch
Branch to Executive	BEX	S	2	8	92	No MMU
			2	8	87	MMU
Load Status (Note 1)	LST	D	3	3	42	MMU Attached
			3	3	47	No MMU Attached
	LST	DX	3	3	42	MMU Attached
			3	3	47	No MMU Attached
	LST	I	3	4	46	MMU Attached
			3	4	51	No MMU Attached
	LST	IX	3	4	46	MMU Attached
			3	4	51	No MMU Attached
Stack IC and Jump to Subroutine	SJS	D	3	1	22	
	SJS	DX	3	1	22	
Unstack IC and Return from Subroutine	URS	S	3	1	15	
No-Operation	NOP	S	1	0	9	
Breakpoint	BPT	S	1	1	23	No Console (I/O)
Built-In-Function (to Utilize External Co-Processors)	BIF	D	3	2	34	(I/O)
	BIF	DX	3	2	34	(I/O)
	BIF	I	3	3	38	(2 I/O)
	BIF	IX	3	3	38	(2 I/O)

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
PROGRAMMED INPUT/OUTPUT						
Execute Input/Output (Note 1)	XIO	IM	2	0	27	Overhead—PI
	XIO	IMX	2	0	30	Overhead—PI
	XIO	IM	2	0	21	Overhead—PO
	XIO	IMX	2	0	24	Overhead—PO
Vectored Input/Output (Note 1)	VIO	D	2	2	35	Overhead
	VIO	DX	2	2	38	Overhead
	VIO		0	1	33	PI Case—Incremental
	VIO		0	1	30	PO Case—Incremental
	VIO		0	0	18	Incremental—Unused Bits
Programmed Input	PI		0	1	4	(I/O In)
Programmed Output	PO		0	1	5	(I/O Out)
TIMER CONTROL						
Timer A Start	TAS		0	1	5	(I/O Out)
Timer A Halt	TAH		0	1	5	(I/O Out)
Output Timer A	OTA		0	1	7	(I/O Out)
Input Timer A	ITA		0	1	7	(I/O In)
Timer B Start	TBS		0	1	5	(I/O Out)
Timer B Halt	TBH		0	1	5	(I/O Out)
Output Timer B	OTB		0	1	7	(I/O Out)
Input Timer B	ITB		0	1	7	(I/O In)
INTERRUPT/DMA/FAULT CONTROL						
Set Interrupt Mask	SMK		0	1	4	(I/O Out)
Clear Interrupt Request	CLIR		0	1	7	(I/O Out)
Enable Interrupts	ENBL		0	1	5	(I/O Out)
Disable Interrupts	DSBL		0	1	5	(I/O Out)
Reset Pending Interrupt	RPI		0	1	18	(I/O Out)
Set Pending Interrupt	SPI		0	1	4	(I/O Out)
Read Interrupt Mask	RMK		0	1	4	(I/O In)
Read Pending Interrupt Register	RPIR		0	1	3	(I/O In)
Read and Clear Fault Register	RCFR		0	1	7	(I/O In)
Enable DMA	DMAE		0	1	5	(I/O Out)
Disable DMA	DMAD		0	1	5	(I/O Out)
MMU CONTROL						
Write Instruction Page Register	WIPR		0	1	5	(I/O Out)
Write Operand Page Register	WOPR		0	1	5	(I/O Out)
Read Instruction Page Register	RIPR		0	1	4	(I/O In)
Read Operand Page Register	ROPR		0	1	4	(I/O In)
BPU CONTROL						
Load Memory Protect RAM	LMP		0	1	5	(I/O Out)
Read Memory Protect RAM	RMP		0	1	4	(I/O In)
Memory Protect Enable	MPEN		0	1	5	(I/O Out)
MISC						
Write Status Word	WSW		0	1	12	(I/O Out) MMU
	WSW		0	1	17	(I/O Out) No MMU
Read Status Word	RSW		0	1	4	(I/O In)
Reset NML PWRUP Discrete	RNS		0	1	5	(I/O Out)
Pulse the TRIGO RST Signal	GO		1	1	5	(I/O Out)

Instruction Execution Times (Continued)

TABLE II. F9450 Instruction Execution Times (Continued)

Group	Instruction	Mode	Nf	No	Nc	Notes
CONSOLE OPERATIONS						
Disable	74		0	0	19	Repeat Till Interrupt or CONREQ
Examine Register	60		0	2	20	
Deposit Register	61		0	2	20	
Examine and Clear Fault Register	62		0	2	20	
Deposit Status Word	63		0	2	22	
Examine Memory	66		0	4	28	
Deposit Memory	67		0	3	21	
Examine Next Memory	6A		0	3	27	
Deposit Next Memory	6B		0	3	24	
Continue	75		2	1	24	
Examine XIO	6C		0	4	31	
Deposit XIO	6D		0	3	24	
Examine Next XIO	6E		0	3	27	
Deposit Next XIO	6F		0	3	27	
INTERRUPT RESPONSE						
Interrupt Acknowledge			2	9	96	No MMU
			2	9	91	MMU

Note 1: Privileged Instruction

Note 2: F9450-F15, F18, F20 Only

Note 3: F9450-15 Only

Nf: Number of Instruction Fetch cycles.

No: Number of Operand bus cycles (either Memory or I/O). I/O cycles are indicated with a note in the comments column. VIO instructions include only the execution of one operation.

Nc: Total number of clocks needed to perform the operation. Variable length instructions require the addition of the base time plus the proper number of increments.

Nf/N6: An Instruction Fetch occurs during a 5-clock-machine cycle, thus hiding 1 wait state in the data phase of the operation.

Bus Lock: Bus Lock is used during the execution of the instruction to retain control of the bus for 2 consecutive machine cycles.

Bus Lock (1): This instruction activates Bus Lock and keeps it active for 2 bus cycles with 1 ALU cycle in between.

Bus Lock (2): This instruction activates Bus Lock and keeps it active for a total of 4 machine cycles, including:

1 Memory Read Bus Cycle	1 Memory Read Bus Cycle
1 ALU Cycle	1 Memory Write Bus Cycle

Calculation of some instruction execution times requires the addition of more than one number, e.g., the time for an RPI I/O command in a VIO chain requires the addition of the base time for the VIO instruction, plus the incremental time for each VIO operation, plus the time for any unused bits preceding the RPI in the VIO Vector Select, plus the time for the RPI command.

All floating-point operations assume normalized operands and yield normalized results per requirements of MIL-STD-1750A.

Floating-point compares are implemented through the use of the floating-point subtract. Results are held and tested in the temporary registers A1, A2, and Q1. The execution time for a floating-point compare may depend on the values in these registers.

Instruction Execution Times (Continued)

TABLE IIa. MIL-STD-1750A Defined I/O Commands

Mnemonic	Function	I/O Command Field (Hex)	
TIMER CONTROL			
TAS	Timer A Start	4008	The F9450 implements these I/O commands on-chip.
TAH	Timer A Halt	4009	
OTA	Output Timer A	400A	
ITA	Input Timer A	C00A	
TBS	Timer B Start	400C	
TBH	Timer B Halt	400D	
OTB	Output Timer B	400E	
ITB	Input Timer B	C00E	
INTERRUPT/DMA/FAULT CONTROL			
SMK	Set Interrupt Mask	2000	The F9450 implements these I/O commands on-chip.
CLIR	Clear Interrupt Request	2001	
ENBL	Enable Interrupts	2002	
DSBL	Disable Interrupts	2003	
RPI	Reset Pending Interrupt	2004	
SPI	Set Pending Interrupt Register	2005	
RMK	Read Interrupt Mask	A000	
RPIR	Read Pending Interrupt Register	A004	
RCFR	Read and Clear Fault Register	A00F	
DMAE	DMA Enable	4006	
DMAD	DMA Disable	4007	
MISC			
WSW	Write Status Word	200E	
RSW	Read Status Word	A00E	
RNS	Reset Normal Power-Up Discrete	200A	
GO	Pulse $\overline{\text{TRIGO}}$ $\overline{\text{RST}}$ Output	400B	
MMU CONTROL			
WIPR	Write Instruction Page Register	51XY	These commands are implemented within the MMU and BPU. The F9450 performs no special operation during the execution of these I/O commands. The F9450 treats these as any external I/O.
WOPR	Write Operand Page Register	52XY	
RIPR	Read Instruction Page Register	D1XY	
ROPR	Read Operand Page Register	D2XY	
BPU CONTROL			
LMP	Load Memory Protect RAM	50XX	
RMP	Read Memory Protect RAM	D0XX	
MPEN	Memory Protect Enable	4003	
MISCELLANEOUS			
PO	Programmed Output	0YXX	The F9450 is totally transparent to these codes. No special operation results in the F9450 from the execution of these I/O commands. The F9450 treats these operations as any external I/O. Please refer to XIO and VIO instructions for execution times.
PI	Programmed Input	8YXX	
OD	Output Discretes	2008	
CO	Console Output	4000	
CLC	Clear Console	4001	
ESUR	Enable Start Up ROM	4004	
DSUR	Disable Start Up ROM	4005	
RIC1	Read I/O Interrupt Code, Level 1	A001	
RIC2	Read I/O Interrupt Code, Level 2	A002	
RDOR	Read Discrete Output Register	A008	
RDI	Read Discrete Input	A009	
TPIO	Test Programmed Output	A00B	
RMFS	Read Memory Fault Status	A00D	
CI	Console Input	C000	
RCS	Read Console Status	C001	

Instruction Execution Times (Continued)

TABLE III. F9450 Dedicated I/O Addresses

I/O Address/Command	Input/Output	Function
8400	Input	Read console command
8401	Input	Read console data
0400	Output	Write result into console
8410	Input	Read system configuration (see the "System Configuration Register (SCR)" section).
0800, 0900, 0A00, 0B00	Output	Write derived address to coprocessor no. 1, 2, 3 or 4, respectively (used to implement the Built-In Function).
0801, 0901, 0A01, 0B01	Output	Write op-code into coprocessor no. 1, 2, 3 or 4, respectively.
1000	Output	Indicate an interrupt acknowledge cycle. Used by external devices to reset their level-generated interrupts.
1F00-1F34	Output	If these I/O addresses are used within the system, they should be protected during F9450 self-test.

Note: These dedicated I/O adresses/commands are in addition to those defined by MIL-STD-1750A.

Instruction Execution Times

The execution times, in μs, for a core instruction set in the different addressing modes are given in Table IV, where all times are at 20 MHz with no wait states. The execution times degrade linearly with the clock rate if no wait states are inserted; i.e., the Add Register instruction will be 0.5 μs at 10 MHz. Table V gives the execution times in μs for a 15 MHz device under the same conditions.

Note that the times given for floating-point operations do not include any shifts for exponent adjustment or result normalization. Table II should be used to estimate execution time for floating-point operations that do require these results.

TABLE IV. F9450 Instruction Execution Times in μs, for a 20 MHz Device

Basic Instruction	Register	Direct	Direct Index	Indirect	Immediate	Immediate Short	Base Relative	Relative Index
SINGLE PRECISION								
Load/Store	0.200	0.600	0.600	0.800	0.550	0.350	0.550	0.550
Add/Sub	0.250	0.650	0.650		0.600	0.400	0.600	0.600
Multiply	2.100	2.500	2.500		2.450		2.450	2.450
Divide	5.050	5.300	5.300		5.250		5.250	5.250
Compare	0.400	0.800	0.800		0.750	0.550	0.750	0.750
Set/Reset Bit	0.350	0.800	0.800	1.000				
DOUBLE PRECISION								
Load	0.800	1.100	1.100	1.300			1.050	1.050
Store		0.800	0.800	1.000			0.750	0.750
Add/Sub	0.900	1.200	1.200					
Multiply	6.500	6.800	6.800					
Divide	12.050	12.350	12.350					
Compare	1.050	1.350	1.350					
FLOATING-POINT								
Add/Sub*	3.500	3.800	3.800				3.750	3.750
Multiply*	6.000	6.300	6.300				6.250	6.250
Divide*	11.100	11.400	11.400				11.350	11.350
Compare*	2.600	2.900	2.900				2.850	2.850
EXTENDED FLOATING-POINT								
Load		1.300	1.300					
Store		1.000	1.000					
Add/Sub*	4.250	4.600	4.600					
Multiply*	12.150	12.500	12.500					
Divide*	23.100	23.450	23.450					
Compare*	2.750	3.400	3.400					
BRANCH								
	Taken 0.750	Not Taken 0.200						

*Includes no shifts in exponent adjust or normalization

Instruction Execution Times (Continued)

TABLE V. F9450 Instruction Execution Times in μs, for a 15 MHz Device

Basic Instruction	Register	Direct	Direct Index	Indirect	Immediate	Immediate Short	Base Relative	Relative Index
SINGLE PRECISION								
Load/Store	0.267	0.800	0.800	1.067	0.733	0.467	0.733	0.733
Add/Sub	0.333	0.867	0.867		0.800	0.533	0.800	0.800
Multiply	2.800	3.333	3.333		3.267		3.267	3.267
Divide	6.733	7.067	7.067		7.000		7.000	7.000
Compare	0.533	1.067	1.067		1.000	0.733	1.000	1.000
Set/Reset Bit	0.467	1.067	1.067	1.333				
DOUBLE PRECISION								
Load	1.067	1.467	1.467	1.733			1.400	1.400
Store		1.067	1.067	1.333			1.000	1.000
Add/Sub	1.200	1.600	1.600					
Multiply	8.667	9.067	9.067					
Divide	16.067	16.467	16.467					
Compare	1.400	1.800	1.800					
FLOATING-POINT								
Add/Sub*	6.067	6.467	6.467				6.400	6.400
Multiply*	8.000	8.400	8.400				8.333	8.333
Divide*	14.800	15.200	15.200				15.133	15.133
Compare*	3.467	3.867	3.867				3.800	3.800
EXTENDED FLOATING-POINT								
Load		1.733	1.733					
Store		1.333	1.333					
Add/Sub*	7.067	7.533	7.533					
Multiply*	16.200	16.667	16.667					
Divide*	30.800	31.267	31.267					
Compare*	3.667	4.533	4.533					
BRANCH								
	Taken	Not Taken						
	1.000	0.267						

*Includes no shifts in exponent adjust or normalization

Interrupts

There are 16 levels of interrupt prioritized on-chip, as listed in Table VI. Nine interrupts are external (PIR 0, 2, 8, 10–15), of which two are level-sensitive (IOL_1 INT, IOL_2 INT), and the other seven are either level- or edge-sensitive (USR_0 INT–USR_5 INT, PWRDN INT), according to the interrupt mode bit in the System Configuration Register. The remaining seven interrupts are internal to the CPU (PIR 1, 3–7, 9). All interrupts are latched into the Pending Interrupt Register (PIR) and may be disabled or masked by the Mask Register (MK), except as indicated in Table VI. All external interrupt inputs (except IOL_1 INT and IOL_2 INT) have hysteresis circuitry for noise immunity.

An enabled interrupt with highest priority that is not masked is processed as shown in *Figure 3*. Upon completion of the current instruction, which is not aborted, further interrupts are disabled. The F9450 then reads, via the Service Pointer (with AS = 0), the new Mask, Status Word, and Instruction Counter. It then stores, via the Linkage Pointer (with the new AS), the old Mask, Status Word, and Instruction Counter.

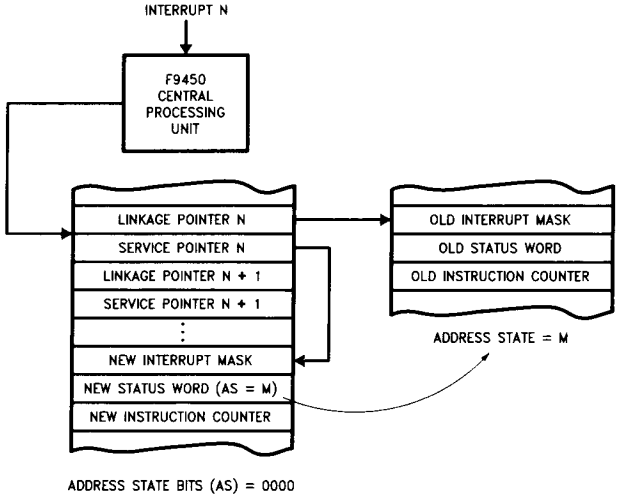


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FIGURE 3. Interrupt Vectors

TABLE VI. Interrupt Priorities

Interrupt	Priority (PIR/MK Bit Number)	Interrupt Linkage Pointer Address (Hex)	Interrupt Service Pointer Address (Hex)
Power Down (Note 1)	0 (Note 2)	20	21
Machine Error (Note 3)	1	22	23
User 0	2	24	25
Floating-Point Overflow	3	26	27
Fixed Point Overflow	4	28	29
Executive Call (Note 1)	5 (Note 4)	2A	2B
Floating Point Underflow	6	2C	2D
Timer A	7	2E	2F
User 1	8	30	31
Timer B	9	32	33
User 2	10	34	35
User 3	11	36	37
I/O Level 1	12	38	39
User 4	13	3A	3B
I/O Level 2	14	3C	3D
User 5	15	3E	3F

Note 1: Cannot be masked or disabled.

Note 2: Interrupt level 0 has the highest priority.

Note 3: Cannot be disabled.

Note 4: BEX is not part of the Interrupt priorities; it is the highest priority regardless of the PIR setting. The BEX instruction execution, once started, must complete before another interrupt can occur.

Interrupts (Continued)

Interrupts are acknowledged automatically by resetting the appropriate interrupt bit in the PIR and executing an I/O cycle, during which the acknowledged interrupt number is sent to I/O device 1000 (see *Figure 3*). For example, if interrupt level 11 is to be acknowledged, the CPU performs an I/O write cycle to address 1000 (in the I/O space) and writes data equal to FFEF (IB11 = 0, all other bits = 1). Level interrupt requests should be removed within two machine cycles after their respective interrupt acknowledge (IOW) cycle. If an additional delay in removing the interrupt request is needed in a particular system application, this period could be extended by inserting wait states.

The Pending Interrupt Register can be loaded via a privileged XIO instruction to generate simulated interrupts.

The Executive Call (software interrupt), invoked by the BEX instruction, provides a means to jump to a routine in another address state (AS). It is typically used to make controlled, protected calls to an executive, using one of 16 executive entry points.

The BEX instruction does not set PIR bit 5. However, if PIR bit 5 is set to 1 from program execution of SPI, a BEX = 0 will be executed.

Fault and Error Handling

Extensive fault handling, as required by real-time applications, involves the Fault Register, interrupt priority processing, and the abort scheme. Four levels of severity exist for faults and errors:

1. **Unrecoverable Errors**— errors with fatal implications for program execution. This class is recorded in the FT and will generate a machine error interrupt (priority level 1) that cannot be disabled. The five unrecoverable errors are:
   - — Illegal instruction
   - — Memory protect error on an instruction fetch
   - — Parity error on an instruction fetch
   - — External address error on an instruction fetch
   - — Address state fault
2. **Major Errors**— errors without fatal implications for program execution. This class is recorded in the FT and results in a machine error interrupt (priority level 1) after the instruction has completed execution. The three types of major errors are:
   - — Privileged instruction violation
   - — Memory protect or parity error on a CPU-initiated memory data bus cycle
   - — External address error on a CPU-initiated data bus (memory or I/O) read cycle
3. **Unclassified Errors (Warnings)**— are also recorded in the FT and will generate a machine error interrupt (priority level 1). See the "Fault Register (FT)" section for examples of unclassified errors.
4. **Arithmetic Errors**— other errors resulting from arithmetic exception cases (overflow, etc.). These are not recorded in the FT but in the PIR to generate lower-priority interrupts.

Note that the FT records unrecoverable, major, and unclassified errors from violations internal and external to the CPU. Any bit set in the FT will set PIR 1 and cause a level 1 interrupt. The FT can be cleared by the execution of the XIO instruction "CLR INT REQ" (2001 Hex), which also clears the PIR, or the instruction "READ AND CLEAR FT" (A00F Hex), which first transfers the contents of FT to the specified register and then clears FT and PIR 1, or by executing the console command EXAMINE AND CLEAR FAULT REGISTER (FT).

Instruction Abort

An instruction will be aborted by any one of three major errors:

- — Memory protect error ($\overline{\text{MEM PRT ER}}$)
- — Parity error ($\overline{\text{PAR ER}}$)
- — External address error ($\overline{\text{EXT ADR ER}}$) on a CPU-initiated data bus (memory or I/O) read cycle

Aborted instructions will complete execution, with modification of internal registers inhibited. Erroneous information may be written into memory or I/O locations. Outputs UNRCV ER (pin 8) and MAJ ER (pin 31) may be ORed together to form the ABORT input for the F9451 MMU (pin 13). If this peripheral is part of the system. This external ABORT signal may be connected to the Power Down Interrupt (PWRDN INT) input (pin 33) to ensure proper interrupt handling of the major and unrecoverable error conditions, even if the machine error interrupt (bit 1 of PIR) is masked out.

Three conditions will cause an effective NOP (i.e., the current instruction will not be executed and the next instruction will be fetched):

- — Two unrecoverable errors—illegal instruction and address state fault
- — One major error—privileged instruction violation

These conditions will set the appropriate bits in the FT and cause a machine error interrupt.

Note: The user should be aware that three unrecoverable errors,

- **— Memory protect error on instruction fetch**
- **— Parity error on instruction fetch**
- **— External address error on instruction fetch,**

result in a machine error interrupt. Because of the F9450 pipeline architecture, faults that occur during the instruction fetch result in an internal machine error interrupt which may occur before the instruction can be executed, providing the machine error interrupt is not masked.

Instruction Abort (Continued)

If the last machine cycle of an operation includes an instruction fetch, and the second word of the following instruction is fetched, and a fault occurs on this fetch, the new instruction will be executed before the interrupt occurs. However, the interrupt occurs prior to the execution of the next instruction, as required by MIL-STD-1750A.

Also, some instructions that transfer control to another part of the program may initiate the fetch of the following instruction before flushing the pipeline. If a fault occurs on this fetch, the interrupt will occur prior to the transfer of control. Provisions should be made by the user to handle these faults in the interrupt service routine.

Fault Register (FT)

The 16-bit-wide Fault Register records major (M), unrecoverable (U), or unclassified (W) faults during data or instruction fetch operations as shown in Table VII.

TABLE VII. Fault Register Bit Assignments

Bit	Fault	Errors		
		Major	Unrecoverable	Unclassified
0	CPU Memory Protect Error Data Cycle Instruction Fetch	M	 U	
1	Non-CPU Memory Protect Error			W
2	Parity Error Data Cycle Instruction Fetch		 U	W
3	Spare (Zero)			
4	Spare (Zero)			
5	Illegal I/O Address	M		
6	Spare (Zero)			
7	System Fault 0*			W
8	Illegal Memory Address Data Cycle Instruction Fetch	M	 U	
9	Illegal Instruction		U	
10	Privileged Instruction	M		
11	Address State Error		U	
12	Spare (Zero)			
13	BITE (Built-In Test) or System Fault 1*			W
14	Spare (Zero)			
15	System Fault 1*			W

*Signals $SYSFLT_0$ and $SYSFLT_1$ are asynchronous, edge-sensitive inputs to the F9450 processor and have hysteresis circuitry for noise immunity.

F9450 Component Description

The F9450 microprocessor architecture is organized in five sections, as illustrated in *Figure 4.*

— Data processor
— Microprogrammed control
— Address processor
— Interrupt and fault processor
— Timing unit

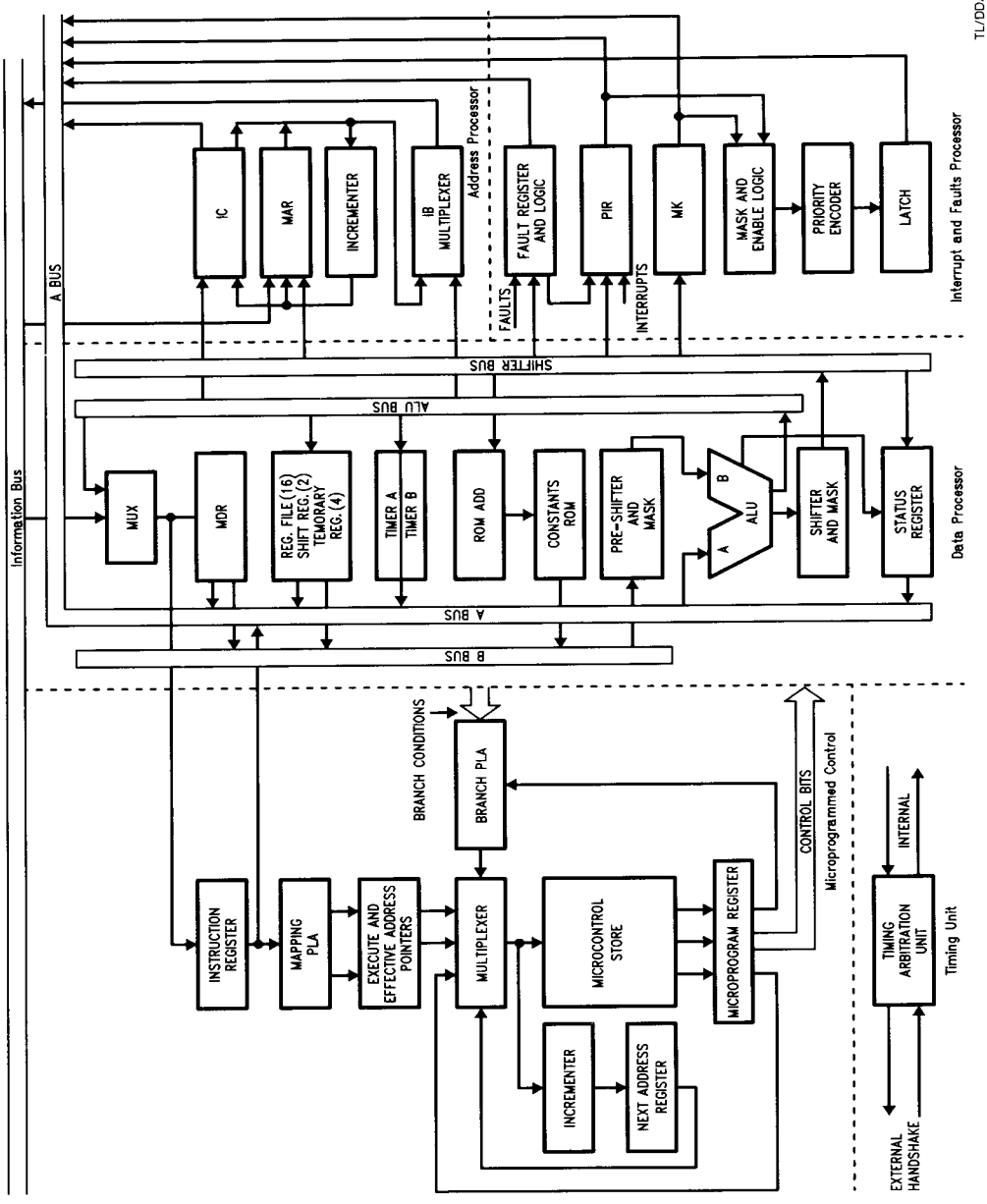


FIGURE 4. F9450 Block Diagram

Data Processor

The 16-bit-wide data processor section is responsible for all data processing in the CPU. It is organized in nine functional blocks:

—17-bit ALU

—Shifter and Mask

—16 general-purpose registers (R0–R15)

—Six temporary registers (including 2 Shift Registers)

—Memory Data Register (MDR)

—Two timers

—Constants ROM

—Status Word Register (SW)

—Pre-shifter and mask

Microprogrammed Control

The operation of the CPU is governed by a microprogrammed control section with two levels of pipelining. New instructions are fetched into the instruction register. The mapping PLA is fed from the instruction register and generates the pointers necessary for both execution and the effective address routines that reside in the microcontrol store. The microcontrol store generates three output fields to the microregister. Two—Next Address Field and Branch Field—determine the subsequent microaddress. The Output Field controls the operation of all CPU components.

Address Processor

The address processor includes an Instruction Counter (IC) and a Memory Address Register (MAR) that determine the addresses for all instructions and operands. Included in the Address Processor is an independent incrementer that provides Instruction Counter and operand address updates in parallel with data processor operation.

Interrupt and Fault Processor

All faults and interrupts, whether generated internally or externally, are handled by the Interrupt and Fault Processor. It includes the Pending Interrupt Register (PIR), Mask Register (MK), Fault Register (FT), interrupt enabling logic, and a priority encoder. Also included is abort condition detection and activation logic.

Timing Unit

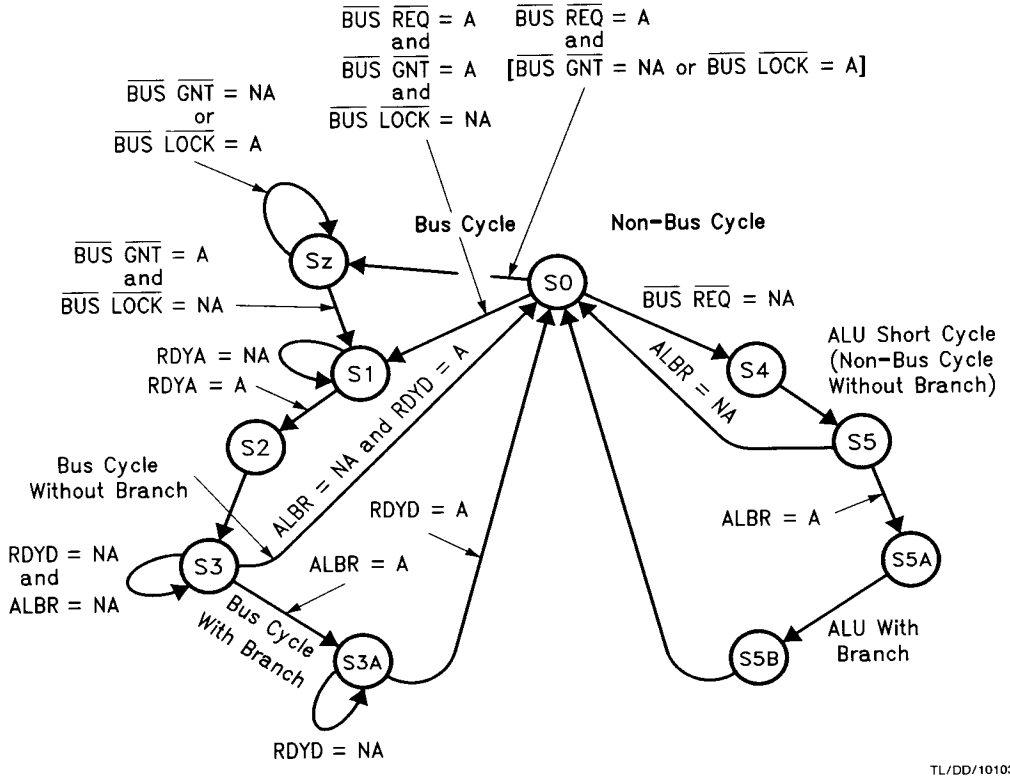
The Timing Unit generates the internal and external strobes required for internal CPU operation and the different bus transactions. A basic machine cycle could comprise three, four, or five CPU clock cycles (states), as illustrated in *Figure 5*.

1. A 3-state cycle (S_0, S_4, S_5) for pure internal ALU operations.
2. A 4-state cycle (S_0, S_1, S_2, S_3) for minimum length bus cycles.
3. A 5-state cycle (S_0, S_1, S_2, S_3, S_{3A} or S_0, S_4, S_5, S_{5A}, S_{5B}) applies for those cycles that use the result of the current ALU operation to determine the next address in the microprogrammed control store.

As shown in *Figure 5*, every timing cycle starts with state S_0, in which the timing unit receives the control information needed to initiate a bus cycle or a short ALU cycle.

A bus cycle can be extended indefinitely by manipulating the $\overline{\text{BUS GNT}}$, RDYA, or RDYD external inputs. The $\overline{\text{BUS GNT}}$ signal holds the CPU in the S_Z (high-impedance) state when the bus is assigned to another CPU or DMA device. The RDYA signal holds the CPU in the S_1 (address phase) state; the RDYD signal holds the CPU in the S_3 (data phase) state.

Timing Unit (Continued)



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Legend
A = Asserted (Active)
NA = Not Asserted
ALBR = ALU Branch Cycle (5 States)—Internal Signal Indicating Conditional Branch within Microcode
BUS REQ = Bus Request Output
BUS GNT = Bus Grant Output
BUS LOCK = Bus Lock from External Source
RDYA = RDYA Input
RDYD = RDYD Input
S_Z = High-Impedance State—CPU Drivers are TRI-STATE®

FIGURE 5. F9450 Timing Generator State Diagram

Self-Test and Initialization

The Self-Test is part of the Initialization sequence (see *Figure 6*) that is invoked by asserting the RESET signal. Asserting RESET forces the processor into an S_5 state on the next rising edge of the CPU clock, regardless of all other inputs. The processor remains in the S_5 state until RESET goes high, at which time the Self-Test sequence begins. The Self-Test functions are:

1. Reads and writes all registers in the register file.
2. Verifies ALU functions.
3. Checks multiply hardware by performing a multiply.
4. Checks divide hardware by performing a divide.
5. Checks ALU shifter in both directions by multiply and divide.
6. Verifies ROM constants can be accessed.
7. Verifies that the IC and MAR can be accessed and incremented.

If the Self-Test is successfully completed, the Normal Power Up (NML PWRUP) discrete output is set; otherwise, bit 13 in the Fault Register is set.

The Self-Test function reads the system configuration from I/O address 8410 into the SCR to determine the presence or absence of the MMU, BPU, Console, and Coprocessor, and also initializes the interrupt mode and then initializes the system, as shown in Table VIII.

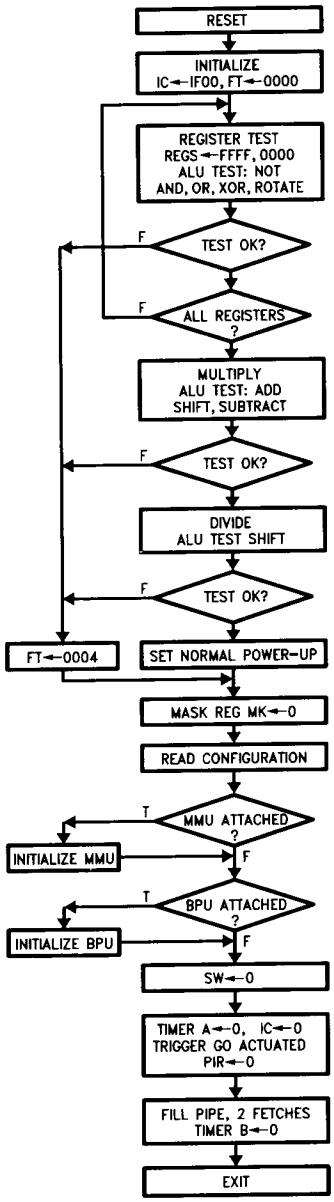
As depicted in the Self-Test flow chart *(Figure 6)*, while FT is originally set to all zeros, bit 13 is set any time a partial self-test is failed. Any external fault occurring prior to assertion of Normal Power Up causes a fault to be pending on completion of the self-test. From Normal Power-Up to the end of Initialization, the number of clock cycles can be determined from the figure, including the additional clock cycles spent for initializing the F9451 MMU and/or the BPU, if they are part of the system.

The Self-Test is intended to test useability of major functional sections of the F9450. It does **not** test all instructions or functions, but ensures basic operation of the F9450.

TABLE VIII. F9450 System Initialization

CPU	
Instruction Counter (IC)	All Zeros
Status Word (SW)	All Zeros
Fault Register (FT)	All Zeros
Pending Interrupt Register (PIR)	All Zeros
Interrupt Mask Register (MK)	All Zeros
Interrupt	Disabled
DMA Enable	Disabled
Timer A and Timer B	All Zeros and Counting Up
Trigger Go Reset ($\overline{\text{TRIGO RST}}$)	Pulsed
Normal Power Up (NML PWRUP)	Set High
MMU	
Page Registers	
AL Field	All Zeros
W Field	All Zeros
E Field	All Zeros
PPA Field	Logical to Physical
BPU	
CPU Write Protect Registers	All Zeros
DMA Write Protect Registers	All Zeros
Global Memory Protect	Enabled

Self-Test and Initialization (Continued)



I/O ADDRESS	DATA	REMARKS	CLOCK CYCLE	
1F00	XXXX	IOW	12	
1F01	FFFF			
02	0000			
03	0000			
04	FFFF			
05	0000			
06	0000	IOW	294	
07	FFFF			
08	0000			
09	0000			
.	.			
.	.			
.	.			
1F30	000			
1F31	0000	IOW	40	
1F32	0000	IOW		
1F33	000F	IOW	63	
1F34	0000	IOW		
			16	
8410		IOR		
5200	0000			
5100	0000		5	
5201	0001			
5101	0001			
5202	0002			
5102	0002	IOW	3334	IF MMU PRESET
.	.			
.	.			
.	.			
52FF	00FF		5	
51FF	00FF			
5000-507F	0000	IOW	1158	IF BPU PRESENT
			20	

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Note: The purpose of the I/O Write (IOW) addresses is to inform the user of the presently executed instruction in the self-test program. The user must furnish bus control signals to the CPU to enable it to continue the self-test sequence.

FIGURE 6. Self-Test and Initialization Sequence

Console Operations

The F9450 offers a feature that is unique among microprocessors: the capability of being connected to a programmer's console. This connection gives the programmer the ability to examine and change the contents of various registers within the CPU, the system memory, and the I/O subsystems.

The F9450 console is treated as three input/output addresses:

1. Console command 8400H
2. Console data read address (switches) 8401H
3. Console data write address (displays) 0400H

Entering Console Mode

The Console Mode is entered in one of two ways:

1. Drive the $\overline{\text{CON REQ}}$ input low. The CPU completes the current instruction, executes an I/O cycle to read the console command from the information bus (I/O address 8400H), and then executes the console command. (See Table IX for a list of the valid console operations and their corresponding codes.) Console operations typically involve I/O address 8401H to enter console data and/or 0400H to write data to the console.
2. Execute the BPT instruction. The CPU reads the system configuration bits from I/O address 8410H. If the console bit is reset, the CPU treats the BPT instruction as a NOP instruction. Otherwise, it enters Console Mode and waits for a console request.

When responding to a Console Request, the F9450 executes the user-specified console command and then goes into a loop, waiting for the $\overline{\text{CON REQ}}$ signal to be asserted.

Use of Console Mode

The sequence of console operations follows. (See *Figure 7*, a flow chart of the console handshake.)

1. The Console Request ($\overline{\text{CON REQ}}$) input (pin 2), which has a higher priority than interrupts, is activated. It is sampled at the beginning of the last microcycle of each instruction.
2. On completing the instruction that is being executed and recognizing the console request, the processor enters the Console Mode and halts Timer A and Timer B. They resume counting from this same point when the CPU exits its console operations.
3. The CPU issues an I/O Read command using I/O address 8400H. At that time, the $\overline{\text{CON REQ}}$ signal should be deactivated and the console command placed on the bus.
4. On decoding this console command, the CPU proceeds through the proper steps to execute the command. Often this includes additional I/O cycles to either read data or an address from the console (I/O address 8401H) or to write data to the console (I/O address 0400H).
5. At this time, the CPU remains in the Console Mode and waits for the $\overline{\text{CON REQ}}$ signal to be reasserted.

Exiting Console Mode

The Console Mode is exited in one of two ways:

1. If an interrupt is pending when the CPU is executing a DISABLE command, the CPU services the interrupt and returns to the normal mode of operation, fetching and executing instructions from the system memory.

   If no interrupt is pending at this time, the CPU remains in an intermediate state, alternately checking for pending interrupts or a console request.
2. The CPU executes a console CONTINUE command.

Notes

The F9450 executes the EXAMINE MEMORY console command by reading the address from I/O address 8401, storing that address into the IC, reading memory at that address, and then writing that data to I/O address 0400. When the EXAMINE NEXT command is executed, the F9450 first increments the IC, reads memory at the address specified by the IC, and then writes that data to I/O address 0400.

The DEPOSIT MEMORY command deposits the user-provided data (from I/O address 8401) into the memory location pointed to by the F9450 Instruction Counter (IC). When the DEPOSIT NEXT command is executed, the F9450 first increments the IC and then stores the user-provided data into the memory location pointed to by the new value of the IC.

The EXAMINE XIO console command reads the I/O address from I/O location 8401 and saves that address in A1 (one of the F9450 internal scratchpad registers). The CPU then performs an I/O read from the address in A1 and writes that data to I/O address 0400. The DEPOSIT XIO command writes the user-specified data to the I/O address contained in A1. This console command expects the I/O address to be preloaded in register A1 by one of two methods:

1. Through the DEPOSIT REGISTER console command.
2. Execute an EXAMINE XIO command before executing a DEPOSIT XIO command.

When executing the EXAMINE NEXT XIO and DEPOSIT NEXT XIO console commands, the F9450 first increments register A1 and then performs the appropriate transfer with the I/O location pointed to by the new value of A1. While normally the most significant bit (MSB) of the I/O address indicates direction (read or write), this is not true for four console commands: EXAMINE XIO, DEPOSIT XIO, EXAMINE NEXT XIO, and DEPOSIT NEXT XIO.

During console commands that generate a bus cycle, the state of the D/I line is 1 (Data cycle). An illegal console command is treated as a NOP instruction and the CPU waits for another console request.

The processor CANNOT be single-stepped by maintaining an active CON REQ signal and repeatedly responding to the I/O read at 8400H with the CONTINUE command. If this is done, the CPU recognizes the CON REQ before executing the instruction and never exits the Console Mode. To perform the single-step operation, the CONTINUE command is executed and the CON REQ signal is activated immediately on recognizing the second fetch from instruction space in the system memory.

Notes (Continued)

If an external fault (EXT ADR ER, MEM PRT ER, or PAR ER) occurs during a console operation, the register file is protected in the same manner as if an instruction were in process. None of the 16 general-purpose registers or the six temporary registers can be modified until the processor exits the Console Mode. To exit the Console Mode, execute a console CONTINUE command or reset the processor.

National's application Note MC-2, 'Simple Console Controller for the F9450", describes how a specially programmed MOSTEK 38P70 microcontroller can be implemented to control the Console function of the F9450.

TABLE IX. Console Command Formats

0	7	8 (Note 1)	9	10							15
CONSOLE CODE		**X**	**X**	**REGISTER ADDRESS**							
Console Code and Command (Hex)				**Binary**						**Hex**	**Reg.**
74: DISABLE (1) (Notes 2, 3)				0	0	0	0	0	0	(00)	R0
60: EXAMINE REGISTER (1)				0	1	0	0	0	0	(10)	R1
61: DEPOSIT REGISTER (2)				0	0	0	0	0	1	(01)	R2
62: EXAMINE AND CLEAR				0	1	0	0	0	1	(11)	R3
FAULT REGISTER (FT)(1) (Note 3)				0	0	0	0	1	0	(02)	R4
63: DEPOSITE STATUS WORD (SW) (2) (Note 3)				0	1	0	0	1	0	(12)	R5
66: EXAMINE MEMORY (2) (Note 3)				0	0	0	0	1	1	(03)	R6
67: DEPOSIT MEMORY (2) (Note 3)				0	1	0	0	1	1	(13)	R7
6A: EXAMINE NEXT MEMORY (1) (Note 3)				0	0	0	1	0	0	(04)	R8
6B: DEPOSIT NEXT MEMORY (2) (Note 3)				0	1	0	1	0	0	(14)	R9
75: CONTINUE (1) (Note 3)				0	0	0	1	0	1	(05)	R10
6C: EXAMINE XIO (2) (Note 3)				0	1	0	1	0	1	(15)	R11
6D: DEPOSIT XIO (2) (Note 3)				0	0	0	1	1	0	(06)	R12
6E: EXAMINE NEXT XIO (1) (Note 3)				0	1	0	1	1	0	(16)	R13
6F: DEPOSIT NEXT XIO (2) (Note 3)				0	0	0	1	1	1	(07)	R14
				0	1	0	1	1	1	(17)	R15
				0	0	1	0	0	0	(08)	A2
				0	1	1	0	0	0	(18)	A1
				0	0	1	0	0	1	(09)	Q2
				0	1	1	0	0	1	(19)	Q1
				0	0	1	0	1	0	(0A)	DO0
				0	1	1	0	1	0	(1A)	DO1
				0	0	1	0	1	1	(0B)	PIR
				0	1	1	0	1	1	(1B)	MK
				0	0	1	1	0	0	(0C)	FT (Note 4)
				0	0	1	1	0	1	(0D)	SW (Note 5)
				0	0	1	1	1	0	(0E)	TA
				0	1	1	1	1	0	(1E)	TB
				1	0	0	1	0	1	(25)	IC (Note 5)
				1	0	1	1	X	X	(2C–2F)	IR

Note 1: Bits 8 and 9 are always "Don't Care."

Note 2: The (1) and (2) designations indicate a 1- or 2-word-long console command:

(1) indicates command only

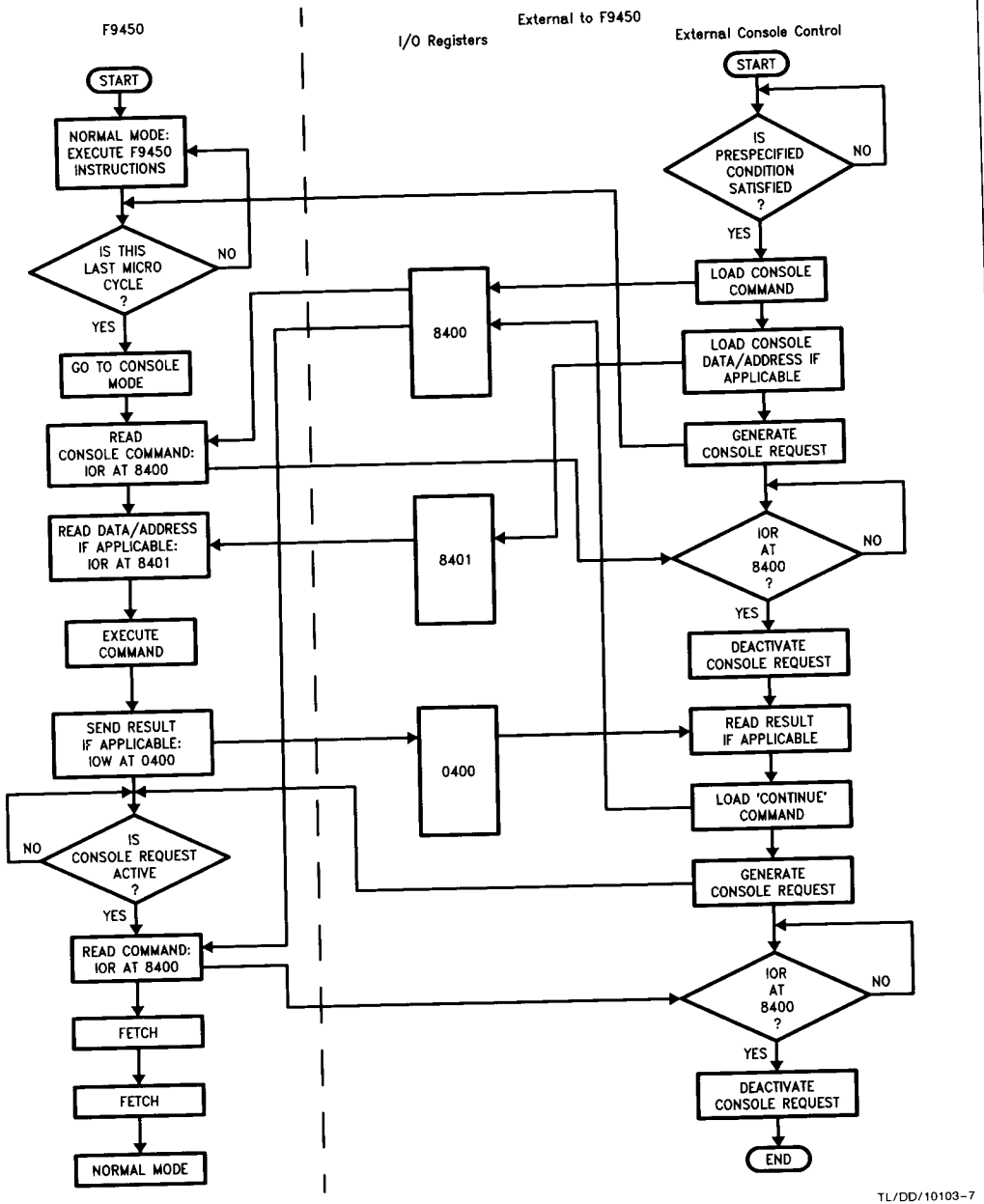
(2) indicates command and data

Note 3: For commands that do not require a register address, bits 10 through 15 are "Don't Care".

Note 4: In executing the DEPOSIT REGISTER command (61 Hex), only bits 9, 10, 11 and 13 of the Data Word can be deposited into the FT register. These four bits are user-specified with the inverted polarity. The remaining 12 bits are Don't Care; e.g., to set bits 10, 11, 13 to a one and bit 9 to a zero, Data Word XXXX XXXX X100 X0XX must be supplied from I/O location 8401.

Note 5: Only the EXAMINE REGISTER command applies to the Status WORD (SW) and Instruction Counter (IC) registers. To deposit (Load) the IC with a 16-bit value, the EXAMINE MEMORY console command is used. The address specified in this command (the second word) is automatically loaded into the IC.

Notes (Continued)



IOR = I/O Read
IOW = I/O Write

FIGURE 7. F9450 Console Handshake Sequence

Signal Descriptions

The F9450 input and output signals are described in Table X.

TABLE X. F9450 Signal Descriptions

Mnemonic	Pin No.	Name	Description
CLOCKS			
CPU CLK	51	CPU Clock	Single-phase input clock signal (specified frequency, 40% to 60% duty cycle).
TIMER CLK	17	Timer Clock	A 100 kHz input that, after synchronization with CPU CLK, provides the clock for Timer A and Timer B. If timers are used, the CPU CLK signal frequency must be > 500 kHz (40% to 60% duty cycle).
EXTERNAL REQUESTS			
$\overline{\text{RESET}}$	5	Reset	An active-low input that initializes the F9450. The processor must be $\overline{\text{RESET}}$ after input power (V_{CC}, I_{INJ}) is within spec and stable, to ensure proper operation.
$\overline{\text{CON REQ}}$	2	Console Request	An active-low input that initiates console operations after the current instruction.
INTERRUPTS			
PWRDN INT	33	Power Down Interrupt	An input interrupt request that cannot be masked or disabled. This signal is active on the positive-going edge or the high level, according to the interrupt mode bit in the configuration register. This input has hysteresis circuitry for noise immunity.
USR_0 INT – USR_5 INT	34–39	User Interrupt	Input signals that are active on the positive-going edge or high level, according to the interrupt mode bit in the configuration register. These inputs have hysteresis circuitry for noise immunity.
IOL_1 IOL_2	40, 41	I/O Level Interrupts	Active-high inputs that can be used to expand the number of user interrupts.
FAULTS			
$\overline{\text{MEM PRT ER}}$	26	Memory Protect Error	An active-low input generated by the MMU or BPU, or both, and sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault Register (bit 0 if CPU bus cycle, bit 1 if non-CPU bus cycle).
$\overline{\text{PAR ER}}$	27	Parity Error	An active-low input sampled by the $\overline{\text{BUS BUSY}}$ signal into bit 2 of the Fault Register.
$\overline{\text{EXT ADR ER}}$	28	External Address Error	An active-low input sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault Register (bit 5 or 8), depending on the cycle (memory or I/O).
$SYSFLT_0$ $SYSFLT_1$	29, 30	System Fault 0 System Fault 1	Asynchronous, positive-edge-sensitive inputs to the F9450 that set bit 7 ($SYSFLT_0$) or bits 13 and 15 ($SYSFLT_1$) in the Fault Register. These inputs are protected from system noise through hysteresis circuitry.

Signal Descriptions (Continued)

TABLE X. F9450 Signal Descriptions (Continued)

Mnemonic	Pin No.	Name	Description
INFORMATION BUS			
IB_0–IB_{15}	9–18, 20–25	Information Bus	An active-high, bidirectional, time-multiplexed address/data bus that is TRI-STATE during bus cycles not assigned to this CPU; IB_0 is the most significant bit.
STATUS BUS			
AK_0–AK_3	47–50	Access Key	Active-high outputs used to match the Access Lock in the MMU for memory accesses (a mismatch is one of several possible situations that cause the MMU to pull the $\overline{\text{MEM PRT ER}}$ signal low). These signals are TRI-STATE during bus cycles not assigned to this CPU.
AS_0–AS_3	42–45	Address State	Active-high outputs that select the page register group in the MMU; TRI-STATE bus during bus cycles not assigned to this CPU. These outputs together with D/$\overline{\text{I}}$ can be used to expand the F9450 direct addressing range to 2M words.
ERROR CONTROL			
UNRCV ER	8	Unrecoverable Error	An active-high output that indicates the occurrence of an error classified as unrecoverable.
MAJ ER	31	Major Error	An active-high output indicating the occurrence of an error classified as major.
DISCRETE CONTROL			
DMA EN	3	Direct Memory Access Enable	An active-high output that indicates the DMA is enabled. It is disabled when the CPU is initialized (reset) and is enabled under program control.
NML PWRUP	6	Normal Power Up	An active-high output that is set when the CPU has successfully completed the built-in test in the initialization sequence.
SNEW	63	Start New	An active-high output, used for debug purposes, that indicates a new instruction will start executing in the next machine cycle. Signal is valid at frequencies up to $\frac{1}{2}F_{Max}$.
$\overline{\text{TRIGO RST}}$	4	Trigger Go Reset	An active-low discrete output. This signal can be pulsed low under program control [I/O address 400B (Hex)] and is automatically pulsed once during processor initialization.
BUS CONTROL			
D/$\overline{\text{I}}$	58	Data or Instruction	An output signal that indicates whether the current bus cycle access is for Data (high) or Instruction (low); TRI-STATE during bus cycles not assigned to this CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
R/$\overline{\text{W}}$	57	Read or Write	An output signal that indicates direction of data flow with respect to the current bus master: a high indicates a read or input operation and a low indicates a write or output operation. The signal is TRI-STATE during bus cycles not assigned to this CPU.
M/$\overline{\text{IO}}$	59	Memory or I/O	Output signal that indicates whether the current bus cycle is memory (high) or I/O (low). This signal is TRI-STATE during bus cycles not assigned to this CPU.

Signal Descriptions (Continued)

TABLE X. F9450 Signal Descriptions (Continued)

Mnemonic	Pin No.	Name	Description
BUS CONTROL (Continued)			
STRBA	52	Address Strobe	An active-high output that can be used to externally latch the memory or I/O address at the high-to-low transition of the strobe. The signal is TRI-STATE during bus cycles not assigned to this CPU.
RDYA	55	Address Ready	An active-high input that can be used to extend the address phase of a bus cycle. When RDYA is not active, wait states are inserted by the F9450 timing unit to accommodate slower memory or I/O devices.
$\overline{\text{STRBD}}$	53	Data Strobe	An active-low output that can be used to strobe data in memory and XIO cycles. This signal is TRI-STATE during bus cycles not assigned to this CPU.
RDYD	56	Data Ready	An active-high input that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the F9450 timing unit to accommodate slower memory or I/O devices.
BUS ARBITRATION			
$\overline{\text{BUS REQ}}$	54	Bus Request	An active-low output that indicates the CPU requires the bus; becomes inactive when the CPU has acquired the bus and started the bus cycle.
$\overline{\text{BUS GNT}}$	61	Bus Grant	An active-low input from an external arbiter that indicates the CPU currently has the highest priority bus request. If the bus is not locked, the CPU may begin a bus cycle, commencing with the next CPU clock.
$\overline{\text{BUS BUSY}}$	60	Bus Busy	An active-low bidirectional signal used to establish the beginning and end of a bus cycle. The trailing edge (low-to-high transition) is used for sampling bits into the Fault Register. It is TRI-STATE in bus cycles not assigned to this CPU; however, the CPU monitors the $\overline{\text{BUS BUSY}}$ line for latching non-CPU bus-cycle faults into the Fault Register.
$\overline{\text{BUS LOCK}}$	62	Bus-Lock	An active-low, bidirectional signal used to lock the bus for successive bus cycles. During non-locked bus cycles, the $\overline{\text{BUS LOCK}}$ signal mimics the $\overline{\text{BUS BUSY}}$ signal. It is TRI-STATE during bus cycles not assigned to this CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB, STLB.
POWER			
V_{CC}	64	Power Supply	+5V, 270 mA typical power supply.
GND	1, 32	Ground	0V reference. **These pins should be tied together as close to the chip as possible.**
I_{INJ1}, I_{INJ2}	19 46	Injector Current	Current source to provide bias (1.1A Nominal) for the injection logic. **These pins should be tied together as close to the chip as possible.**

Device Operation

Bus Transactions

Bus transactions are four or five states long (a state is equivalent to one CPU clock period). Memory and I/O cycles have identical timing requirements and are distinguished by the status of the M/$\overline{IO}$ line.

The $\overline{BUS\ REQ}$ output is activated during the S0 state, indicating to the external arbiter (if any) that this CPU requests the bus. At the end of state S0, the CPU samples the status of the $\overline{BUS\ GNT}$ and $\overline{BUS\ LOCK}$ inputs. If $\overline{BUS\ GNT}$ has been active and $\overline{BUS\ LOCK}$ inactive, satisfying the minimum set-up time, state S1 is entered. Otherwise, the CPU enters the high-impedance state, S_Z, waiting for $\overline{BUS\ GNT}$ to be active (in a single processor system, no arbiter is needed and the $\overline{BUS\ GNT}$ pin can be wired low) and $\overline{BUS\ LOCK}$ to be inactive (since $\overline{BUS\ LOCK}$ is TRI-STATE, it should be pulled high by a resistor to V_{CC}). Refer to *Figure 8*.

Once in S1, the $\overline{BUS\ REQ}$ signal is made inactive to allow bus contenders to bid early for the next bus cycle. The CPU activates the $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$, and status signals, and outputs the address after some delay (measured from the start of the S1 state). At the end of S1, the CPU samples the RDYA input. If low, the CPU stays in the S1 state, extending the address phase on the bus. Otherwise, it proceeds to state S2, and then to state S3.

Once in state S2, the CPU makes the STRBA signal low (this edge is used to latch the address in an external address latch) and, for Read cycles only, activates the $\overline{STRBD}$ output, where the CPU prepares to receive data by turning the address/data bus around. For Write cycles, the CPU starts driving the bus with the write data immediately after the address. The $\overline{STRBD}$ signal is activated during S3, allowing both a reasonable set-up time for the write data to $\overline{STRBD}$ falling edge and a reasonable hold time for the $\overline{STRBD}$ rising edge to write data. The RDYD signal is sampled at the end of S3 and the bus cycle is terminated when RDYD is high; otherwise, it stays in the S3 state. At the end of the bus cycle, all CPU outputs are TRI-STATE. Note that the STRBA, $\overline{STRBD}$ and IB_0–IB_{15} signals for the Write cycles are actively driven through S0 of the next cycle.

All XIO/VIO output commands and internal input commands (e.g. move contents of such internal special registers as MK to an internal general-purpose register, such as R0) are echoed back externally in the form of an I/O Write cycle. The address is the command itself, and the write data is the result of the execution phase, if applicable. The system must provide the RDYA and RDYD signals in these cycles.

Table XI gives the typical memory subsystem access times required by the system at various operating frequencies. The access time includes address latches, address decoder delays, and system memory chip enable access.

TABLE XI. Typical Memory Subsystem Access Time Requirements

CPU Clock (MHz)	System Memory Address Access Time (ns)				
	No Wait	1 Wait	2 Waits	3 Waits	4 Waits
20	90	140	190	240	290
18	107	162	218	273	329
15	135	202	269	335	402

Note: A wait state is inserted due to either the RDYA or RDYD signal being inactive when sampled by the CPU at the proper time.

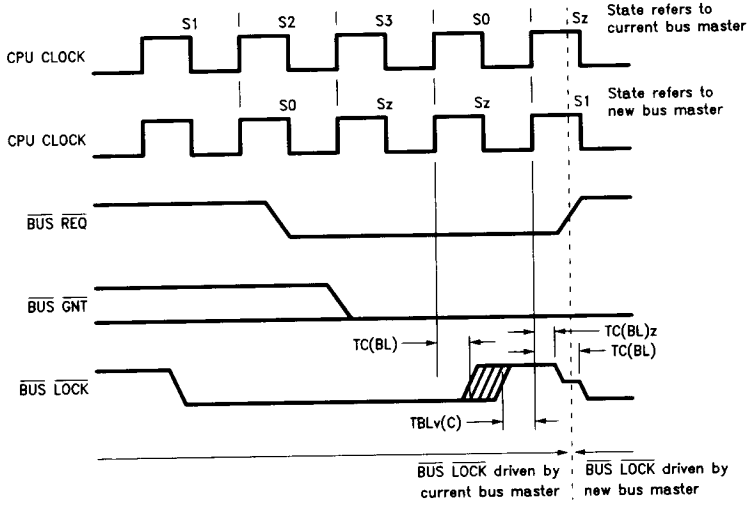


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FIGURE 8. Bus Access Signal Requirements

Note 1: All device masters are F9450 or F9450 bus-compatible devices.

Note 2: Bus masters and external arbiter are operating on the same clock.

Note 3: State S_z is the high-impedance state in which all new bus master drivers are in a TRI-STATE condition.

Note 4: Do not scale.

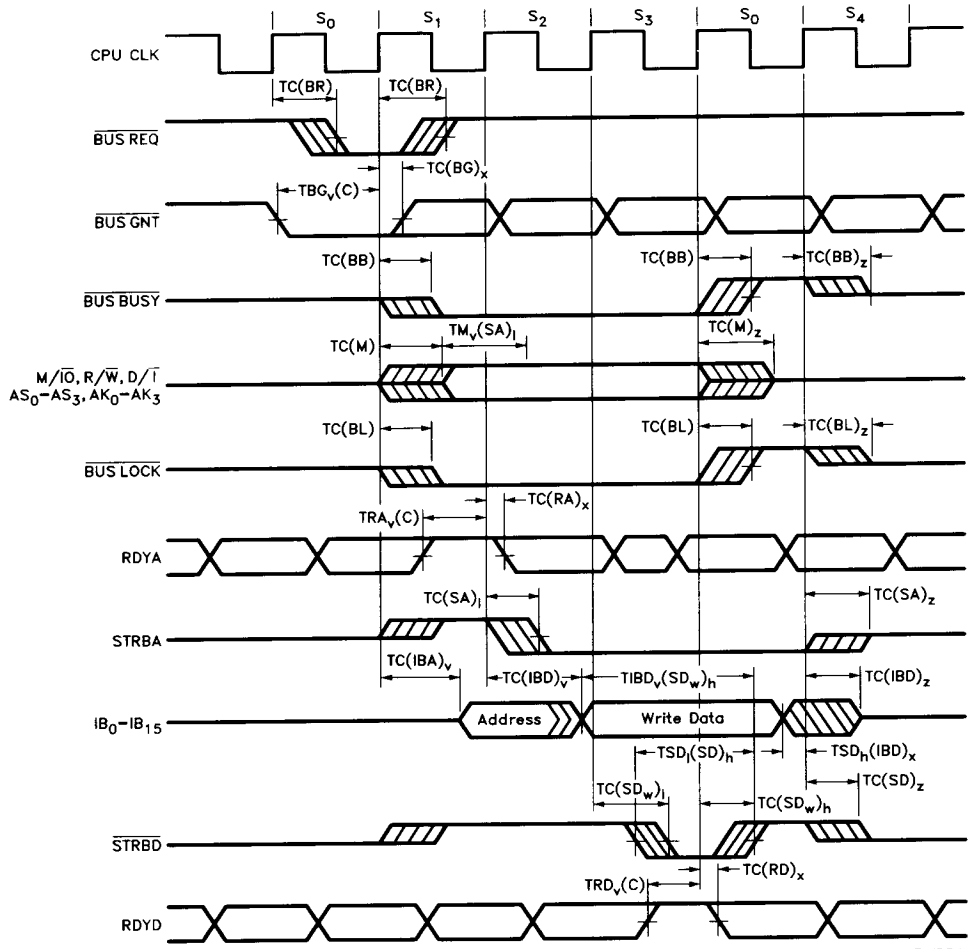
Timing Characteristics

The F9450 timing characteristics are shown in *Figures 9* through *19* and described in Table XII. A switching time test circuit is shown in *Figure 20*.

The abbreviated symbol convention used for timing parameters in this datasheet in TAb(C)d, where:

- Timing symbols all being with the letter "T".
- The mnemonic in the position represented by "A" indicates the signal node beginning the interval.
- The mnemonic in the position represented by "b" defines the direction of signal transition at the beginning node, if such definition is necessary; the new state of the signal may be low (l), high (h), TRI-STATE (z), don't care (x), or valid (v).
- The mnemonic in the position represented by "(C)", which always appears in the parentheses, indicates the signal node ending the interval.
- The mnemonic in the position represented by "d" is the same as "b", but refers to the state of the signal at the node indicated by the mnemonic in position "(C)".
- The mnemonics in the positions represented by "b" and "d" are not used for reference to the CPU CLK signal, as it is assumed to be active on the rising edge.

For example, TF(BB) is the setup time from a valid fault ($\overline{\text{EXT ADR ER}}$, $\overline{\text{MEM PRT ER}}$, $\overline{\text{PAR ER}}$) input to $\overline{\text{BUS BUSY}}$.



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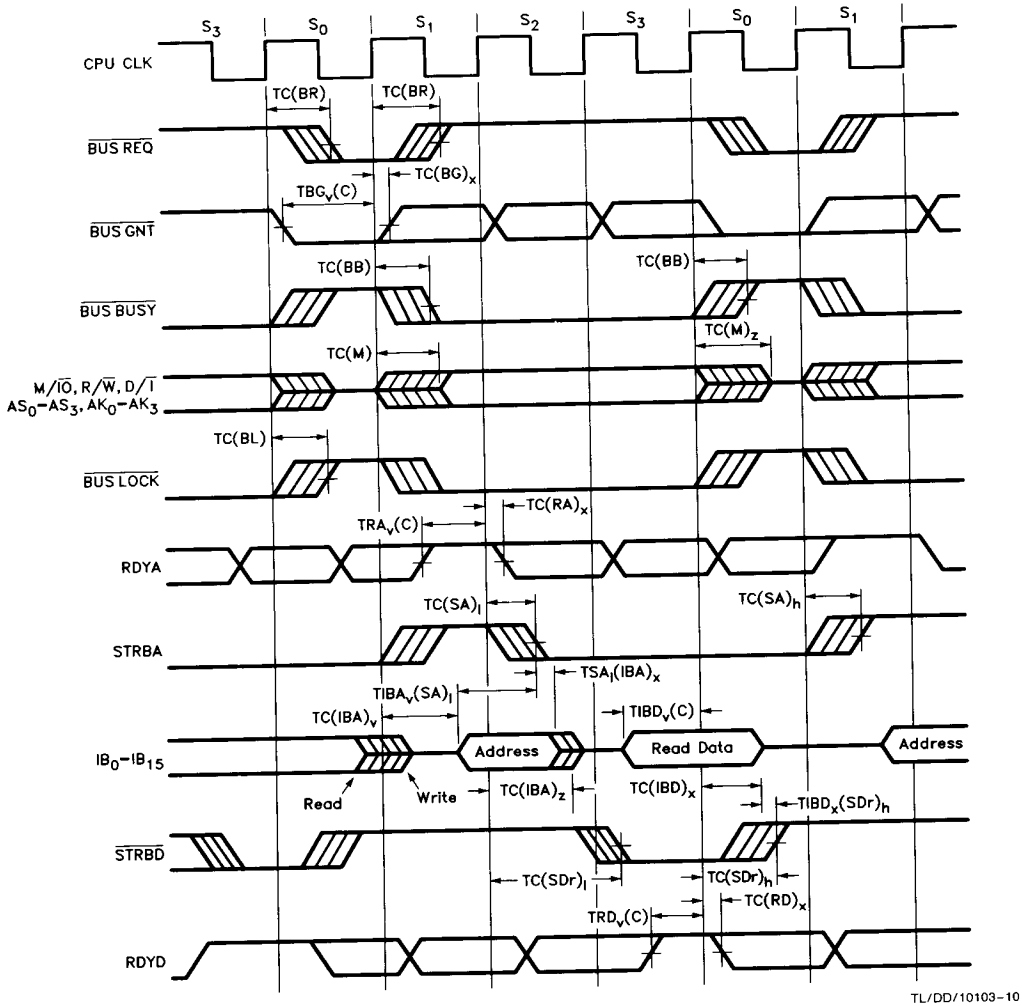
Note 1: Shown is a **single isolated bus cycle,** only one bus master.

Note 2: An intermediate level indicates that the CPU has placed this signal in a TRI-STATE condition.

Note 3: Do not scale.

FIGURE 9. Minimum Write Bus Cycle Timing Diagram

Timing Characteristics (Continued)



Note 1: Shown are **three consecutive bus cycles**, only one bus master.

Note 2: Do not scale.

FIGURE 10. Minimum Read Bus Cycle Timing Diagram

Timing Characteristics (Continued)

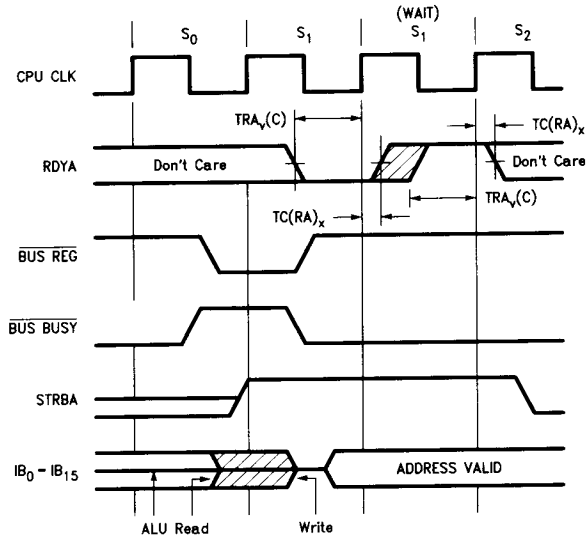


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FIGURE 11. RDYA Signal Timing Diagram

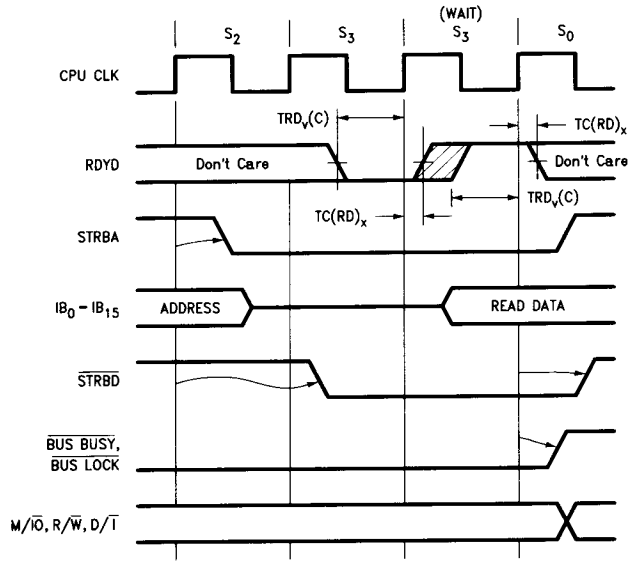

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FIGURE 12. RDYD Signal—Read Bus Cycle Timing Diagram

Timing Characteristics (Continued)

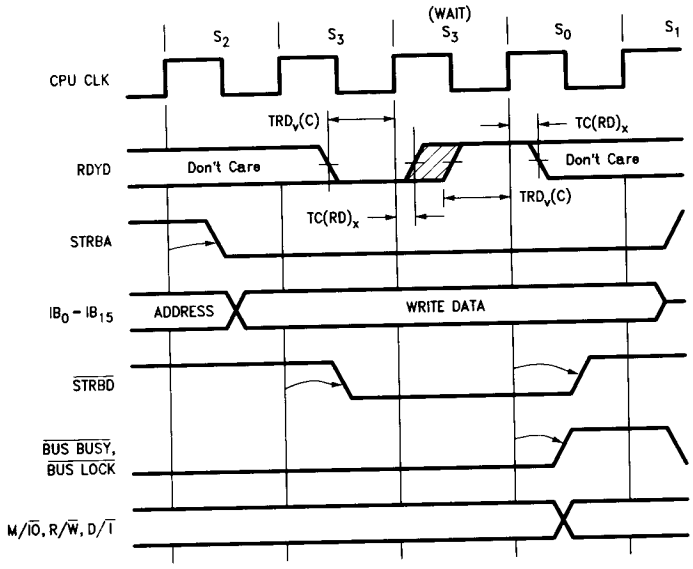

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FIGURE 13. RDYD Signal—Write Bus Cycle Timing Diagram

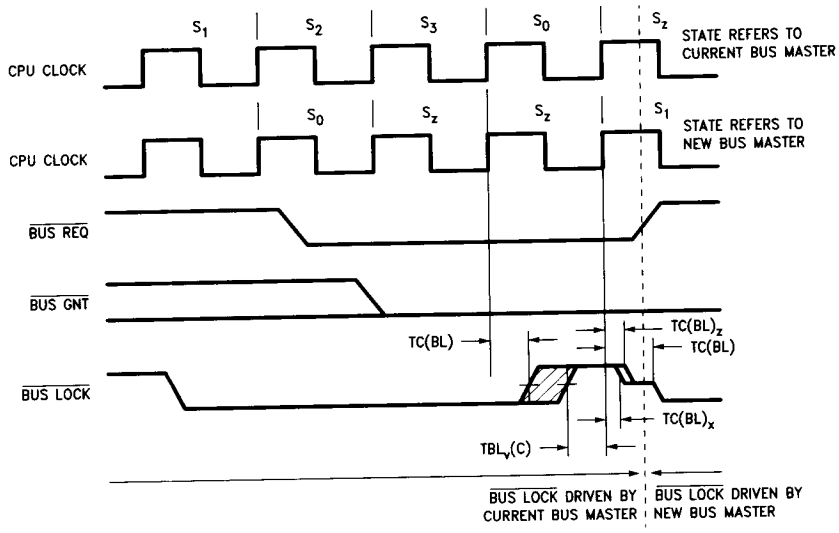

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FIGURE 14. Signal Requirements for Accessing Bus

Note 1: Shown is device response to external control of the $\overline{BUS\ LOCK}$ signal. Note that current bus master must release active drive of $\overline{BUS\ LOCK}$ before new bus master begins driving.

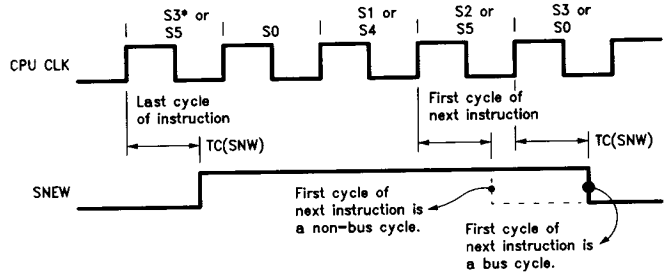
Note 2: All device masters are F9450 or F9450 bus-compatible devices.

Note 3: Bus masters and external arbiter are operating on the same clock.

Note 4: State S_Z is the high-impedance state in which all new bus master drivers are in a TRI-STATE condition.

Note 5: Do not scale.

Timing Characteristics (Continued)



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*If Wait states are included in the data time of the previous cycle, this will be the first S3 state.

FIGURE 15. SNEW Discrete Timing Diagram

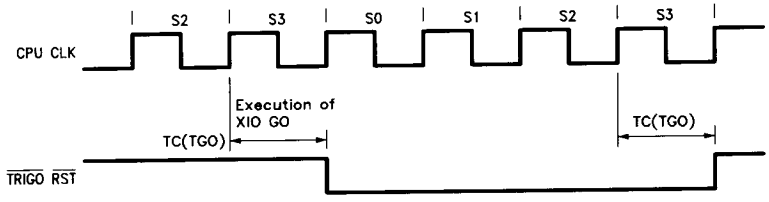

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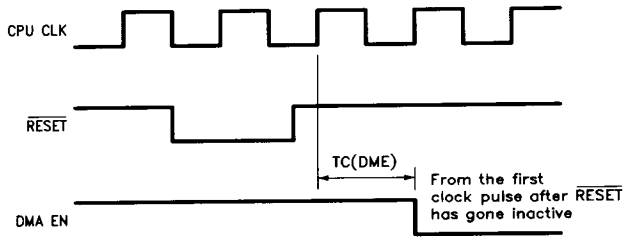
FIGURE 16. $\overline{\text{TRIGO RST}}$ Discrete Timing Diagram

A) During RESET



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B) XIO Operations

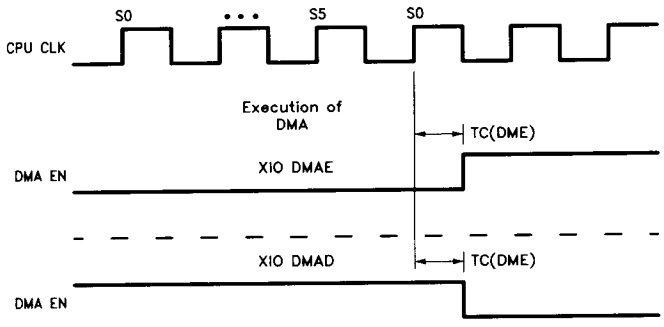

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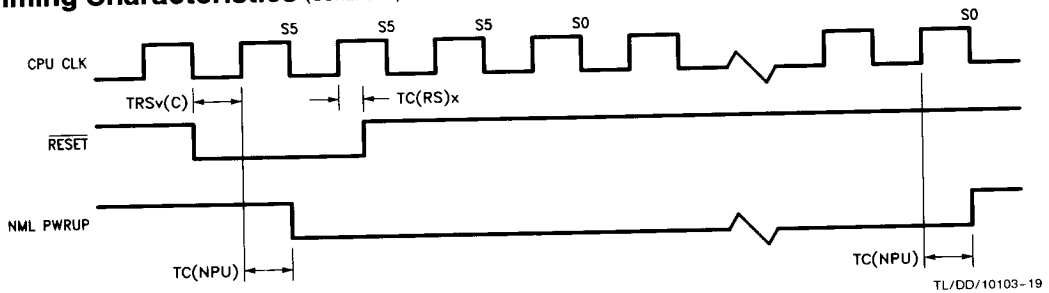
FIGURE 17. DMA EN Discrete Timing Diagram

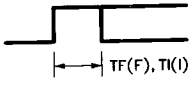
Timing Characteristics (Continued)



Note: The CPU will remain in the S5 state as long as $\overline{\text{RESET}}$ is held low.

FIGURE 18. Normal Power Up Discrete Timing Diagram

A) Edge-Sensitive Interrupts and Faults ($SYSFLT_0$, $SYSFLT_1$) Min. Pulse Width



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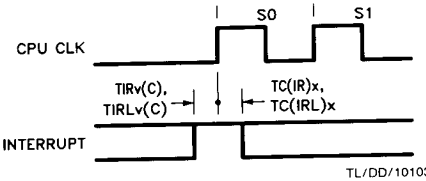
B) Level-Sensitive Interrupts



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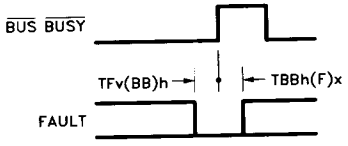
C) Level-Sensitive Faults



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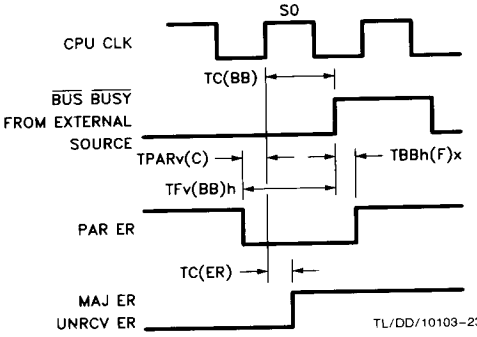
D) PAR ER



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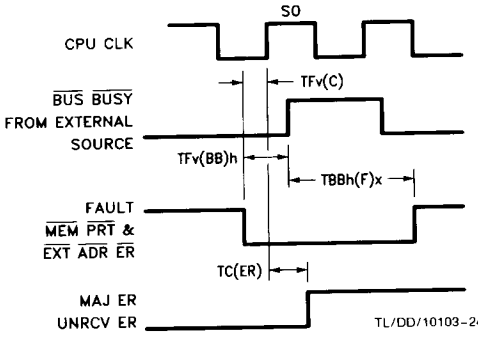
E) FAULT



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F) CON REQ

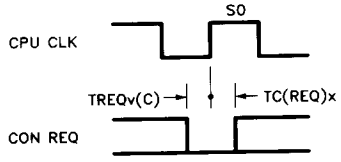

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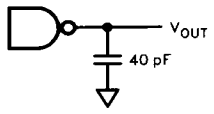
FIGURE 19. External Faults and Interrupts Timing Diagram

Timing Characteristics (Continued)

Standard Output



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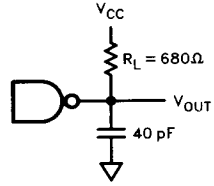
Open-Collector Output



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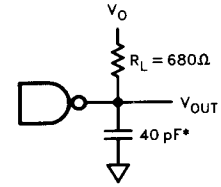
TRI-STATE



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*80 pF for Bi-Directional Pins

Note: Do not scale.

FIGURE 20. Switching Time Test Circuits

Parameter	V_O	V_{MEA}
T_{PLZ}	V_{CC}	V_{OUT} + 0.1V
T_{PHZ}	GND	V_{OUT} − 0.1V

TABLE XII. F9450 Timing Characteristics

Symbol	Description	15DC, 15GC 15DM, 15GM			F15DC, F15GC F15DM, F15GM F18DC, F18GC F18DM, F18GM F20DC, F20GC F20DM, F20GM			Notes
		Units (ns)			Units (ns)			
		Min	Typ	Max	Min	Typ	Max	
PROPAGATION DELAY FROM CLOCK								
TC(M)	M/$\overline{IO}$, D/I, R/$\overline{W}$, AS0–AS3, AK0–AK3 (Status)		45	60		42	55	
TC(BR)	$\overline{BUS\ REQ}$		35	45		32	40	
TC(BB)	$\overline{BUS\ BUSY}$		42	55		28	40	
TC(BL)	$\overline{BUS\ LOCK}$		38	50		25	35	
TC(BL)z	$\overline{BUS\ LOCK}$, TRI-STATE		27	40		15	35	
TC(IBA)v	IB0–IB15 Address		51	65		45	55	
TC(IBA)z	IB0–IB15 Address, TRI-STATE		48	75		30	60	
TC(SA)l	STRBA Low		15	25		10	20	
TC(SA)h	STRBA High		25	35		20	35	
TC(IBD)v	IB0–IB15 Data		50	60		45	55	
TC(IBD)z	IB0–IB15 Data, TRI-STATE		25	45		25	40	
TC(SDr)l	$\overline{STRBD}$ Low (Read)		65	85		35	65	
TC(SDr)h	$\overline{STRBD}$ High (Read)		30	45		25	35	
TC(SDw)l	$\overline{STRBD}$ Low (Write)		35	50		25	40	
TC(SDw)h	$\overline{STRBD}$ High (Write)		31	40		25	35	
TC(SNW)	SNEW		60	75		50	65	
TC(TGO)	$\overline{TRIGO\ RST}$		55	70		45	60	
TC(DME)	DMA EN		47	60		37	50	
TC(NPU)	NML PWRUP		60	70		47	60	
TC(ER)	Clock to MAJ ER, UNRCV ER Valid		83	100		65	85	

Timing Characteristics (Continued)

TABLE XII. F9450 Timing Characteristics (Continued)

Symbol	Description	15DC, 15GC 15DM, 15GM			F15DC, F15GC F15DM, F15GM F18DC, F18GC F18DM, F18GM F20DC, F20GC F20DM, F20GM			Notes
		Units (ns)			Units (ns)			
		Min	Typ	Max	Min	Typ	Max	
PROPAGATION DELAY FROM CLOCK (Continued)								
TC(M)z	Clock to Status, TRI-STATE		25	40		25	40	
TC(BB)z	Clock to $\overline{\text{BUS BUSY}}$ TRI-STATE		23	35		16	30	
TC(SD)z	Clock to $\overline{\text{STRBD}}$, TRI-STATE		25	40		15	30	
TC(SA)z	Clock to STRBA, TRI-STATE		25	40		18	30	
SETUP TIME BEFORE CLOCK (unless otherwise specified)								
TRAv(C)	RDYA		20	30		18	30	
TRDv(C)	RDYD		20	30		17	30	
TIBDv(C)	IB0–IB15 Data In		−5	0		−5	5	
TREQv(C)	$\overline{\text{CON REQ}}$		−20	0		−15	0	
TRSv(C)	$\overline{\text{RESET}}$		0	10		5	20	
TBLv(C)	$\overline{\text{BUS LOCK}}$		13	25		15	25	
TBGv(C)	$\overline{\text{BUS GNT}}$		15	25		14	25	
TIRv(C)	PWRDN INT, USRx INT Lvl Sense		0	15		0	15	
TFv(C)	Level-Sensitive Fault, $\overline{\text{MEM PRT ER}}$, $\overline{\text{EXT ADR ER}}$ to Clock		15	35		17	35	
TFv(BB)h	Faults to External BUS BUSY		50	70		25	60	
TIRLv(C)	IOL1 INT, IOL2 INT		−25	0		−15	0	
TPARv(C)	Load FT, Generate UNRCV ER			5		3	10	
TPARv(C)	Inhibit Register Load		12	20		3	10	
TEAEv(C)	Terminate Wait States			50			50	
HOLD TIME AFTER CLOCK (unless otherwise specified)								
TC(RA)x	RDYA		−15	0		−10	0	
TC(RD)x	RDYD		−20	0		−15	0	
TC(IBD)x	IB0–IB15 Data In		15	25		15	20	
TC(REQ)x	$\overline{\text{CON REQ}}$		30	40		20	35	
TC(RS)x	$\overline{\text{RESET}}$		10	15		4	20	
TC(BL)x	$\overline{\text{BUS LOCK}}$		−15	0		−10	0	
TC(BG)x	$\overline{\text{BUS GRANT}}$		−15	0		−15	0	
TC(IR)x	PWRDN INT, USRx INT Lvl Sense		0	40		0	30	
TC(IRL)x	IOL1 INT, IOL2 INT		30	40		20	30	
TBBh(F)x	Level-Sensitive Faults (after $\overline{\text{BUS BUSY}}$)		−20	0		−15	0	

Timing Characteristics (Continued)

TABLE XII. F9450 Timing Characteristics (Continued)

Symbol	Description	15DC, 15GC 15DM, 15GM			F15DC, F15GC F15DM, F15GM F18DC, F18GC F18DM, F18GM F20DC, F20GC F20DM, F20GM			Notes
		Units (ns)			Units (ns)			
		Min	Typ	Max	Min	Typ	Max	
OTHER TIMING PARAMETERS								
TSDl(SD)h	STRBD Pulse Width/Write Cycle	55	60		60 50 45	67 57 52		15 MHz (Note 1) 18 MHz (Note 1) 20 MHz (Note 1)
TIBAv(SA)l	Address Valid to STRBA Low	10	30		5	15		(Note 1)
TIBDv(SDw)h	Data Valid to STRBD High (Write)	90	115		90 80 70	115 95 85		15 MHz (Note 1) 18 MHz (Note 1) 20 MHz (Note 1)
TSAl(IBA)x	Address Valid after STRBA Low Hold Time	5	20		5	15		
TMv(SA)l	Status Valid to STRBA Low	20	35		10	20		(Note 1)
TSDwh(IBD)x	$\overline{\text{STRBD}}$ Write High to Data Invalid	40	55		40	50		
TIBDx(SDr)h	Data Don't Care to STRBD Read High	0	15		0	10		
TMEM	Memory or I/O System Time	135	150		135 105 90	160 130 115		15 MHz (Notes 1 and 2) 18 MHz (Notes 1 and 2) 20 MHz (Notes 1 and 2)
TIBAz(SD)l	Guaranteed by Design	0			0			
TF(F), TI(l)	Pulse Width—Edge Sense		20	30		15	30	

Test Conditions:

Note 1: Parameter is clock dependent.
65 ns used for 15 MHz devices.
55 ns used for 18 MHz devices.
50 ns used for 20 MHz devices.

: Memory or I/O system time is the elapsed time from valid address to required valid data without additional wait states. If additional time is required for either memory or I/O, it can be obtained by adding wait states in either the address or data time.

C_L = See test circuits. *(Figure 20)*

Input Conditioning: Rise and Fall Time = 6 ns, Amplitude = 0V to 3V; Measurements taken at the 1.5V level.

Clock period (CPRD) = 1/Fmax

Clock Pulse Width (CPW) = 40% to 60% of CPRD.

V_{CC} = 4.75V to 5.25V, I_{INJ} = as specified in Table XIII, T_C = 0°C to +85°C, for DC, GC; TC = −55°C to +125°C for DM, GM.

Absolute Maximum/Minimum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

The absolute minimum and maximum ratings of the F9450 CPU are as follows:

Storage Temperature	−65°C to +150°C
Operating Case Temperature under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +6.0V
Input Voltage (dc)	−0.5V to +5.5V
Input Current (dc)	−20 mA to +5 mA
Output Voltage (Output High)	−0.5V to +5.5V
Output Current (Output Low) (dc)	+20 mA
Injector Current (I_{INJ})	1.8A
Thermal Resistance Junction to Case (θ_{JC})	2.5°C/W
ESD Rating	2000V

These are stress ratings only, and functional operation at these ratings, or under any conditions beyond those indicated in this datasheet, is not implied. Exposure to the absolute rating conditions for extended periods of time may affect device reliability and exposure to stresses greater than those listed may cause permanent damage to the device.

Recommended Operating Ranges

Table XIII lists the recommended operating ranges for the F9450.

TABLE XIII. Recommended Operating Ranges

Part Number	Supply Voltage (V_{CC}) (Volts)			Injector Current (I_{INJ}) (Amps)			Case Temperature (°C)
	Min	Nom	Max	Min	Nom	Max	
F9450-15DC, GC, F15DC, GC	4.75	5.0	5.25	0.98	1.1	1.22	0°C to +85°C
F9450-15DM, GM, F15DM, GM	4.75	5.0	5.25	0.98	1.1	1.22	−55°C to +125°C
F9450-F18DC, GC	4.75	5.0	5.25	0.98	1.13	1.28	0°C to +85°C
F9450-F18DM, GM	4.75	5.0	5.25	0.98	1.13	1.28	−55°C to +125°C
F9450-F20DC, GC	4.75	5.0	5.25	1.04	1.16	1.28	0°C to +85°C
F9450-F20DM, GM	4.75	5.0	5.25	1.04	1.16	1.28	−55°C to +125°C

DC Characteristics

The F9450 CPU DC characteristics are described in Table XIV.

TABLE XIV. F9450 DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	Guaranteed Input High	2.0			V
V_{IH}	Input High Level (CPU CLK Input Only)	Guaranteed Input High	2.2			V
V_{IL}	Input Low Level	Guaranteed Input Low			0.8	V
V_{T+}	Positive-Going Threshold Voltage USR_0 INT–USR_5 INT, $SYSFLT_0$, $SYSFLT_1$, PWRDN INT	V_{CC} = 5.0V I_{INJ} = Typ.	1.5	1.8	2.0	V
V_{T-}	Negative-Going Threshold Voltage USR_0 INT–USR_5 INT, $SYSFLT_0$, $SYSFLT_1$, PWRDN INT	V_{CC} = 5.0V I_{INJ} = Typ.	0.6	0.95	1.1	V
V_{CD}	Input Clamp Voltage	I_{IN} = −18 mA V_{CC} = Min. I_{INJ} = Typ.		−0.9	−1.5	V
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA V_{CC} = Min. I_{INJ} = Typ.	2.4	3.2		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA V_{CC} = Min. I_{INJ} = Typ.		0.25	0.5	V
I_{IH}	Input High Current Except IB_0–IB_{15}, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$	V_{IN} = 2.7V, V_{CC} = Max. I_{INJ} = Typ.			40	μA
I_{IN}	Input High Current IB_0–IB_{15}, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$	V_{IN} = 2.7V, V_{CC} = Max. I_{INJ} = Typ.			100	μA

DC Characteristics (Continued)

The F9450 CPU DC characteristics are described in Table XIV.

TABLE XIV. F9450 DC Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current All Inputs	$V_{IN} = V_{CC}$, V_{CC} = Max. I_{INJ} = Typ.			1.0	mA
I_{IL}	Input Low Current	V_{IN} = 0.4V V_{CC} = Max. I_{INJ} = Typ.		−200	−400	μA
I_{OZH}	Output TRI-STATE Current IB_0–IB_{15}, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$	V_{OUT} = 2.4V V_{CC} = Max. I_{INJ} = Typ.			140	μA
I_{OZH}	Output TRI-STATE Current AK_{-0}–AK_3, AS_0–AS_3, R/$\overline{W}$, M/$\overline{IO}$, D/$\overline{I}$, STRBA, $\overline{STRBD}$	V_{OUT} = 2.4V V_{CC} = Max. I_{INJ} = Typ.			100	μA
I_{OZL}	Output TRI-STATE Current IB_0–IB_{15}, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$	V_{OUT} = 0.5V V_{CC} = Max. I_{INJ} = Typ.			−500	μA
I_{OZL}	Output TRI-STATE Current AK_0–AK_3, AS_0–AS_3, R/W, M/IO, D/I, STRBA, $\overline{STRBD}$	V_{OUT} = 0.5V V_{CC} = Max. I_{INJ} = Typ.			−100	μA
I_{OSH}	Output Short Circuit***	V_{OUT} = 0V V_{CC} = Max. I_{INJ} = Typ.	−15		−125	mA

***Not more than one output shorted at one time.

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = Max. I_{INJ} = Typ. T_C = −55°C.		340	390	mA
		V_{CC} = Max. I_{INJ} = Typ. T_C = 0°C*.		325	350	mA
		V_{CC} = Max. I_{INJ} = Typ. T_A = Room Ambient		270		mA
		V_{CC} = Max. I_{INJ} = Typ. T_C = 85°C*		260	300	mA
		V_{CC} = Max. I_{INJ} = Typ. T_C = 125°C**		210	260	mA
V_{INJ}	Injector Voltage	V_{CC} = Max. I_{INJ} = Min.	1.2		1.43	V
		V_{CC} = Max. I_{INJ} = Max.	1.34		1.55	V

*Commercial Product Only.

**For derating purposes, use this number for 115°C.

DC Characteristics (Continued)

F9450-F15, F9450-F18, F9450-F20

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = Max. I_{INJ} = Typ. T_C = −55°C		340	450	mA
		V_{CC} = Max. I_{INJ} = Typ. T_C = 0°C*		325	350	mA
		V_{CC} = Max. I_{INJ} = Typ. T_A = Room Ambient		300		mA
		V_{CC} = Max. I_{INJ} = Typ. T_A = 85°C*		260	300	mA
		V_{CC} = Max. I_{INJ} = Typ. T_C = 125°C**		210	290	mA
V_{INJ}	Injector Voltage	V_{CC} = Max. I_{INJ} = Min.	1.2		1.43	V
		V_{CC} = Max. I_{INJ} = Max.	1.34		1.55	V

*Commercial Product Only.

**For derating purposes, use this number for 115°C.

System Implementation

For examples of sources of injection current, contact a National Sales Office to obtain a copy of the "Injection Current Sources" Application Note. Please refer to the F9450 User Guide for additional application information.

F9450 Address Space Implementation

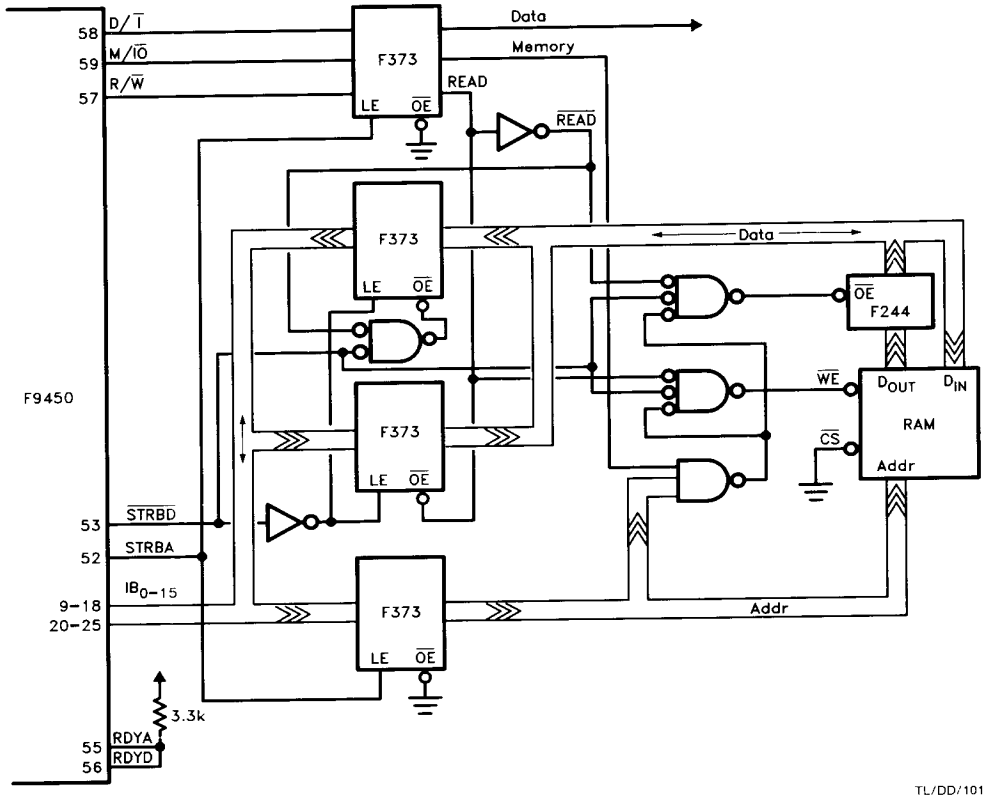
The F9450 implements the direct-address memory standard, as defined by MIL-STD-1750A, using 16 address lines and a data/instruction (D/I) line that differentiates between data or instruction address (see *Figure 21*). The sixteen address lines provide 64k words of address space. The additional D/I line provides 128k words of address space: 64k words of data and 64k words of instruction.

Memory Expansion

The F9451 Memory Management Unit (MMU) and a Block Protect Unit (BPU) facilitate system memory expansion and provide comprehensive memory protection. The MMU does logical-to-physical address translation for a system consisting of up to 10M words of memory (1M words for MIL-STD-1750A applications). The MMU also supplies the logic that allows execute protection in the instruction space and write protection in the data space. (Refer to the F9451 datasheet for additional information.)

The BPU provides supplementary protection capability by allowing separate write protection for both CPU and DMA access. This protection is based on a 20-bit physical address for the data space.

Memory Expansion (Continued)



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Note: This diagram depicts a simple 64 kW F9450 System. It is intended for reference only and should not be considered to be an exact system implementation.

FIGURE 21. Typical Memory Subsystem Minimum Configuration

Memory Expansion without an MMU

Note: Most interpretations of MIL-STD-1750A do not permit extending address space without a memory management unit. Therefore, these memory expansion schemes require the CPU to be initialized as though attached to an MMU. National does not certify the following non-standard uses of the circuit.

In addition to the standard 17-line direct-address scheme (16 direct-address lines plus data/instruction line), MIL-STD-1750A provides four Address State (AS) lines that extend addressing space. The F9450 enables these four AS lines to be implemented directly as address lines, therefore providing a total of 21 address lines and effectively increasing the address space to 2M words: 1M word of data and 1M word of instruction.

These additional bits of address must be viewed as memory "segment" bits, and must be specifically set in the Status Word Register to enter a different segment (see *Figure 22*). The Instruction Counter (IC) is 16 bits wide and no addressing schemes within MIL-STD-1750A will change the AS bits. Therefore, the programmer must directly manipulate the AS bits to enter a different Address State.

Memory Expansion without an MMU (Continued)

On initialization after reset, the processor performs a complete test of all major functions and initializes its internal registers in accordance with the available information. (Refer to the "Self-Test and Initialization" section for details.) Since all extensions to the normal addressing range rely on the use of the Address State (AS) bits in the Status Word Register, the F9450 must be initialized as though attached to an MMU.

Attempts to modify the AS bits without initializing the processor as though attached to an MMU result in an Address State Fault (setting bit 11 in the Fault Register). To prevent the fault, the automatic IOR at 8410 (Hex), which initializes the System Configuration Register (SCR), must contain a high (1) in bit 0. Once the SCR is initialized, the AS bits can be toggled without generating an Address State Fault. There are three methods used to change the Address state bits.

BEX Instruction: The Branch tc Executive (BEX) instruction provides the best method of changing the AS bits and all pointers related to normal program execution. A BEX instruction saves the current MK, SW, and IC in locations LP, LP + 1, and LP + 2. The new MK, SW and IC are retrieved from SVP, SVP + 1, and SVP + 2 + N. The Service Pointer (SVP) is loaded from location 2B (Hex); the Linkage Pointer (LP) is loaded from location 2A (Hex). Note that interrupts are automatically disabled when this instruction is executed. During real-time applications, the programmer must reenable them. Return is best accomplished via the Load Status (LST) instruction.

XI0 RA, WSW Instruction: The Execute Input/Output, Write Status Word (XI0 RA, WSW) instruction transfers the contents of register RA into the Status Word Register (SWR). It contains no provisions for saving/replacing current pointers; the programmer must ensure these steps prior to instruction execution. Basically, this instruction was designed to set/clear the flags and the AK(PS) bits in the Status Register. It allows no control of the IC, which remains the same +1. Therefore, the program will continue execution in a new memory segment, but at the same location (IC) as in the old segment. This expansion scheme requires the programmer to place entry points of routines carefully, and does not allow easy program modification. Return is best accomplished via the Load Status (LST) instruction, which returns control to a known location.

LST Instruction: The Load Status (LST) method, designed to be used as an unconditional jump instruction, loads a new MK, SW, and IC from a known memory location (not the vector table), and begins execution based on these new pointers.

In the previous expansion schemes, the LST instruction is recommended for returning from the expanded memory segment. This instruction is best used to accomplish a return, as a specific location in memory could be reserved to hold return pointers, just as destination pointers are held. The programmer should note that the instruction does not save old pointers prior to the jump.

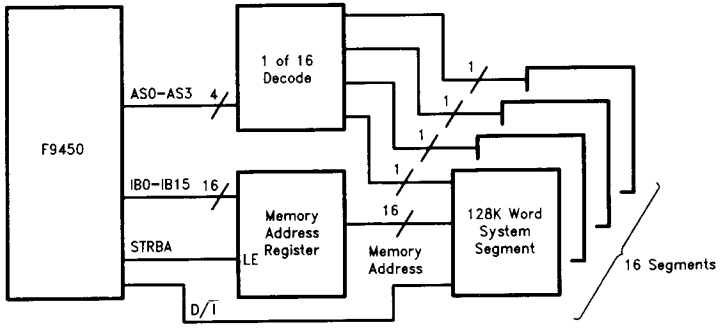

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FIGURE 22. Typical Segmented 2M Word Memory System

Built-In Function Implementation with an External Coprocessor

The Built-In Function (BIF) is an escape code in the F9450 instruction set that allows user-defined instructions. The F9450 implements Built-In-Function as a three-word instruction. The MSH of word 0 contains 4F, in accordance with MIL-STD-1750A (Notice 1); the format of the remaining 40 bits is as follows:

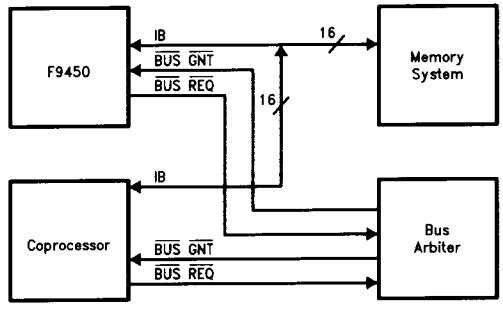
Bit No.	Description
8	*Indicates Immediate (0)/Direct (1) (Referring to Coprocessor Command)
9	*Indicates Two-Word (0)/Three-Word (1) Command (must be (1); if (0) Bit 9 of FT is set)
10, 11	*Indicates Coprocessor Number (00 = 0, 01 = 1, 10 = 2, 11 = 3) (The F9450 Supports Four Coprocessors)
12 to 15	*Indicates Index Register Number (0 through F_{16}, 0 = No Index Register)
16 to 31	Coprocessor Command
32 to 47	Coprocessor Data Address

*Bits in Opcode Extension

Use of an external user-defined coprocessor for BIF implementation is shown in *Figure 23*.

The coprocessor receives the command word (defining the instruction) and control word via XIO operations (see Table III). The operands to the coprocessor are passed from the F9450 by parameter address passing, and the coprocessor becomes a bus contender arbitrated by the bus arbiter. If the system includes an MMU, an additional latch is added to provide an Address State (AS) and Access Key (AK) for the coprocessor.

(a) No MMU



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(b) With MMU

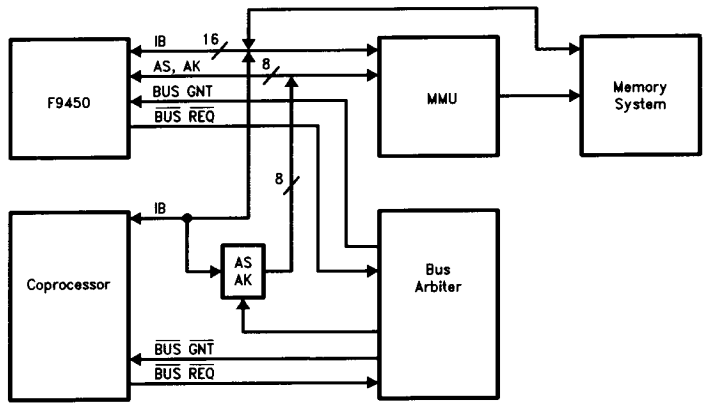

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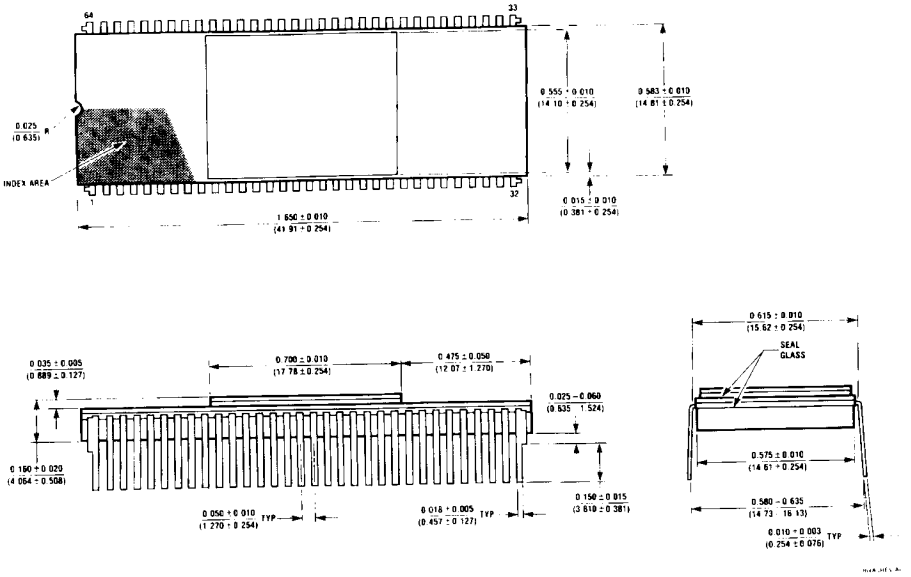
FIGURE 23. F9450/ Coprocessor Configuration

Ordering Information

Order Code	Case Temperature (T_C) Operating Range (°C)	Package Type
F9450-15DC-MSP	0°C to +85°C	Hermetic DIP
F9450-15DMQB	−55°C to +125°C	Hermetic DIP
F9450-15GC-MSP	0°C to +85°C	Hermetic Gull Wing Surface Mount
F9450-15GMQB	−55°C to +125°C	Hermetic Gull Wing Surface Mount
F9450-F15DC-MSP	0°C to +85°C	Hermetic DIP
F9450-F15DMQB	−55°C to +125°C	Hermetic DIP
F9450-F15GC-MSP	0°C to +85°C	Hermetic Gull Wing Surface Mount
F9450-F15GMQB	−55°C to +125°C	Hermetic Gull Wing Surface Mount
F9450-F18DC-MSP	0°C to +85°C	Hermetic DIP
F9450-F18DMQB	−55°C to +125°C	Hermetic DIP
F9450-F18GC-MSP	0°C to +85°C	Hermetic Gull Wing Surface Mount
F9450-F18GMQB	−55°C to +125°C	Hermetic Gull Wing Surface Mount
F9450-F20DC-MSP	0°C to +85°C	Hermetic DIP
F9450-F20DMQB	−55°C to +125°C	Hermetic DIP
F9450-F20GC-MSP	0°C to +85°C	Hermetic Gull Wing Surface Mount
F9450-F20GMQB	−55°C to +125°C	Hermetic Gull Wing Surface Mount

Physical Dimensions inches (millimeters)



64-Pin Ceramic Dual-In-Line Package (DC or DM)
Order Number F9450
NS Package Number J64A

Note 1: Index Area; A pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown.

Note 2: The letter "BeO" shall be located adjacent to pin 64.

Note 3: All dimensions are in inches **(bold)** and millimeters (parentheses); tolerances ± 0.010 (0.25) unless otherwise stated.

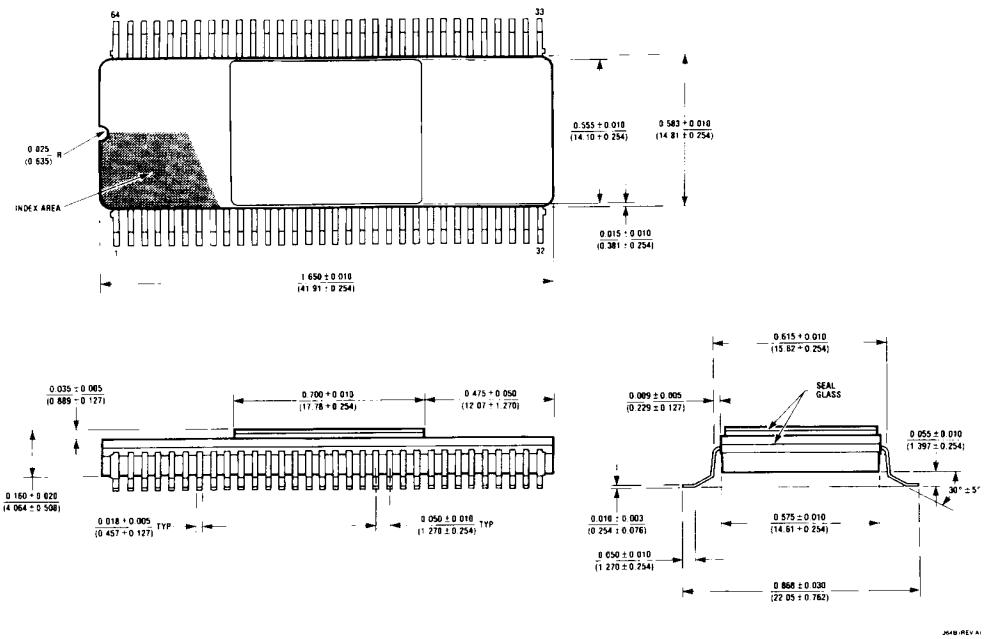
Note 4: Lead finish: hot solder dip per MIL-M-38510

Note 5: Cap is ceramic.

Note 6: Base is BeO.

Note 7: Package weight is 8.5 grams.

Physical Dimensions inches (millimeters) (Continued)



64-Pin Ceramic Gull-Wing Dual-In-Line Package (GC or GM)
Order Number F9450
NS Package Number J64B

Note 1: Index Area; A pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown.

Note 2: The letter "BeO" shall be located adjacent to pin 64.

Note 3: All dimensions are in inches (**bold**) and millimeters (parentheses); tolerances ± 0.010 (0.25) unless otherwise stated.

Note 4: Lead finish: hot solder dip per MIL-M-38510.

Note 5: Cap is ceramic.

Note 6: Base is BeO.

Note 7: Package weight is 8.5 grams.

Note 8: Plane of lead "feet" parallel to bottom surface of BeO base ± 5°C.

Lit. # 103798

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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