FAN5201

Chemistry Independent Intelligent Battery Charger

Features

- Chemistry independent charging
- SMBus™ 2-wire serial interface controlled
- Independent Voltage, Current and Power DACs
- 6A maximum charging current
- 4–19V battery voltage range
- 24V maximum input voltage
- 5V “keep alive” regulator controller onboard
- 100% maximum duty-cycle
- Synchronous rectification
- System soft start protects during hot plug-ins
- Latched current limit protection
- Output over-voltage protection (crowbar)
- Input under-voltage lockout
- Battery backfeed prevented
- Optimized response for each control loop (current, voltage and power)
- Power down driven by SMBus or by adapter not available or by softstart pin
- Controlled drive of discrete FETs minimizes power dissipation
- Logic signal ACAV indicates presence of AC adapter (adjustable threshold)
- Output current “motorboating” prevented
- True power multiplier

Applications

- Notebooks’ fast chargers
- PDAs
- Hand-held portable instruments

Description

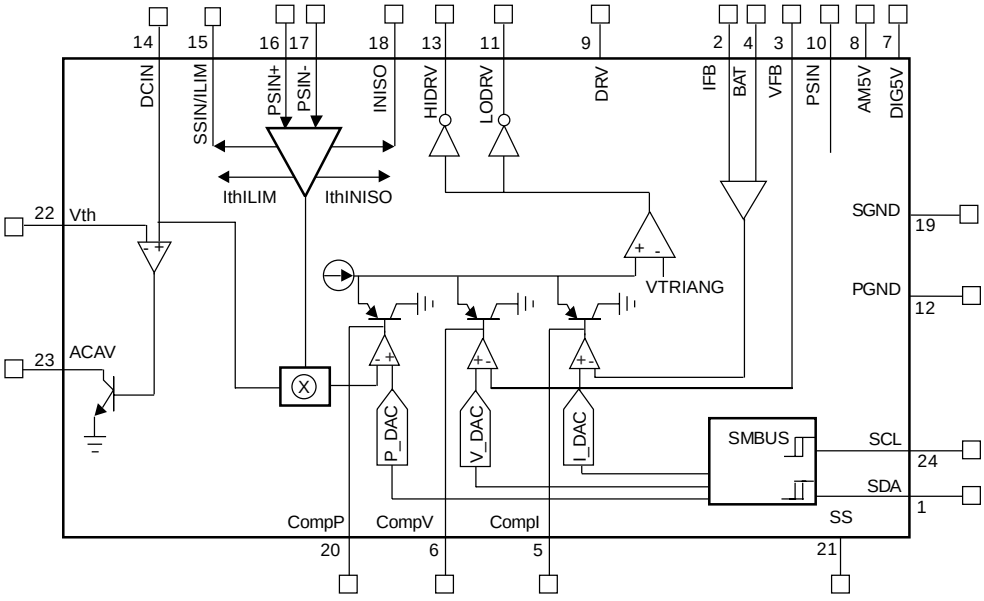
The FAN5201 is a smart battery charger IC controller for Li+ and Ni based battery chemistries. The charger (slave) together with the host controller and smart battery constitutes a smart battery system that communicates via the SMBus protocol, a two wire serial communication system.

An innovative power control loop allows operation from line power and battery charging (with residual power) without exceeding the maximum input power programmed according to the AC adapter power rating.

The FAN5201 is available in one SSOP24 package.

Preliminary Specification

Block Diagram



Preliminary Specification

SMBus Functional Description

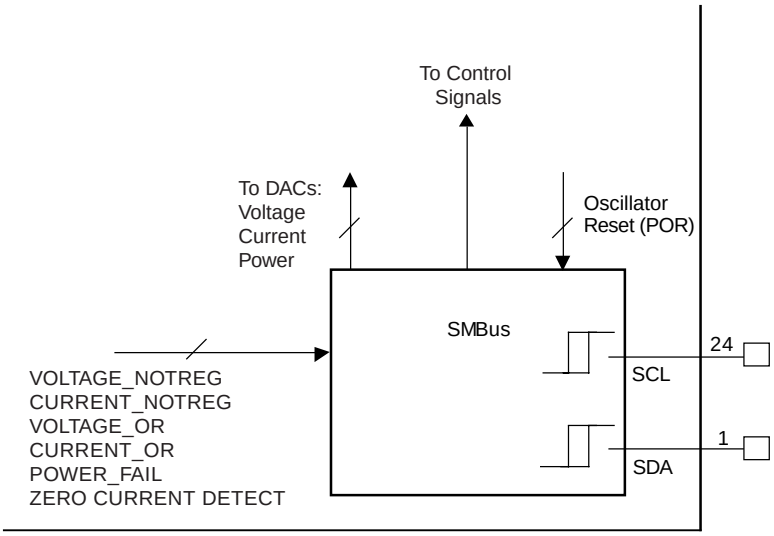
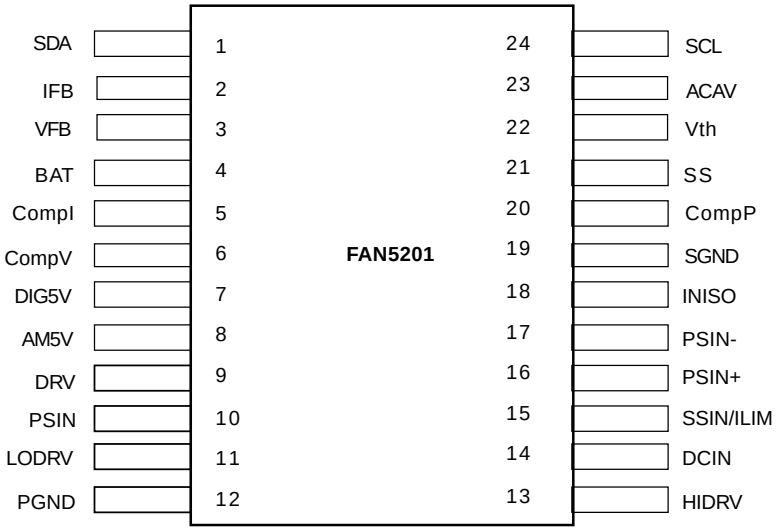


Figure 1. Internal SMBus Configuration

Pin Assignments



Pin Descriptions

Pin Number	Pin Name	Pin Function Description
1	SDA	**Serial Data**. SMBus data I/O.
2	IFB	**Current Feedback.** Output current sense +. Connect this pin to the positive side of a battery current sense resistor.
3	VFB	**Voltage Feedback.** Voltage remote sense feedback. Connect this pin to the battery terminals.
4	BAT	**Battery.** Output current sense -. Connect this pin to the negative side of a battery current sense resistor.
5	CompI	**Current Compensation.** Frequency compensation for current loop.
6	CompV	**Voltage Compensation.** Frequency compensation for voltage loop.
7	DIG5V	**5V Digital Input.** 5V internal power.
8	AM5V	**5V Analog Input.** Connect to 5V power. See Figure 4.
9	DRV	**Drive.** Base (gate) drive for external PNP (P-channel MOSFET).
10	PSIN	**Power Supply.** Power source node, powered either by the AC adapter or by the battery.
11	LODRV	**Low Side FET Driver.** Drive for low side switching MOSFET Q4.
12	PGND	**Power Ground.**
13	HIDRV	**High Side FET Driver.** Drive for high side switching MOSFET Q3.
14	DCIN	**DC Power Input.** Connect to the AC adapter input.
15	SSIN/ILIM	**Soft Start and Current Limit.** Connect to an external MOSFET for limiting inrush and fault current.
16	PSIN+	**Input Power Sense +.** Connect this pin to the positive side of an adapter current sense resistor.
17	PSIN-	**Input Power Sense -.** Connect this pin to the negative side of an adapter current sense resistor.
18	INISO	**Input Isolation Drive.** Q2 gate drive. Attach to a P-channel MOSFET to prevent battery backfeed.
19	SGND	**Signal Ground.** Attach all small signal grounds to this pin, and attach the pin to the ground plane with a single connection.
20	CompP	**Power Compensation.** Frequency compensation for power loop.
21	SS	**Soft Start.** Connect to a capacitor to softstart.
22	Vth	**Voltage Threshold.** Sets the level at which ACAV trips.
23	ACAV	**AC Available.** Open collector output signaling that the AC adapter is present.
24	SCL	**Serial Clock.** SMBus clock input.

Absolute Maximum Ratings[1]

Parameter	Conditions	Min.	Typ.	Max.	Unit
DCIN				30	V
PSIN+, PSIN-				30	V
Ambient Temperature, T_A		0		70	°C
Maximum Power Dissipation	SSOP24, T_J = 125°C		TBD		W

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions **DCIN = 19V, T_A = 0-70°C, unless otherwise specified.**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply and Reference					
DCIN Input Supply Voltage	Internal 5V	8		24	V
	External 5V	6		24	V
DCIN Quiescent Current	Operation			3	mA
	Power Down, Note 1			200	µA
PSIN Current	Operation			300	
	Power Down, Note 1		140	200	µA
5V Accuracy	I < 10mA	-4		4	%
DRV Output Sink Current		1			mA
Switching Regulator					
$V_{bat,min}$	I_{OUT} = 32mA	4			V
Maximum Duty Cycle		100			%
Oscillator Frequency		225	250	275	kHz
HIDRV ON Resistance	High		4	7	Ω
	Low		4	7	Ω
HIDRV High Output, $V_{DCIN} - V_{HI}$	I = 10µA			100	mV
HIDRV Low Output, $V_{DCIN} - V_{LO}$	I = 10µA	5			V
LODRV ON Resistance	High		4	7	Ω
	Low		4	7	Ω
LODRV High Output	I = 10µA, AM5V = DIG5V = %5v	4.5			V
LODRV Low Output				100	mV
Analog Functions					
Input Current Limit Threshold		108		132	mV
Input UVLO		5.4		6.6	V
Input UVLO Hysteresis			400		mV
Vtriang Amplitude, pk-pk			950		mV
Vtriang Mean			2.5		V
Vtriang gain from DCIN			50		mV/V
Psense Amplifier CMRR		60			dB
Psense Amplifier CMRR @ 250kHz		32			dB
VFB Leakage	Operation			30	µA
	Power Down, Note 1			1	

Preliminary Specification

Operating Conditions (Continued) DCIN = 19V, T_A = 0-70°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
BAT, IFB Leakage	Operation			TBD	µA
	Power Down, Note 1			10	µA
Output Overvoltage Threshold		107	110	113	%Vout
Vthreshold ACAV	Rt1 = 9KΩ, Rt2 = 1KΩ	5.4		6.6	V
Vhysteresis ACAV	Rt1 = 9KΩ, Rt2 = 1KΩ		400		mV
Battery POWER_FAIL Threshold		5.4		6.6	V
CURRENT_NOTREG		90		110	%Ireg
VOLTAGE_NOTREG		90		110	%Vreg
Input Isolation Current Threshold	Ith = Vth/RS1	3.6			mV
Backfeed Current Threshold	Ith = Vth/RS2	3.6			mV
Zero Current Detect Threshold			9.7		mV
VOLTAGE_OR Threshold			110		%Vout
CURRENT_OR Threshold		110		112	mV
AC_PRESENT Threshold		5.4		6.6	V
AC_PRESENT Hysteresis			400		mV
Soft Start Current			2		µA
Soft Start Disable	Output disabled			800	mV
Over-temperature Shutdown			150		°C
Digital Functions					
Current DAC Resolution				8	Bits
Current DAC Accuracy		-5		+5	%FS
Current DAC Differential Nonlinearity		-1/2		+1/2	LSB
Current DAC Integral Nonlinearity		-2		+2	LSB
Current DAC Conversion Time				2	msec
Current DAC Voltage Offset		0			mV
Voltage DAC Resolution				8	Bits
Voltage DAC Accuracy		-5		+5	%Vout
Voltage DAC Differential Nonlinearity		-1/2		+1/2	LSB
Voltage DAC Integral Nonlinearity		-2		+2	LSB
Voltage DAC Conversion Time				2	msec
Power DAC Resolution				4	Bits
Power DAC Accuracy		-5		+5	%FS
Power DAC Differential Nonlinearity		-1/2		+1/2	LSB
Power DAC Integral Nonlinearity		-2		+2	LSB
Power DAC Conversion Time				2	msec
Switches Q1, Q2					
SSIN/ILIM Source Current, pk		10			mA
SSIN/ILIM Sink Current, pk		35		65	µA
SSIN/ILIM High Output, $V_{DCIN} - V_{HI}$				100	mV
SSIN/ILIM Low Output, $V_{DCIN} - V_{LO}$	V_{DCIN} = 19V	10		12	V
	V_{DCIN} = 10V	8			V
INISO ON Sink Current				50	µA

Preliminary Specification

Operating Conditions (Continued) DCIN = 19V, T_A = 0-70°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
INISO High Output, $V_{DCIN} - V_{HI}$				100	mV
INISO Low Output, $V_{DCIN} - V_{LO}$	V_{DCIN} = 19V	10		12	V
	V_{DCIN} = 10V	8			V
SMBus					
Data/Clock input low voltage, V_{IL}		-0.3		0.6	V
Data/Clock input high voltage, V_{IH}		1.4		5.5	V
Data/Clock output low voltage, V_{OL}	At I_{PULLUP} MIN			0.4	V
Data/Clock hysteresis, V_{HYS}			200		mV
Input leakage, I_{LEAK}		-1		1	µA
Current through pullup resistor or current source, I_{PULLUP}		100		350	µA
SMB operating frequency, F_{SMB}		10		100	kHz
Bus free time between Stop and Start condition, T_{BUF}		4.7			µsec
Hold time after (repeated) Start condition, $T_{HD:STA}$	After this period, the first clock is generated	4.0			µsec
Repeated Start condition setup time, $T_{SU:STA}$		4.7			µsec
Stop condition setup time, $T_{SU:STO}$		4.0			µsec
Data hold time, $T_{HD:DAT}$		300			nsec
Data setup time, $T_{SU:DAT}$		250			nsec
$T_{TIMEOUT}$	Note 2	25		35	msec
Clock low period, T_{LOW}		4.7			µsec
Clock high period, T_{HIGH}	Note 3	4.0		50	µsec
Cumulative clock low extend time, $T_{LOW:SEXT}$	Note 4			25	msec
Clock/Data fall time, T_F				300	nsec
Clock/Data rise time, T_R				1000	nsec

Notes:

1. 5V DRV Current = 0, SMBus off.
2. A device will timeout when any clock low exceeds this value.
3. T_{HIGH} Max provides a simple guaranteed method for devices to detect bus idle conditions.
4. $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data times and reset itself.

Applications Discussion

Overview

The FAN5201 contains three control loops: a voltage-regulation loop, a current-regulation loop and a power-regulation loop. All three loops operate independently of each other. They are or'red internally to optimize the battery charging while the notebook is drawing power in its normal operation. The voltage-regulation loop monitors the battery to ensure that its voltage is held at the voltage set point (V0). The current-regulation loop monitors current delivered to the battery to ensure that it regulates at the current-limit set point (I0). The power-regulation loop monitors total input power, to both the battery and the notebook, to ensure that total power drawn from the charger never exceeds the maximum power set point (P0). Assuming that there is adequate power available from the charger, the current-regulation loop is in control as long as the battery voltage is below V0. When the battery voltage reaches V0, the current loop no longer regulates, and the voltage-regulation loop takes over. If on the other hand there is not adequate power available from the charger, the power-regulation loop is in control, and limits the charging of the battery in order to guarantee enough power for the notebook. Figure 2 shows the V-I-P characteristic at the battery.

Setting V0, I0 and P0

The FAN5201's voltage-, current-, and power-limits can be set via the Intel System Management Bus (SMBus™) 2-wire serial interface. The FAN5201's logic interprets the serial-data stream from the SMBus interface to set internal digital-to-analog converters (DACs) appropriately. See the FAN5201 Logic section and SMBus Interface Specification for more information.

Analog Section

The FAN5201analog section consists of 1) three transconductance error amplifiers, one for regulating current, one for regulating voltage, and one for regulating system power, 2) a PWM controller, with its associated gate drivers, and 3) miscellaneous control and reference functions, consisting of an AC present signal, 5V reference, inrush current limiter, reverse feed protection, and a soft start circuit.

The FAN5201 uses DACs to set the current, voltage and power levels, which are controlled via the SMBus interface. Since separate amplifiers are used for each of these controls, each of the control loops can be compensated separately for optimum stability and response in each state.

Whether the FAN5201 is controlling the voltage, current or power at any time depends on the battery's state. If there is adequate power available from the charger, and if the battery has been discharged, the FAN5201's output reaches the current-regulation limit before the voltage limit, causing the system to regulate current. As the battery charges, the voltage rises until the voltage limit is reached, and the charger switches to regulating voltage. On the other hand, if there is not enough power available for both the notebook and the battery charging, the FAN5201 regulates charging current at such a level as to respect the maximum power limit. When the voltage limit is reached, the charger will similarly switch to regulating voltage. The transitions from current to voltage regulation, or from power to voltage regulation, are done by the charger, and need not be controlled by the host.

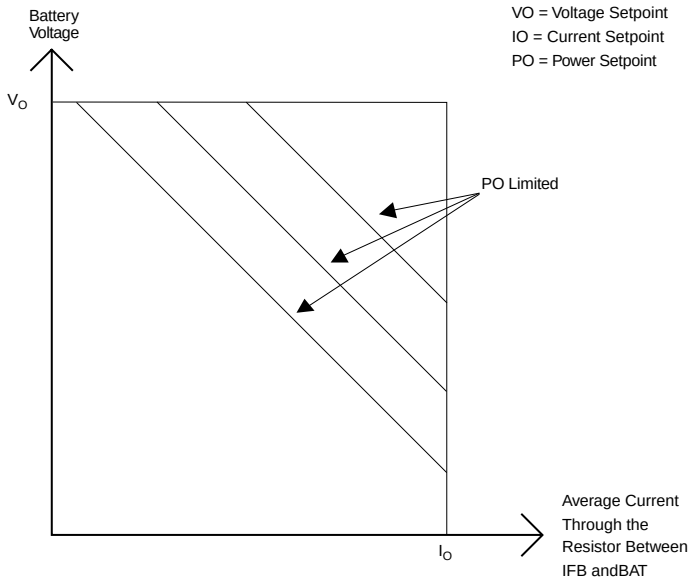


Figure 2. V-I-P Characteristic of FAN5201. If power is available, the battery is charged at a rate I0 until it reaches V0. As power becomes limiting, the charge current is reduced.

Voltage Control Loop

The internal transconductance voltage amplifier controls the FAN5201's output voltage. The battery voltage is fed to the non-inverting input of the amplifier from the VFB pin. The voltage at the amplifier's inverting input is set by an 8-bit DAC, which is controlled by a ChargingVoltage( ) command on the SMBus (See the FAN5201 Logic section and SMBus Interface Specification for more information). The output of the amplifier drives an inverting "or'ring" transistor; the or'ring provides control of the PWM to the lowest of the three amplifiers, while the inversion provides the negative feedback needed for proper control. The ChargingVoltage( ) command of the SMBus provides a 10.000V offset, and 32mV steps, so that the charging voltage can be anywhere from 10.000V to 10.000V + 255 * 32mV = 18.16V. Because a lithium-ion (Li+) battery's typical per-cell voltage is 4.2V maximum, this charger is best suited for 3- and 4-cell batteries. It can also be used for several different cell counts with NiMH batteries.

The voltage amplifier's output is connected to the CompV pin, which compensates the voltage-regulation loop. Typically, a series-resistor/capacitor combination is used to form a pole-zero pair. The pole introduced rolls off the gain starting at low frequencies. The zero provides AC gain at mid-frequencies. The output capacitor of the switcher then rolls off the mid-frequency gain to below 1 to guarantee stability, before encountering the zero introduced by the output capacitor's ESR. Further information on loop stabilization is available in Applications Bulletin AB-18.

Current Control Loop

The internal transconductance current amplifier controls the battery current while the charger is regulating current. Battery current is sensed by monitoring the voltage across a sense resistor (pins IFB and BAT) with an amplifier that removes the common mode battery voltage. The battery current is fed to the non-inverting input of the amplifier. The voltage at the amplifier's inverting input is set by an 8-bit DAC, which is controlled by a ChargingCurrent( ) command on the SMBus (See the FAN5201 Logic section and SMBus Interface Specification for more information). The output of the amplifier drives an inverting "or'ring" transistor; the or'ring provides control of the PWM to the lowest of the three amplifiers, while the inversion provides the negative feedback needed for proper control. The ChargingCurrent( ) command of the SMBus provides 32mA steps with an 18mΩ sense resistor, so that the charging current can be anywhere from 0.000A to 255 * 32mA = 8.16A.

The current amplifier's output is connected to the CompI pin, which compensates the current-regulation loop. Typically, a series-resistor/capacitor combination is used to form a pole-zero pair. The pole introduced rolls off the gain starting at low frequencies. The zero provides AC gain at mid-frequencies. The output capacitor of the switcher then rolls off the mid-frequency gain to below 1 to guarantee stability, before encountering the zero introduced by the output capacitor's ESR. Further information on loop stabilization is available in Applications Bulletin AB-18.

Power Control Loop

The internal transconductance power amplifier controls the system's total power consumption (notebook plus battery charging). Input voltage is monitored on pin DCIN, and input current is sensed by monitoring the voltage across a sense resistor (pins PSIN+ and PSIN-) with an amplifier that removes the common mode input voltage. These two signals are then multiplied together with an analog multiplier, and the result is fed to the non-inverting input of the amplifier. The voltage at the amplifier's inverting input is set by a 4-bit DAC, which is controlled by a ChargingPower( ) command on the SMBus (See the FAN5201 Logic section and SMBus Interface Specification for more information). The output of the amplifier drives an inverting "or'ring" transistor; the or'ring provides control of the PWM to the lowest of the three amplifiers, while the inversion provides the negative feedback needed for proper control. The ChargingPower( ) command of the SMBus provides a 25W offset, and 5W steps, so that the total power drawn can be anywhere from 25W to 25W + 15 * 5W = 100W.

The power amplifier's output is connected to the CompP pin, which compensates the power-regulation loop. Typically, a series-resistor/capacitor combination is used to form a pole-zero pair. The pole introduced rolls off the gain starting at low frequencies. The zero provides AC gain at mid-frequencies. The output capacitor of the switcher then rolls off the mid-frequency gain to below 1 to guarantee stability, before encountering the zero introduced by the output capacitor's ESR. Further information on loop stabilization is available in Applications Bulletin AB-18.

A sudden surge in power required by the notebook will result in a momentary overload on the AC adapter. This has no ill effects, because the power loop recovery time is much shorter than the adapter's thermal time constant, and the minimum adapter output voltage equals the battery voltage, which is sufficient to run the notebook.

PWM Controller

The battery voltage or current or input power is controlled by the pulse-width-modulated (PWM) DC-DC converter controller. This controller drives two external MOSFETs, an N- and a P-channel, which switch the voltage from the input source. This switched voltage feeds an inductor, which filters the switched rectangular wave. The controller sets the pulse width of the switched voltage so that it supplies the desired voltage or current to the battery. The heart of the PWM controller is its multi-input comparator. This comparator compares the lowest of three input signals with a ramp, to determine the pulse width of the switched signal, setting the battery voltage or current. The three signals being or'red together are the current-sense amplifier's output, the voltage-error amplifier's output, and the power-error amplifier's output.

When the current-sense amplifier is in control of the PWM, the comparator adjusts the duty cycle of the switches, regulating the average battery current and keeping it proportional to the error voltage. The current is averaged, rather than peak, since the current sense resistor is between the output capacitor and the battery. Since the average battery current is nearly the same as the peak current, the controller acts as a transconductance amplifier, reducing the effect of the inductor on the output filter LC formed by the output inductor and the output capacitance. This makes stabilizing the circuit easy, since the output filter changes from a complex second-order RLC to a first-order RC. To preserve the inner current-control loop's stability, slope compensation is also fed into the comparator. This damps out perturbations in the pulse width at duty ratios greater than 50%. At heavy loads, the PWM controller switches at a fixed frequency and modulates the duty cycle to control the battery current. At light loads, the DC current through the inductor is not sufficient to prevent the current from going negative through the synchronous rectifier (Figure 2, Q4). The controller monitors the current through the sense resistor; when it drops to below 200mA, the synchronous rectifier turns off to prevent negative current flow.

When the voltage error amplifier is in control of the PWM, the comparator adjusts the duty cycle of the switches, regulating the battery voltage and keeping it proportional to the error voltage. In this mode, the control loop is a standard voltage-mode control, and the only requirement to guarantee stability is that the loop gain be rolled off below 0dB before the LC resonant frequency.

When the power error amplifier is in control of the PWM, the comparator adjusts the duty cycle of the switches, regulating the total power drawn from the charger. The loop determines whether the total power available from the wall adapter is sufficient to provide both the load and battery charging needs. If not, the charging power to the battery is reduced by the amount needed to keep the total demand within the AC-DC output power limit of the adapter.

The PWM controller also implements voltage feedforward. This means that the gain of the control loops are adjusted inversely proportionally to the input voltage: as the input voltage increases, loop gain is decreased. This improves the audio susceptibility of the converter, and in particular, means that the bandwidth of each of the loops is relatively independent of the AC adapter voltage. Feedforward is accomplished by modulating the amplitude of the ramp signal.

MOSFET Drivers

The FAN5201 drives external MOSFETs to regulate battery voltage or current, a high-side P-channel and a low-side N-channel for synchronous rectification. Use of a P-channel MOSFET for the high-side switch permits operation without charge-pumping and its attendant external components. The synchronous rectifier behaves like a diode, but with a smaller voltage drop to improve efficiency. A small dead time is added between the time that the high-side MOSFET turns off and the synchronous rectifier turns on, and vice versa. This prevents shoothrough currents (currents that flow through both MOSFETs during the brief time that one is turning on and the other is turning off). A schottky rectifier from the source to the drain of Q4 prevents the synchronous rectifier's body diode from conducting. The body diode typically has slower switching-recovery times, so allowing it to conduct would degrade efficiency.

Control and Reference Functions

The FAN5201 has a number of additional analog functions to enhance overall system performance. The ACAV is an open collector signal that can be used to determine the presence of the AC charger; its threshold is set by an external resistor divider attached the Vth pin.

A 5V keep alive linear regulator receives power either from the AC adapter via Q1 or from the battery (PSIN pin). This regulator can provide up to 10mA to power memory during a system shutdown.

Protection Circuitry

The FAN5201 protects against a variety of possible fault or problem conditions.

Input Protection

Inrush current can be a problem during hot plug-in if in front of the switching regulator a large capacitor is used to decouple noise. Conceivably, the inrush could be high enough to trip on overcurrent protection in the AC adapter. The FAN5201 provides the means for limiting inrush current to any desired value: The SSIN/ILIM pin provides a sink current of 65µA maximum to turn on the gate of the P-channel MOSFET Q1, so that selecting a gate-source capacitance on Q1 will slow its turn-on time to any desired speed, thus restricting the amount of inrush current.

The charger has its own local soft start, which controls the maximum duty cycle of the PWM. The softstart time is set by selecting a capacitor attached to the SS pin. The softstart pin can also be used for a hard shutdown, by pulling it to ground.

While the AC adapter is not present, the FAN5201 shuts itself off, using an UVLO set at 6.0V.

If the AC adapter is connected to the FAN5201 circuit but is not plugged in, the adapter could present a load to the battery. The FAN5201 prevents this by turning off Q2 (attached to the INISO pin) if the input current falls below 200mA (with an 18mΩ sense resistor). However, this function is disabled until the softstart pin reaches steady state.

Output Protection

If input current exceeds the design of the FAN5201 (6A with an 18mΩ sense resistor) the IC latches off Q1, disconnecting the circuitry from input power within a few microseconds.

If one AC adapter is connected when the battery is not present, the overcurrent limit does not disable the converter because Q1 acts as an inrush current limit.

If the battery voltage exceeds certain levels, internal protection in the battery may open. To prevent this, the FAN5201 latches off Q1, Q3 and Q4 if the output voltage exceeds approximately 110% of the setpoint.

The power converter is a synchronous buck for efficiency. This topology is actually two-quadrant, and could potentially draw current from the battery, boosting it high enough to override the AC adapter. To prevent this backfeed, the FAN5201 turns off the synchronous rectifier if the current into the battery drops below 200mA (with an 18mΩ sense resistor), utilizing instead the paralleled schottky.

If the internal overvoltage switch in the battery were to open due to a high charge current producing a high voltage (due to battery ESR), the voltage loop would take over. With the voltage loop in control, the battery switch would close, and the current could surge high until the current control loop comes out of saturation. The FAN5201 prevents this type of oscillation by means of a special loop controlling the error amplifier of the current loop.

Battery Conditioning

With switch B1 off (see Figure 5), the notebook load can be applied to the batteries even in the presence of the DC adapter. This permits deep discharge of the batteries as part of the battery conditioning process.

Battery Present

The presence of the battery can be detected by the host microcontroller.

Logic Section

The FAN5201 uses serial data to control its operation. The serial interface is compliant with the SMBus specification (see “System Management Bus Specification”, Rev. 1.08). Charger functionality is compatible with an extended subset of the Intel/Duracell Smart Charger Specification for a level 2 charger. The FAN5201 uses the SMBus Read-Word, Write-Word, and Block-Read protocols to communicate with the host system that monitors the battery. The FAN5201 never initiates communication on the bus; it only receives commands and responds to queries for status information. Figure 9 shows examples of the SMBus Write-Word and Read-Word protocols. Each communication with the FAN5201 begins with a start condition that is defined as a falling edge on SDA with SCL high. The device address follows the start condition. The FAN5201 device address is 0001001b (b indicates a binary number). Note that the address is only seven bits, and the binary representation uses R/W as its least significant bit.

Programming a µP Interface for the FAN5201

The µP programmer must bear in mind that the FAN5201 operates as a slave device to the host µP; all communications to the battery are *via* the host. Thus, in particular, the ChargingCurrent(), ChargingVoltage(), and AlarmWarning() commands (and thermistor signals for Ni based batteries) must all be passed to the µP. There is no way to send them directly to the charger.

Another important aspect for the programmer to be aware of is that at power-up, all of the internal registers of the FAN5201 are zeroed. Thus, in order to have the FAN5201 turn on, it is necessary to write to all of the DACs. It is also recommended to write to the Control Signals Word before writing to the DACs.

With these suggestions in mind, a possible flowchart for the µP interface to the FAN5201 would be as shown in Figure 3. In the first step, the battery charge requests are read; after this the FAN5201 can be programmed. First, the FAN5201 is left in Power Down until the programming has been successful. Next, Charging Power, Current, and Voltage are set; the FAN5201 will not operate until all three have been written. The µP next checks that all of the data has been correctly written; if not, the programming sequence is retried. Finally, the Power Down signal is turned off.

Application Schematics and BOMs

Figure 4 shows the FAN5201 in a single battery pack system. Figure 5 shows the FAN5201 in a two battery pack system. In a two battery system, the host microcontroller must poll to determine the state of each battery; and then a selector must control the switches. Figure 4 shows a typical Smart Battery system: for Ni based chemistries the temperature information is handled directly by the µC. The µC continuously monitors the SMBus; in case of communications breakdown the µC detects this and takes appropriate action. For a NiMH battery, a hardware overtemperature protection can be implemented using a comparator on the thermistor line, and turning the softstart pin off.

Notice that Q1 through Q4 are drawn with the associated intrinsic diode in Figure 4 and Figure 5.

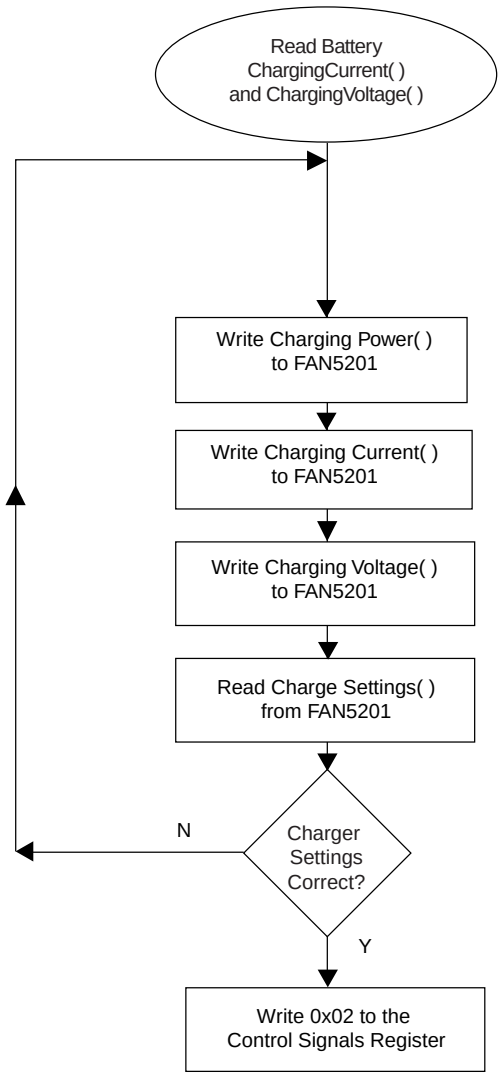


Figure 3. Suggested Flowchart for FAN5201 Startup

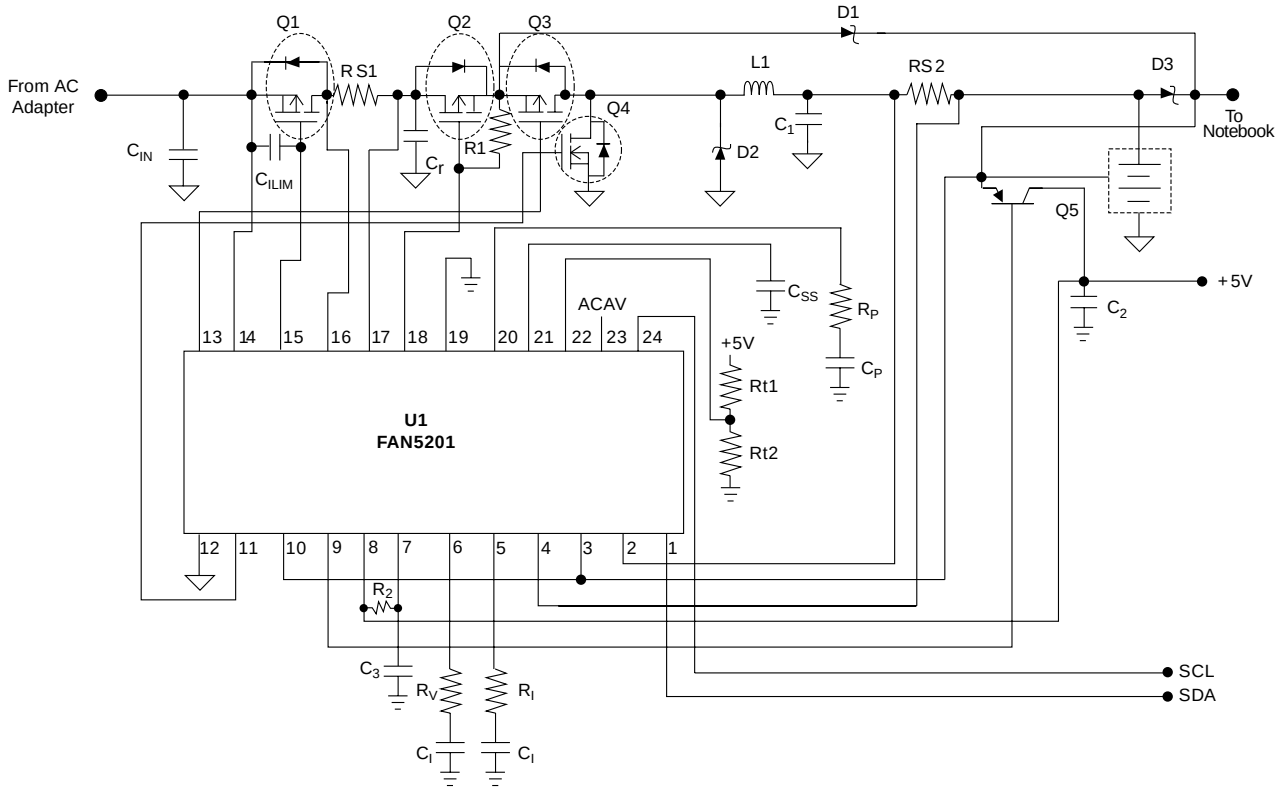


Figure 4. Single Battery Pack System

Table 1. Bill of Materials for Single Battery Pack System (8A maximum current)

Reference	Manufacturer	Manufacturer's P/N	Quantity	Description
C_V, C_I, C_{ILIM}			3	100nF 20% 50V Ceramic Chip Cap
C_1,C_r	AVX	TPSV107*020R0085	2	100µF 20V 85mΩ Tantalum Chip Cap
C_{SS}			1	10nF 20% 50V Ceramic Chip Cap
C2–3			2	10µF, 10V Tantalum Chip Cap
R_V			1	10KΩ 1% 1/10W
Rt1			1	9.09KΩ 1% 1/10W
Rt2, R_I			1	1KΩ 1% 1/10W
RS1-2	Dale	WSL-2512-R018	2	18mΩ 1W SM
R1			1	100KΩ 1/10W
C_P			1	970nF Ceramic Chip cap
R_P, R2			2	10Ω 1/10W
L1	Dale	IHSM-7832-5.6µH	1	5.6µH 6A 25mΩ SM Inductor
Q1-2	Fairchild	NDS8435A	2	30V 23mΩ SO8 P-channel
Q3	Fairchild	FDS9435A	1	30V 50mΩ SO8 P-channel
Q4	Fairchild	FDS6612A	1	30V 10mΩ SO8 N-channel
Q5		FZT704CT	1	100V 2A SOT223 PNP Darlington
D1-3	Motorola	MBRD835L	3	35V 8A Schottky
U1	Fairchild	FAN5201	1	SSOP24 Controller

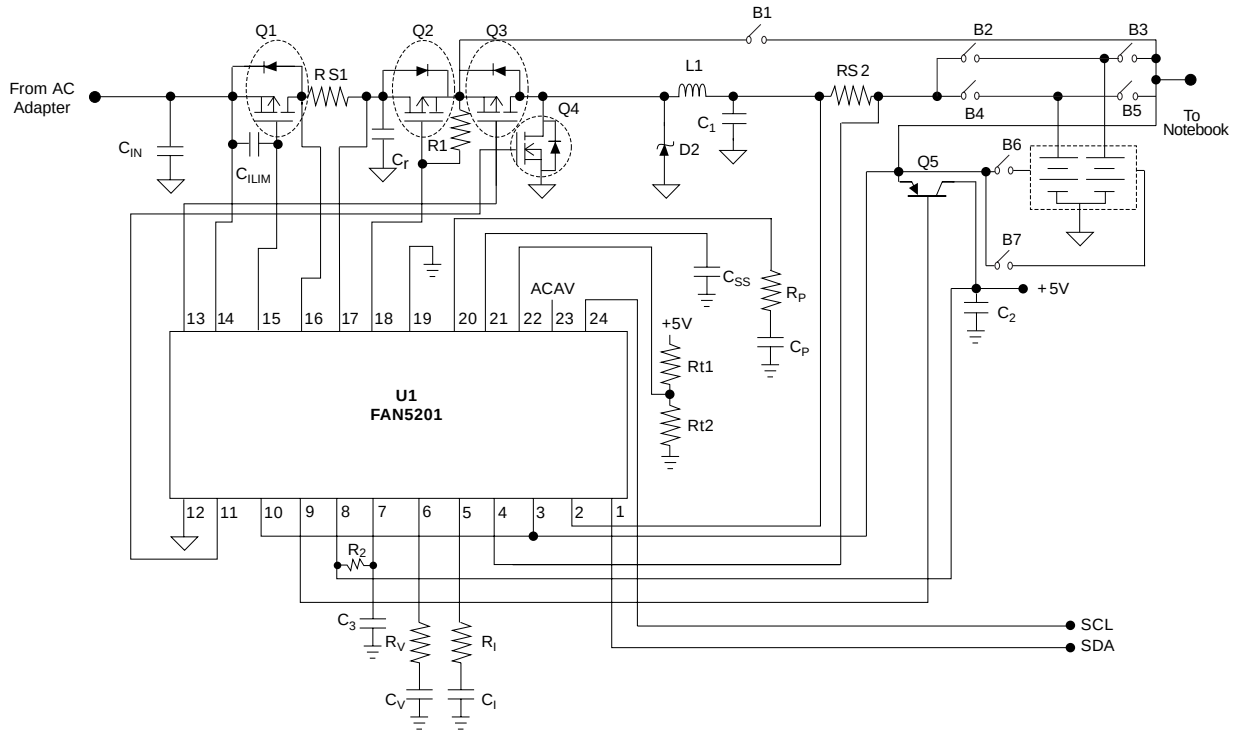


Figure 5. Two Battery Pack System

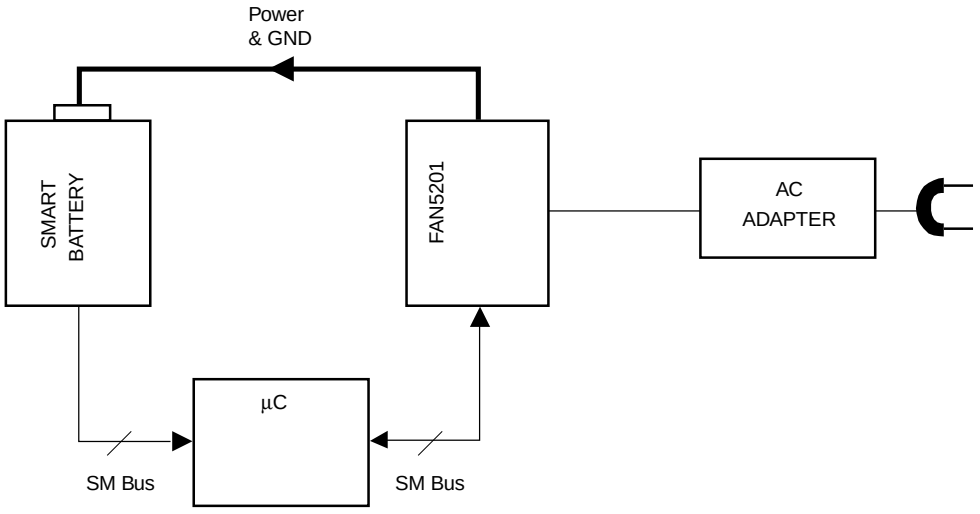


Figure 6. Typical Smart Battery System

SMBus Interface Specification

The FAN5201 is designed to fit in a system whose center is a microcontroller acting as an SMBus host. The host receives charging requests and other signals from a Smart Battery, and sends charging requests to the FAN5201 charger, in the process providing the necessary translations. The FAN5201 acts as a slave only. There is no direct communication between the charger and the battery. Note that the FAN5201 is NOT intended to be fully compliant with the Intel/Duracell Smart Battery System Specification. This document specifies ALL of the FAN5201's SMBus interface.

Slave Address

0001001b

Power On

The FAN5201 powers on with all DACs set to zero. All DACs must be written to before charging can begin. At power on, the Zero Current Bit is 0.

Supported Communications—Write Section (µC to IC)

Charging Current

The host sends the desired charging rate in mA.

- SMBus Protocol: Write Word
- Command Code: 0x14

Table 2. Charging Current Input and Output

Input	
Unsigned 2-Byte	Desired Charging Current
Units	mA
LSB	Bit 5
MSB	Bit 12
Output	
Scale	255 Steps (from 0 to full-scale)
Resolution	32mA (with 18mΩ sense resistor)

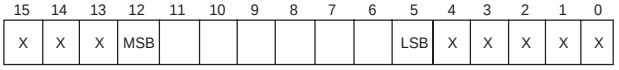


Figure 7. Charging Current Input and Output Word

For example, 0x0200 sets a charge current of 512mA by outputting (16/255) * FS, where FS = 8160mA.

Charging Voltage

The host sends the desired charging voltage in mV with an offset of 10V.

- SMBus Protocol: Write Word
- Command Code: 0x15

Table 3. Charging Voltage Input and Output

Input	
Unsigned 2-Byte	Desired Charging Voltage
Units	mV
LSB	Bit 5
MSB	Bit 12
Output	
Scale	255 Steps (from 0 to full-scale)
Resolution	32mV

Figure 8. Charging Voltage Input and Output Word

For example, 0x0200 sets a charging voltage of 10.512V by outputting (16/255) * FS +10V, where FS = 8.160V.

Charging Power

The host sends the maximum power available from the AC adapter in 5W increments with an offset of 25W.

- SMBus Protocol: Write Word
- Command Code: 0x17

Table 4. Charging Power Input and Output

Input	
Unsigned 2-Byte	Maximum Charging Power
Units	5W
LSB	Bit 0
MSB	Bit 3
Output	
Scale	15 Steps (from 0 to full-scale)
Resolution	5W (with 18mΩ sense resistor)

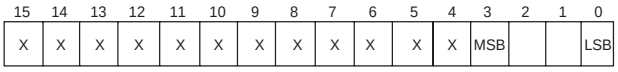


Figure 9. Charging Power Input and Output Word

For example, 0x0005 sets maximum charge power at 50W by outputting (5/15) * FS +25W, where FS = 75W.

Control Signals

The host sends a signal to set the IC into power down mode, and to reset the zero current flag.

When Power Down is sent to the IC, only the 5V linear regulator and the SMBus are on, all other systems are turned off.

The SMBus continues to latch incoming information in Power Down.

Zero Current Reset true (=1) resets the ZERO_CURRENT bit (in the charger status word) to 0 = valid. In order for the ZERO_CURRENT bit to function again, the Zero Current Reset bit must be set false (= 0) after this, otherwise the ZERO_CURRENT bit will remain in the valid state regardless of battery current.

- SMBus Protocol: Write Word
- Command Code: 0x18

Table 5. Control Signals

Field	Bit	Support
Power Down/Normal	1	0/1
Zero Current Reset	2	1 = TRUE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	ZCR	PD	X

Figure 10. Control Signals Word

For example, 0x0006 sets the IC in normal operation, and the zero current bit is reset.

Supported Communications—Read Section (µC to IC)

Charger Status

The host uses this command to read the charger's status bits.

VOLTAGE_NOTREG is set if the battery voltage is outside +10% of the programmed charging voltage.

CURRENT_NOTREG is set if the battery current is outside +10% of the programmed charging current.

ZERO_CURRENT is zero if the battery current is less than 200mA (with an 18mΩ sense resistor).

CURRENT_OR is zero if the battery current is >6A.

VOLTAGE_OR is zero if the battery voltage is >110% of the programmed charging voltage.

POWER_FAIL is set if the battery voltage is <8.5V.

- SMBus Protocol: Read Word
- Command Code: 0x13

Table 6. Charger Status Read

Field	Bit	Support
CHARGE_INHIBITED	0	Always 0, charger enabled
MASTER_MODE	1	Always 0, slave mode
VOLTAGE_NOTREG	2	0 = in regulation
CURRENT_NOTREG	3	0 = in regulation
LEVEL_2/3	4	Not supported
ZERO_CURRENT	5	0 = valid
CURRENT_OR	6	0 = valid
VOLTAGE_OR	7	0 = valid
THERMISTOR_OR	8	Not supported
THERMISTOR_COLD	9	Not Supported
THERMISTOR_HOT	10	Not Supported
THERMISTOR_UR	11	Not Supported
ALARM_INHIBITED	12	Not Supported
POWER_FAIL	13	0 = Voltage OK
BATTERY_PRESENT	14	Not Supported
AC_PRESENT	15	Always 1, charger present

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	X	0/1	X	X	X	X	X	0/1	0/1	0/1	X	0/1	0/1	0

Figure 11. Charger Status Word

For example, a normal operation charger might set this word to 0x8028 to show that the AC adapter is present, power is on, voltage is being regulated, and current is above minimum.

Charger Settings

The host uses this command to read the charger's settings.

- SMBus Protocol: Block Read
- Command Code: 0x3F

Table 7. Charger Settings Read

Field	Byte
Byte Count	Always set to 0x08
Charger Current Low Byte	1
Charger Current High Byte	2
Charger Voltage Low Byte	3
Charger Voltage High Byte	4
Charger Power Low Byte	5
Charger Power High Byte	6
Control Signal Low Byte	7
Control Signal High Byte	8

Non-Supported Communications

The following features are specified in the Intel/Duracell Smart Charger Specification, but are not directly supported by the FAN5201.

Thermistor Interface

Interface to the thermistor occurs exclusively through the host.

Typical Battery Communications

Charging current and voltage requests are intercepted by the host, which transmits them to the charger.

Critical Battery Communications

Overcharge and overtemperature communications are sent to the host, which transmits commands to the charger.

Bus Errors

Unsupported commands, data unavailable, busy or bad data are not transmitted to the host. The FAN5201 signals errors by witholding ACKnowledge (see protocols). It does not support any reads of error registers.

AlarmWarnings()

Alarm warnings are sent to the host, which transmits commands to the charger.

Chargermode() Settings

The ChargerMode() write command is unsupported. The command's effects may be obtained by sending the appropriate commands to the charger.

175 seconds Timeout

Supported by the host, not by the IC. Furthermore, it is recommended that a watchdog timer be used in conjunction with the host processor, to assure that the timeout is not affected by infinite software loops.

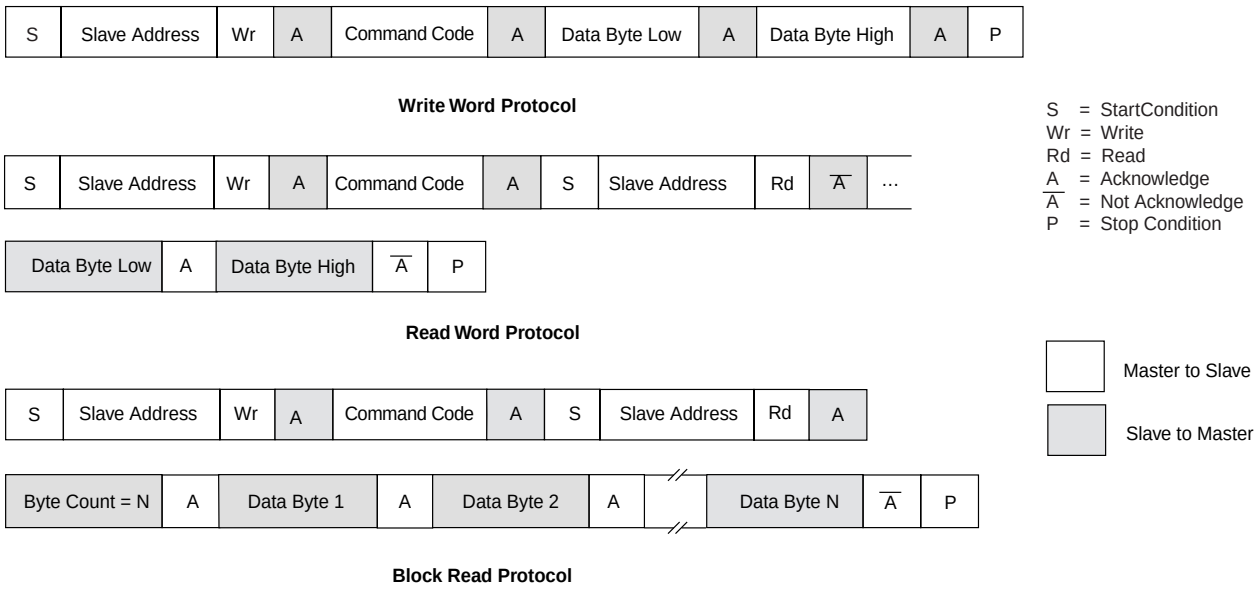


Figure 12. Read and Write Protocols

Timing Diagram

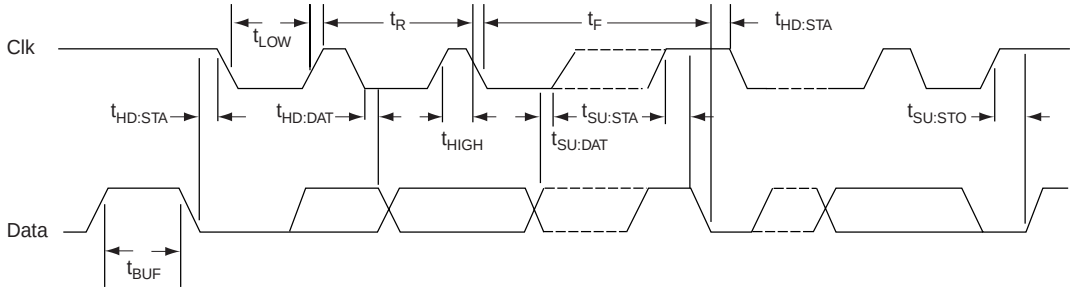


Figure 13. SMBus Timing Diagram

Preliminary Specification

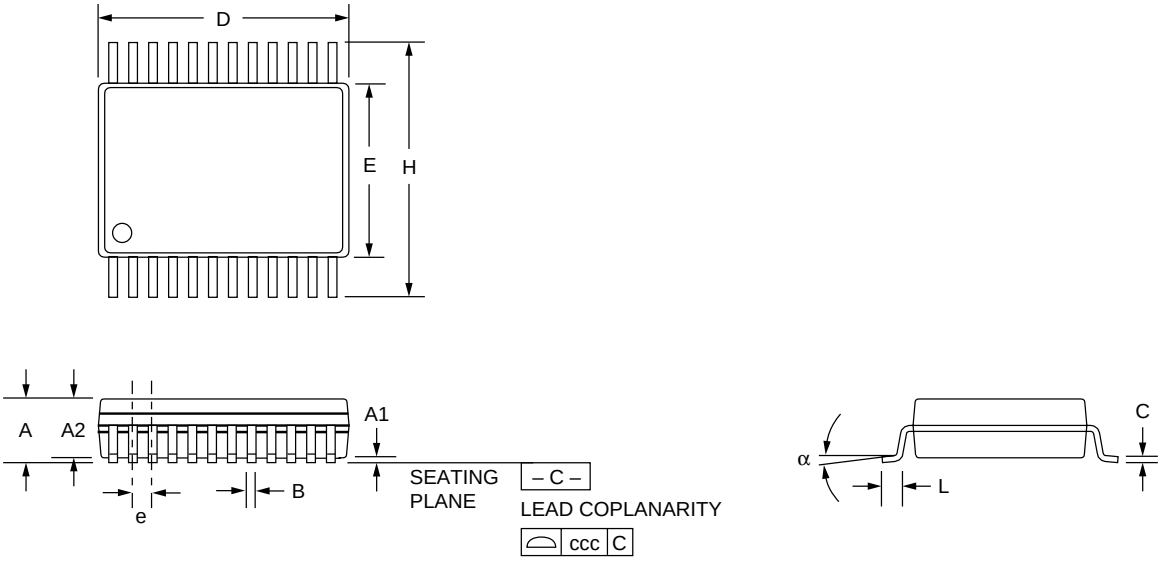
Mechanical Dimensions

24-Lead SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.078	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.010	.015	0.22	0.38	5
c	.0035	.010	0.09	0.25	5
D	.311	.335	7.90	8.50	2, 4
H	.291	.323	7.40	8.20	
E	.197	.220	5.00	5.60	2
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Preliminary Specification

Ordering Information

Product Number	Package
FAN5201MSA	24 Lead SSOP

Preliminary Specification

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
CoolFET™
CROSSVOLT™
E^2CMOS^{TM}
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench®
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic™
UHC™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.