

FAN8400D

Polygon Mirror Motor Drive IC

Features

- 3-Phase BLDC motor driver IC with speed control
- Phase Locked Loop (PLL) speed control
- Built-in phase locked detector output
- Current linear drive scheme
- External clock for arbitrary motor speed
- Built-in FG amplifier and integrating amplifier
- Auto Gain Control (AGC) circuit for compensation hall amplifier
- Built-in protection circuits (over-current limit, under-voltage limit, thermal shut down)

Description

The FAN8400D is a monolithic integrated circuit. it is one driver for laser beam printer (LBP) polygon mirror motor, which has single chip implementation of all circuits. For extremely high rotational precision, it employs the phase locked loop (PLL) speed control scheme.

28-SSOPH-375SG2



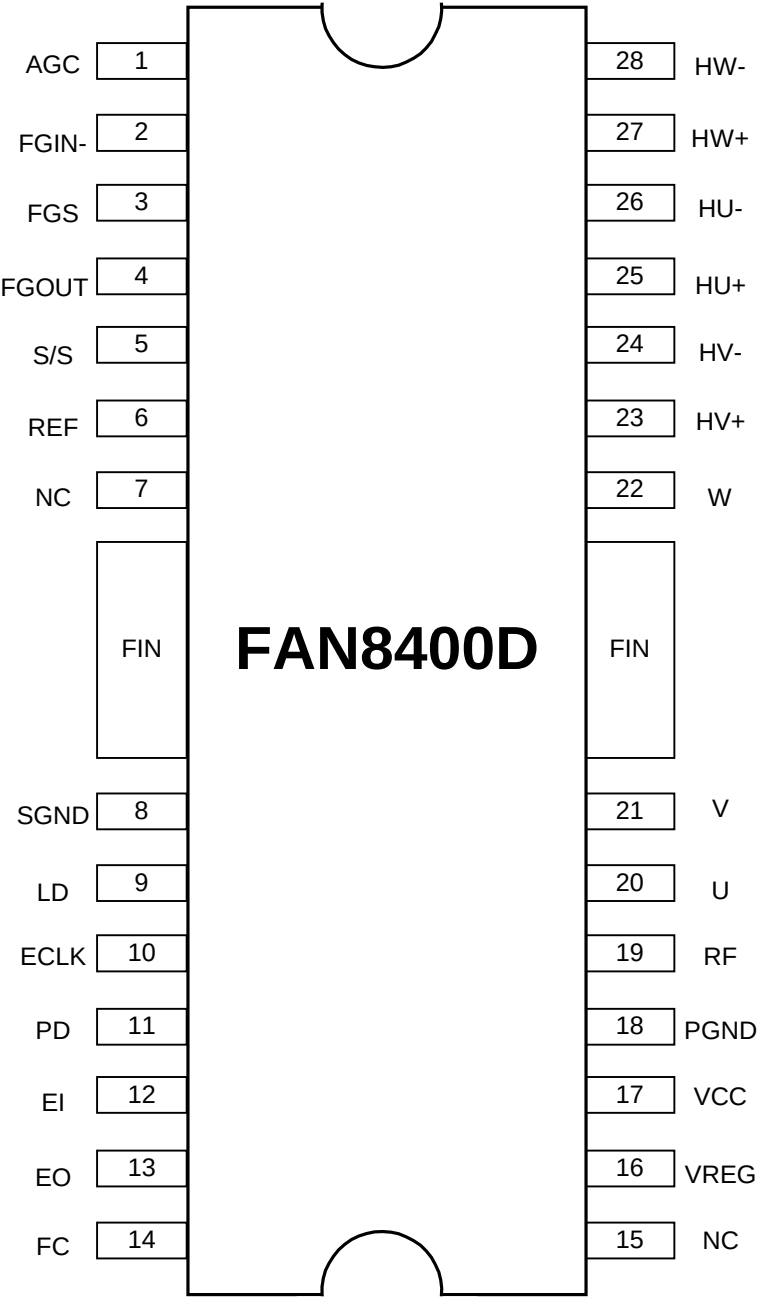
Typical application

- Polygon mirror motor drive IC for laser beam printer
- Polygon mirror motor drive IC for facsimile
- Polygon mirror motor drive IC for duplicator
- Polygon mirror motor drive IC for multi function printer
- General 3 phase BLDC motor drive IC

Ordering Information

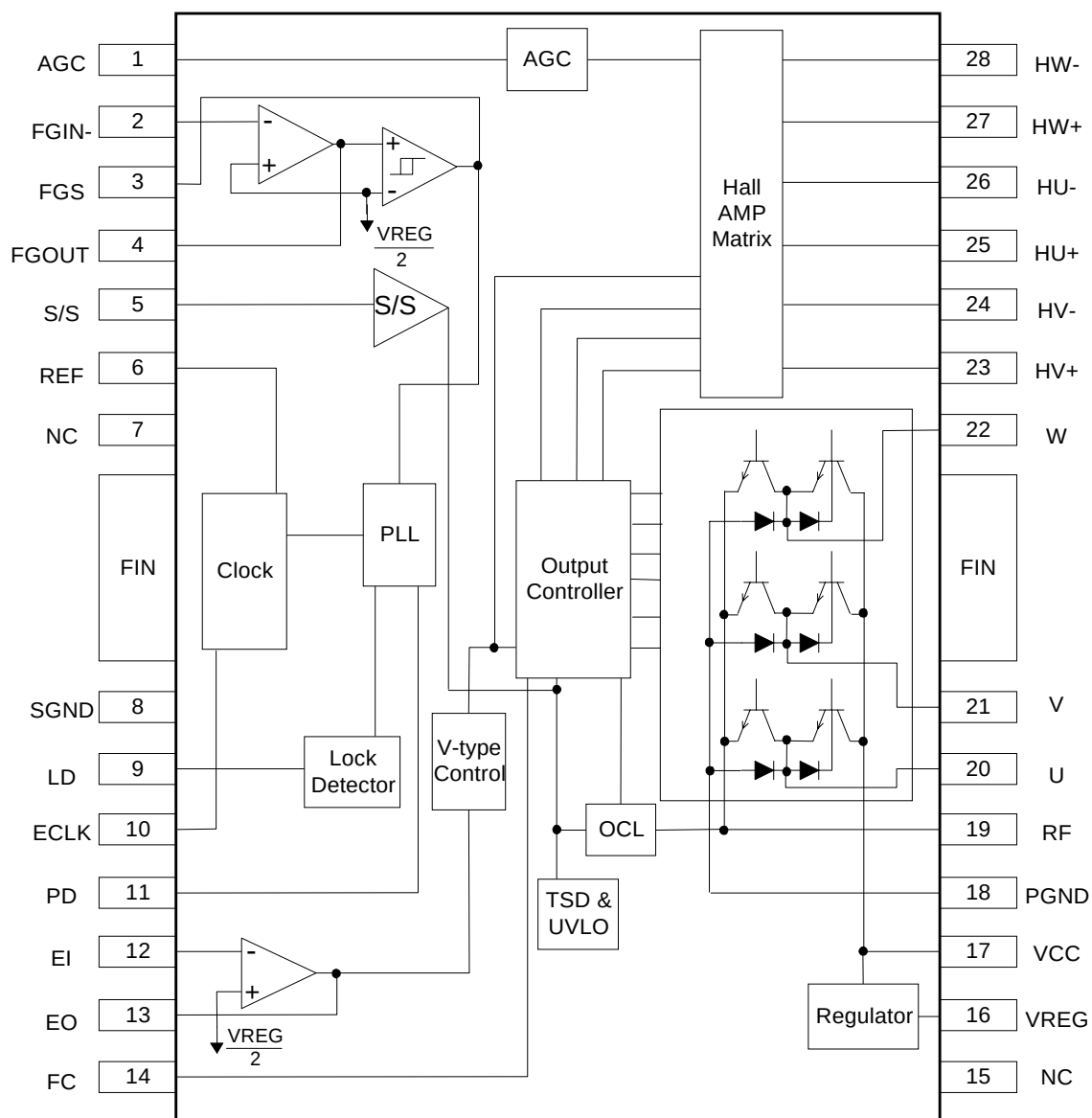
Device	Package	Operating Temp.
FAN8400D3	28-SSOPH-375SG2	-20°C ~ +80°C
FAN8400D3TF	28-SSOPH-375SG2	-20°C ~ +80°C

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGC	AGC amplifier frequency characteristics correction
2	FGIN-	FG amplifier inverting input
3	FGS	FG pulse output
4	FGOUT	FG amplifier output
5	S/S	Stop and start
6	REF	2.5V input
7	NC	-
8	SGND	Signal ground
9	LD	Phase locked loop detector output
10	ECLK	External clock
11	PD	Phase locked loop detector output
12	EI	Error amplifier inverting input
13	EO	Error amplifier output
14	FC	Control amplifier frequency correction
15	NC	-
16	VREG	Regulator voltage stabilization output
17	VCC	Power supply
18	PGND	Power ground
19	RF	Output current detection
20	U	U output
21	V	V output
22	W	W output
23	HV+	V hall amplifier non inverting input
24	HV-	V hall amplifier inverting input
25	HU+	U hall amplifier non inverting input
26	HU-	U hall amplifier inverting input
27	HW+	W hall amplifier non inverting input
28	HW-	W hall amplifier inverting input



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit	Remark
Maximum supply voltage	VCCMAX	30	V	-
Maximum output current	IOMAX	0.6	A	-
Power dissipation	Pd	1.7	W	-
Operating temperature	TOPR	-20 ~ +80	°C	-
Storage temperature	TSTG	-50 ~ +150	°C	-

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating voltage range	VCC	20	24	28	V

Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENT						
Low power supply current	ICCL	Stop mode, VCC=20V	20	30	40	mA
Typical power supply current	ICCT	Stop mode, VCC=24V	21	31	41	mA
High power supply current	ICCH	Stop mode, VCC=28V	22	32	42	mA
OUTPUT POWER TRANSISTOR CHARACTERISTICS (VAGC = 3.5V)						
U source saturation voltage (1)	VSATUU1	IO=0.6A, RF=0Ω	-	1.8	2.5	V
U source saturation voltage (2)	VSATUU2	IO=0.3A, RF=0Ω	-	1.6	2.3	V
U sink saturation voltage (1)	VSATUL1	IO=0.6A, RF=0Ω	-	0.5	1.0	V
U sink saturation voltage (2)	VSATUL2	IO=0.3A, RF=0Ω	-	0.25	0.7	V
V source saturation voltage (1)	VSATVU1	IO=0.6A, RF=0Ω	-	1.8	2.5	V
V source saturation voltage (2)	VSATVU2	IO=0.3A, RF=0Ω	-	1.6	2.3	V
V sink saturation voltage (1)	VSATVL1	IO=0.6A, RF=0Ω	-	0.5	1.0	V
V sink saturation voltage (2)	VSATVL2	IO=0.3A, RF=0Ω	-	0.25	0.7	V
W source saturation voltage (1)	VSATWU1	IO=0.6A, RF=0Ω	-	1.8	2.5	V
W source saturation voltage (2)	VSATWU2	IO=0.3A, RF=0Ω	-	1.6	2.3	V
W sink saturation voltage (1)	VSATWL1	IO=0.6A, RF=0Ω	-	0.5	1.0	V
W sink saturation voltage (2)	VSATWL2	IO=0.3A, RF=0Ω	-	0.25	0.7	V
U output leakage current	IOLEAKU	VCC=28V, OUT1=28V	-	-	100	μA
V output leakage current	IOLEAKV	VCC=28V, OUT2=28V	-	-	100	μA
W output leakage current	IOLEAKW	VCC=28V, OUT3=28V	-	-	100	μA
UNDER VOLTAGE LIMIT						
UVLO operating voltage	VSD	-	7.0	7.6	8.2	V
UVLO hysteresis	HVSD	-	1.0	1.3	1.6	V
REGULATOR VOLTAGE OUTPUT						
Regulator output voltage	VREG	-	5.8	6.3	6.8	V
Power supply variation	HVREG1	VCC=20~28V	-	-	100	mV
Load variation	HVREG2	ILOAD=0~10mA	-	-	100	mV
HALL AMPLIFIER INPUT BLOCK						
HU+ hall AMP input bias current	IBHA1+	-	-	2	10	μA
HU- hall AMP input bias current	IBHA1-	-	-	2	10	μA
HV+ hall AMP input bias current	IBHA2+	-	-	2	10	μA
HV- hall AMP input bias current	IBHA2-	-	-	2	10	μA
HW+ hall AMP input bias current	IBHA3+	-	-	2	10	μA
HW- hall AMP input bias current	IBHA3-	-	-	2	10	μA
Hall differential input range	VHIN	Sine wave input	50	-	350	mVp-p
Hall common input range	VICM	Differential input : 50mVP-P	3.5	-	VCC-3.5	V

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FG AMPLIFIER BLOCK						
FG AMP input bias current	IBFG	-	-1	-	1	μA
FG AMP DC bias level	VBFG	-	2.90	3.15	3.40	V
FG output high level voltage	VOHFG	No external load	VREG -1.1V	-	-	V
FG output low level voltage	VOLFG	No external load	-	0.8	1.2	V
FG SCHMIDT COMPARATOR BLOCK						
FGS high / low input hysteresis	VSHL	-	-50	0	50	mV
FGS low / high input hysteresis	VSLH	-	100	150	200	mV
FGS hysteresis	VFGL	-	100	-	200	mV
FGS input operating level	VFGSIL	-	400	-	-	mVp-p
FGS output saturation voltage	VFGSSAT	IFGS=4mA	-	0.2	0.4	V
FGS output leakage current	IFGSLEAK	VCC=28V	-	-	10	μA
ERROR AMPLIFIER BLOCK						
Error AMP input bias current	IBER	-	-1	-	1	μA
Error AMP DC bias level	VBER	-	2.90	3.15	3.40	V
Error output high level voltage	VOHER	No external load	VREG -1.1V	-	-	V
Error output low level voltage	VOLER	No external load	-	-	1.0	V
CURRENT LIMIT OPERATION						
RF output voltage limit	VRF	-	0.55	0.60	0.65	V
CONTROLLER BLOCK						
Dead zone	VDZ	-	50	100	300	mV
Output idle voltage	VID	-	-	-	5	mV
Forward gain	GDF+	-	0.4	0.5	0.6	-
Reverse gain	GDF-	-	-0.6	-0.5	-0.4	-
Accelerate command voltage	VSTA	-	VREG -1.1V	-	-	V
Decelerate command voltage	VSTO	-	-	0.8	1.5	V
Forward limit voltage	VL+	RF=22Ω	-	0.60	-	V
Reverse limit voltage	VL-	RF=22Ω	-	0.60	-	V
PHASE COMPARATOR OUTPUT BLOCK						
PD output high level voltage	VPDH	No external load	5.2	-	-	V
PD output low level voltage	VPDL	No external load	-	-	0.7	V
PD output source current	IPD+	VPD=0.5*VREG	-	-	-0.6	mA
PD output sink current	IPD-	VPD=0.5*VREG	1.0	-	-	mA
PHASE LOCKED LOOP DETECTOR OUTPUT BLOCK						
LD output saturation voltage	VLDSAT	ILD=5mA	-	0.1	0.4	V
LD output leakage current	ILDLEAK	VCC=28V	-	-	10	μA

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTERNAL CLOCK INPUT BLOCK						
External input frequency	FCLK	External clock mode	0.5	-	7.0	KHz
ECLK input open voltage	VIOCLK	-	3.7	4.2	4.7	V
ECLK input high level current	IIHCLK	VCLK=VREG	100	150	200	μA
ECLK input low level current	IILCLK	VCLK=0V	-400	-300	-200	μA
S/S BLOCK						
S/S input high level voltage	VIHSS	-	3.0	-	VREG	V
S/S input low level voltage	VILSS	-	0	-	1.5	V
S/S hysteresis	VISSS	-	0.3	0.5	0.7	V
S/S input open voltage	VIOSS	-	3.7	4.2	4.7	V
S/S input high level current	IIHSS	VSS=VREG	100	150	200	μA
S/S input low level current	IILSS	VSS=0V	-400	-300	-200	μA
REFERENCE BLOCK						
REF input level voltage	VIREF	-	2.0	-	3.0	V
REF input open voltage	VION2	-	3.7	4.2	4.7	V
REF input high level current	IIHN2	VREF=VREG	100	150	200	μA
REF input low level current	IILN2	VREF=0V	-400	-300	-200	μA

Application Information

1. Output Block

- 3 Phase power transistor and free wheeling diodes
- Reverse active type upper side diodes and parasitic lower side diodes
- full wave current linear drive with current feedback
- Connection with external capacitor to prevent voltage spike and oscillation by current drive
- Output transistor commutation by "Winner takes all" method
- Built in over current limit (OCL) circuit

2. Hall AMP Block

- Detection of rotor position using 3 phase hall sensors
- Determination of output commutation by hall signal

Hall U	Hall V	Hall W	Forward torque [Reverse torque]		
			Output U	Output V	Output W
H	L	H	L [H]	H [L]	M [M]
H	L	L	L [H]	M [M]	H [L]
H	H	L	M [M]	L [M]	H [L]
L	H	L	H [L]	L [H]	M [M]
L	H	H	H [L]	M [M]	L [H]
L	L	H	M [M]	H [L]	L [H]

3. AGC Block

- This block is remained output amplitude.
- It is controlled by envelope through hall signals.

$$V_{AGC} \propto \frac{1}{H_{NI} - H_I}$$

NOTES:

V_{AGC} is voltage of AGC output.

H_{NI} is hall non inverting input voltage.

H_I is hall inverting voltage.

4. Speed Control Block

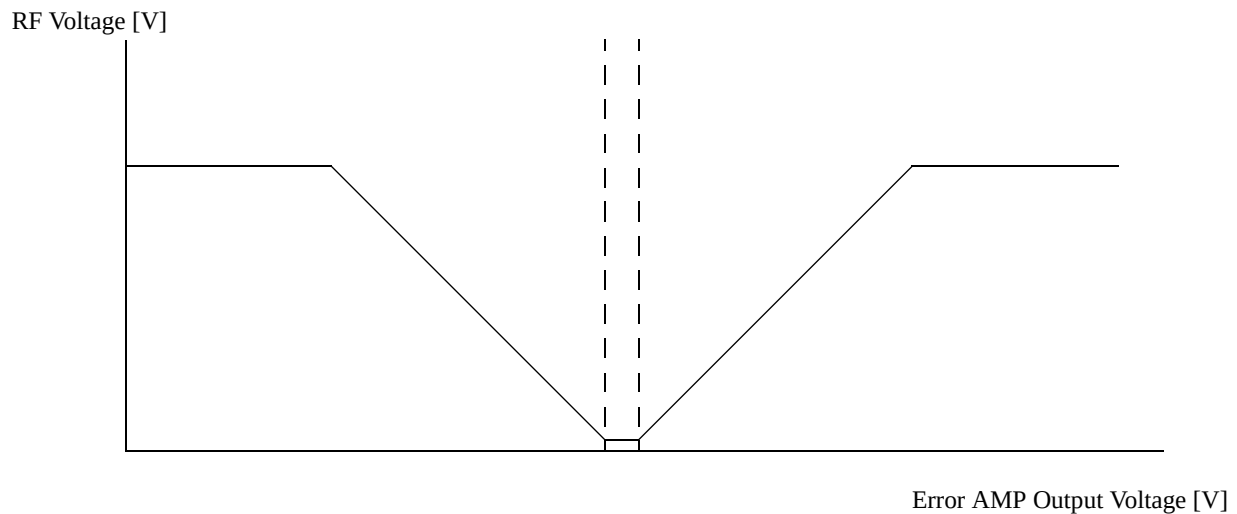
- Digital phase locked loop (PLL) circuit
- Generating error pulse between rising edge of clock and falling edge of FG signal.
- High precision stable speed control

5. FG AMP & FG Schmidt Comparator Block

- This block measures of motor rotation speed and controls motor speed.
- It is determined FG AMP gain and filter by external component.
- FG schmidt block change sine wave form to square wave form

6. Error AMP Block

- It composes of dumping filter and ripple filter by external component.
- It determines output amplitude of error AMP by width error pulse.
- It is determined output current by output amplitude of error AMP.
- Bidirectional torque control



7. Regulator Block

- Power supply of control circuits in inside.
- Band gap reference circuits.

8. Lock Detector

- It is low when FG frequency reaches capture range of clock frequency.
- Open correct

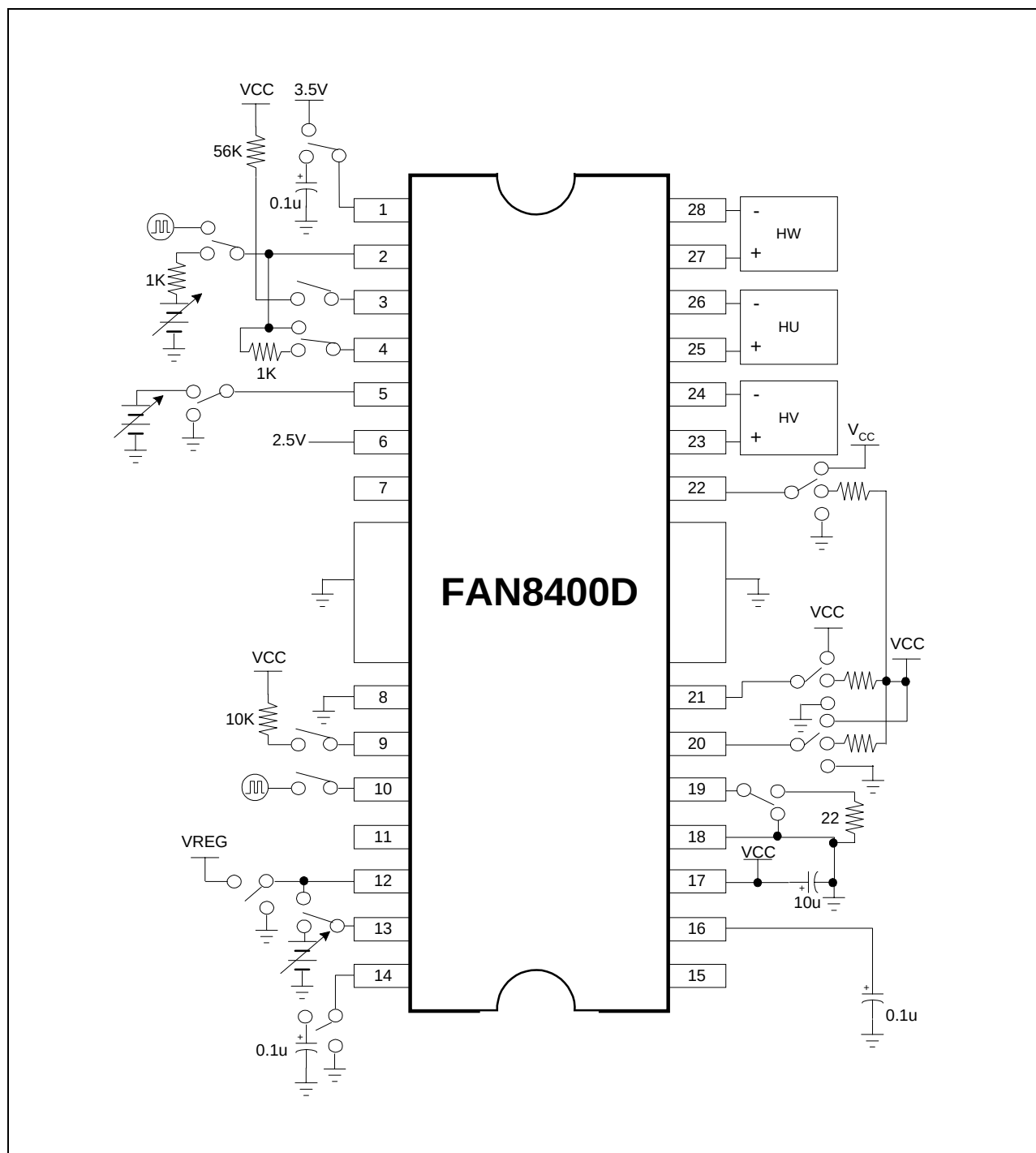
9. FG Pulse Output

- Monitoring pin for motor rotative speed
- Open correct

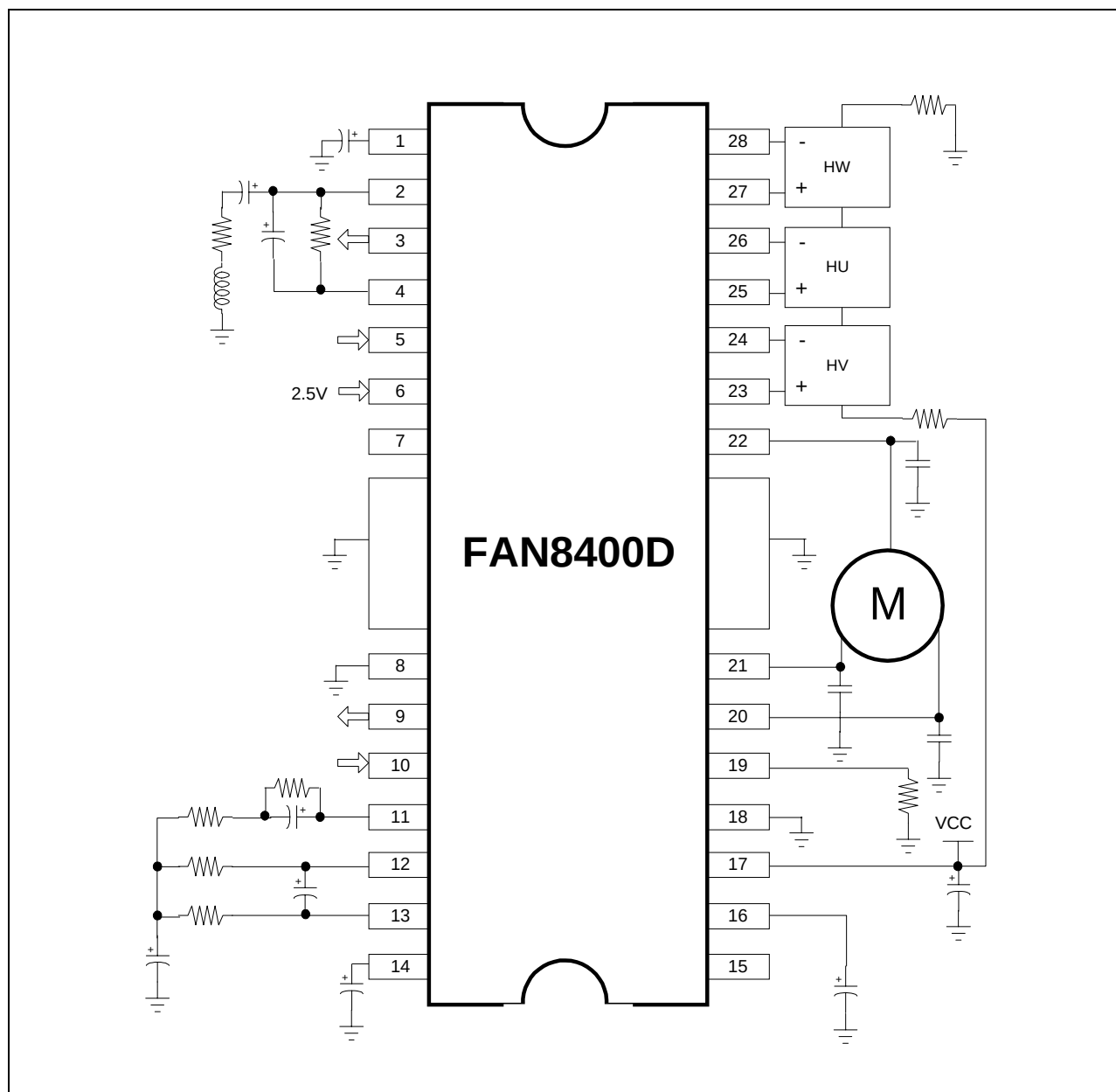
10. Stop And Start

- Stop mode: Open or high voltage
- Start mode: Low voltage

Test Circuits



Typical Application Circuits



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