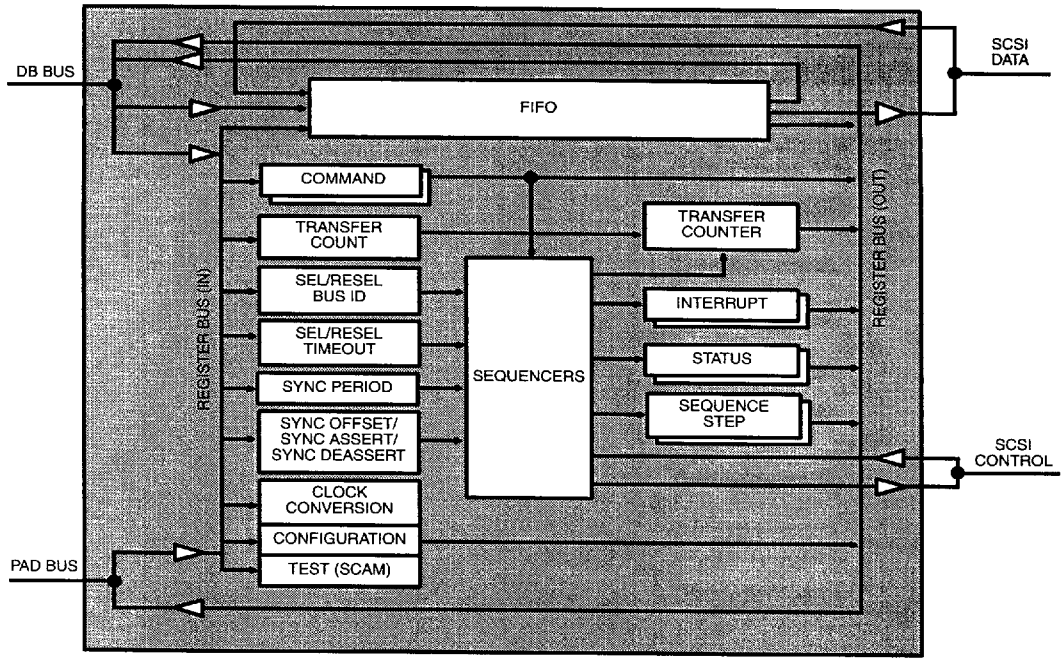
QLogic Corporation

FAS216/216U/236/236U
Fast Architecture SCSI Processor

Data Sheet

Features

- Host application and 16-bit peripheral application support
- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI X3T10/1071D Fast-20 standard
- Asynchronous data transfers up to 7 Mbytes/sec
- Synchronous data transfers up to 5 Mbytes/sec (normal SCSI), 10 Mbytes/sec (fast SCSI), and 20 Mbytes/sec (Ultra SCSI)
  - Programmable synchronous transfer period
  - Programmable synchronous transfer offsets up to 15 bytes
- 24-bit transfer counter
- Initiator and target modes
- Differential driver protection (DIFFSENS)
- Direct memory access (DMA) burst transfer rate up to 20 Mbytes/sec
- Pipelined command structure
- 16-byte data FIFO between DMA and SCSI channels
- Parity pass-through on FIFO data
- Part-unique ID code
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Clock rates up to 40 MHz



NOTE: SCAM APPLIES TO THE FAS216U AND FAS236U ONLY.

Figure 1. FAS2x6 Block Diagram

NOTE: Throughout this data sheet, the term *FAS2x6* refers to the FAS216, FAS216U, FAS236, and FAS236U unless otherwise noted.

Product Description

The FAS2x6 chips are part of the QLogic SCSI processor family with features designed to facilitate SCSI-2 support (FAS216 and FAS236) and SCSI-3 support (FAS216U and FAS236U). The FAS216 and FAS236 can transfer synchronous data at 10 Mbytes/sec. The FAS216U and FAS236U can transfer data at 20 Mbytes/sec with SCAM support. The normal 5-Mbytes/sec transfer rate and the fast 10-Mbytes/sec transfer rate (FAS216U and FAS236U) are supported on-chip by setting the FASTSCSI bit (Configuration 3 register bit 4). Asynchronous transfers up to 7 Mbytes/sec are also supported. The FAS216U and FAS236U chips are firmware and pin compatible with the FAS216 and FAS236 chips, respectively. Figure 1 shows the FAS2x6 block diagram.

The FAS2x6 replaces existing SCSI interface circuitry, which typically consists of discrete devices, an external driver, and a low-performance SCSI interface chip. The FAS2x6 contains a fast DMA interface; a 16-byte FIFO; and fast asynchronous and synchronous data interfaces to the SCSI bus, including drivers in single-ended mode. Differential mode requires external drivers.

The FAS216 and FAS216U support single-ended mode; the FAS236 and FAS236U support single-ended and differential modes. Since the FAS2x6 operates in both initiator and target modes, it can be used in both host and peripheral applications. The chip performs such functions as bus arbitration, selection of a target, and reselection of an initiator. The FAS2x6 also handles message, command, status, and data transfers between the SCSI bus and its internal FIFO or between the SCSI bus and buffer memory. The chip maximizes protocol efficiency by utilizing a FIFO command pipeline and combination commands to minimize host intervention.

Differential Driver Protection (FAS236/236U Only)

The FAS236/236U pins 5 (DIFFSENS) and 7 (EDIFFS) support the SCSI DIFFSENS differential driver protection function.

The DIFFSENS function is enabled in differential mode when pins 5 and 7 are pulled up by an external device. The FAS236/236U is configured for differential mode operations when pin 87 (DIFFM) is low. If a single-ended device or terminator is connected while the chip is configured for differential operations, DIFFSENS becomes grounded, disabling the differential drivers. The Gross Error bit (Status register bit 6) is set and a disconnect interrupt is generated. The Gross Error bit and the disconnect interrupt are asserted as long as the DIFFSENS condition exists. The DIFFSENS function has no effect in single-ended mode.

SCAM Implementation

The FAS216U and FAS236U support levels 1 and 2 of the SCAM protocol. SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the chip hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

System Organization

The FAS2x6 controller systems support three main buses: the 8- or 16-bit data bus (DB), the 8-bit microprocessor address and data bus (PAD), and the 8-bit SCSI bus. The DB provides a path for DMA transfers through the FIFO. The PAD bus provides access to all internal registers. The FAS2x6 supports parity pass-through from the SCSI bus through the FIFO to the DB. This versatile split-bus architecture separates the two high-traffic information flows, the SCSI bus and DB bus, to provide maximum efficiency and throughput. Single- or split-bus configurations with 8- or 16-bit DMA are pin selectable. Table 1 shows chip operating conditions.

Interfaces

The FAS2x6 acts as an interface between the microprocessor and the SCSI bus in target or initiator mode. The other interfaces are described below:

- **Microprocessor Interface.** The DB or PAD bus is the microprocessor interface to the FAS2x6. Both buses allow the microprocessor 8-bit read and write access to all chip registers, including the FIFO. The PAD bus allows microprocessor interface to the chip registers independent of DMA activity on the DB.
- **DMA Interface.** The FAS2x6 logic transfers data to and from a buffer over the DB configured as 8 or 16 bits. (Each byte on the bus has its own parity.) If byte control mode (Configuration 2 register bit 5) is set, an external DMA controller can dictate how the bytes are placed on the bus.

Packaging

The pin diagrams for the FAS216/216U and FAS236/236U are shown in figures 2 and 3. Pins that support the FAS216/216U and FAS236/236U operations are shown in figures 4 and 5. Dimensions for the FAS216/216U 84-pin plastic leaderless chip carrier (PLCC) and the FAS236/236U 100-pin plastic quad flat pack (PQFP) are shown in figures 6 and 7.

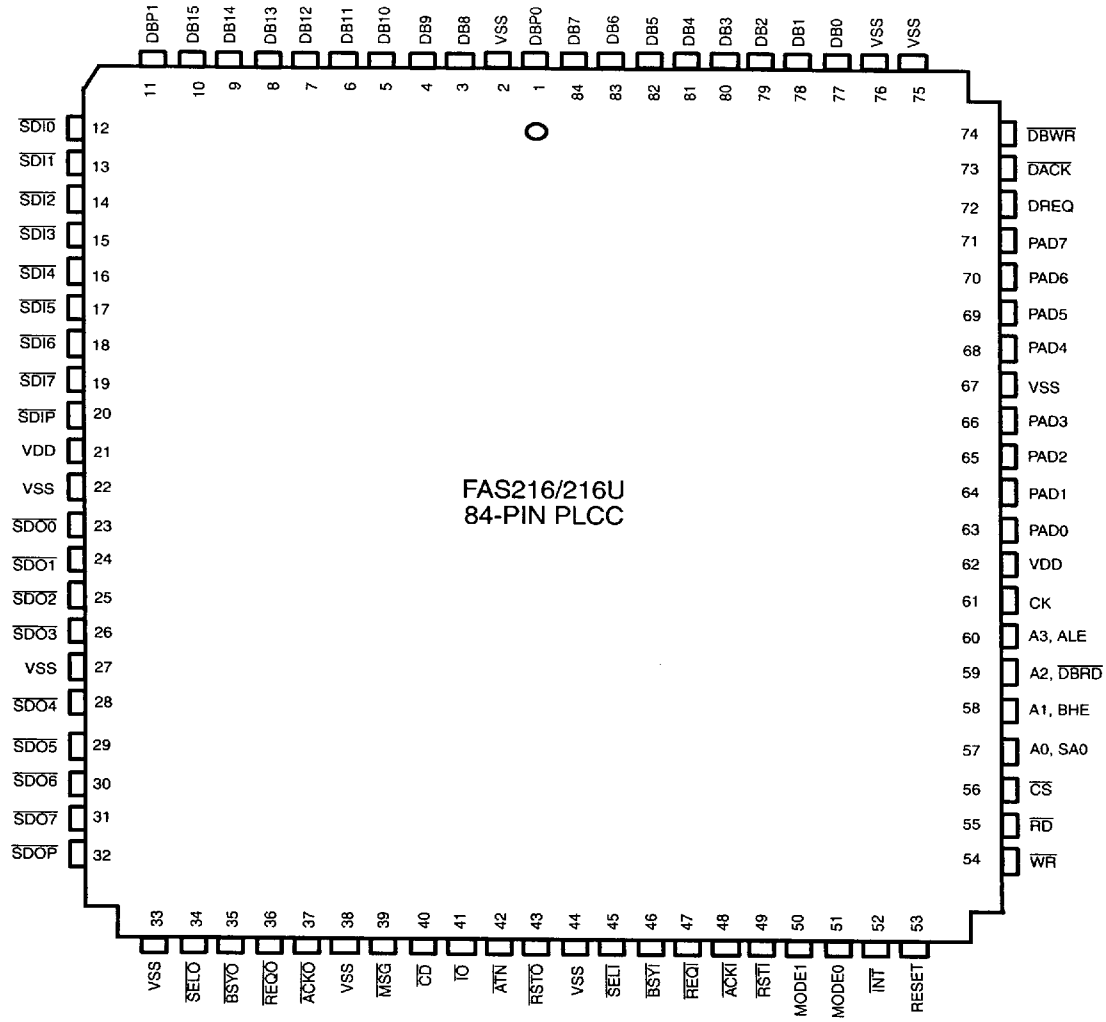


Figure 2. FAS216/216U 84-Pin PLCC Pin Diagram

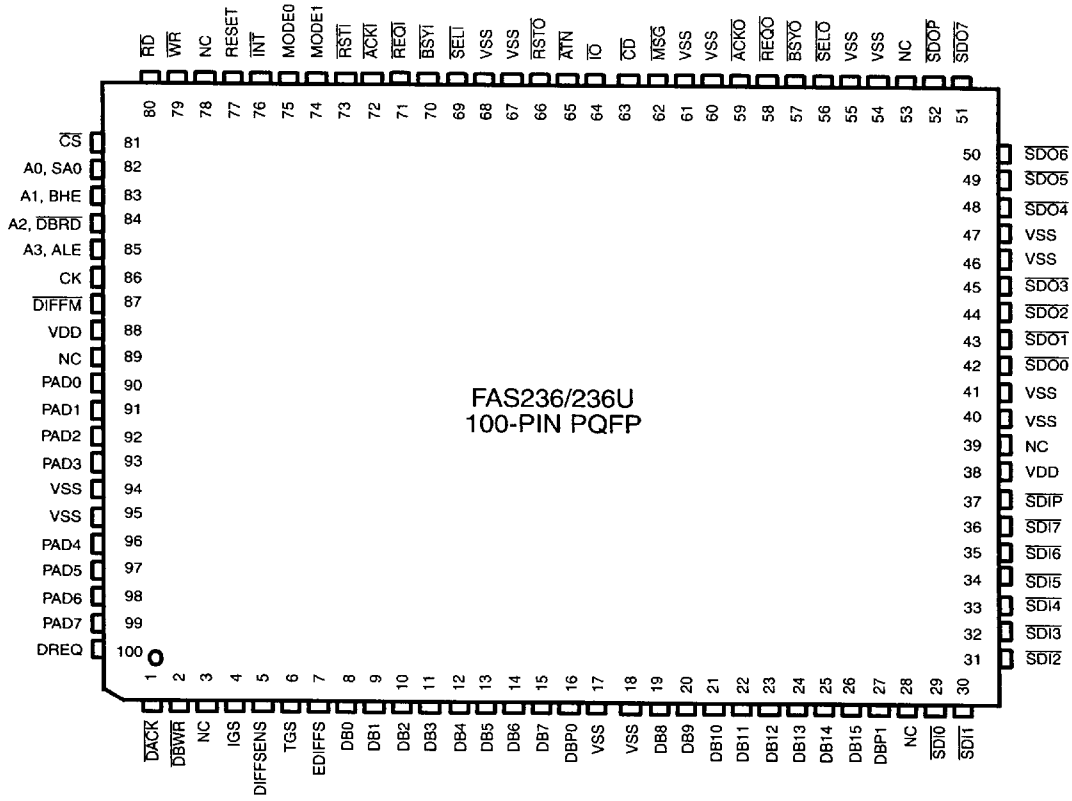
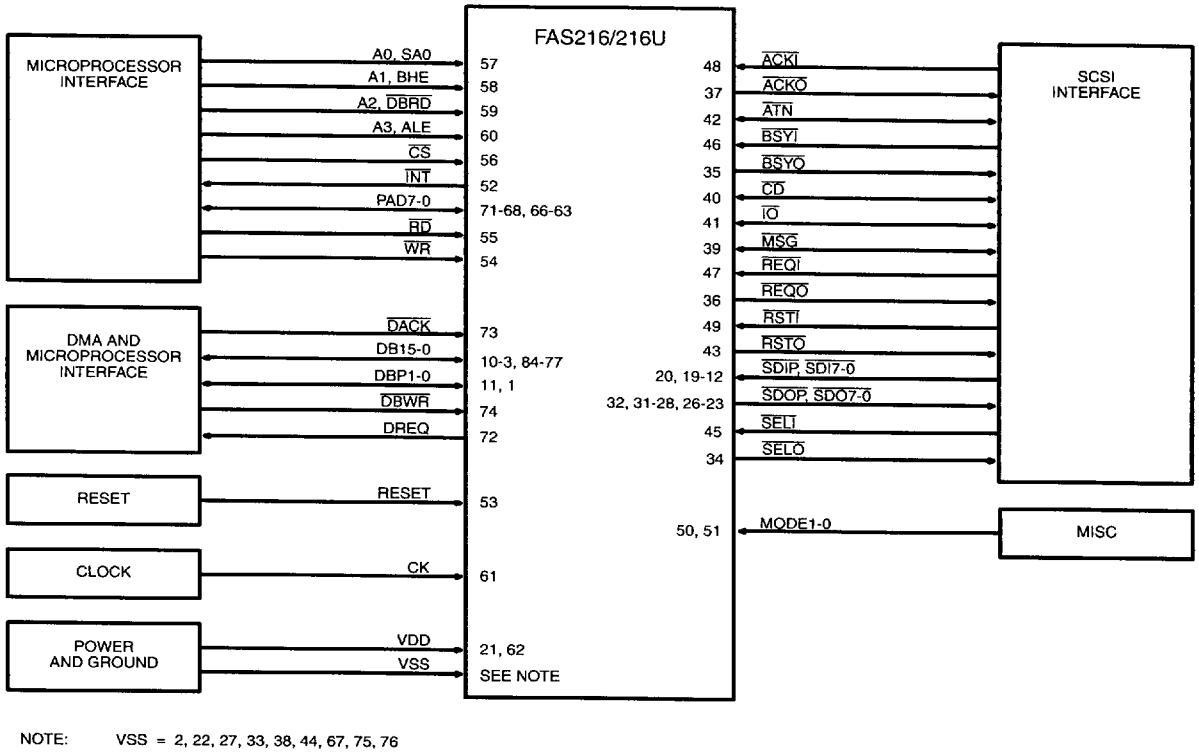
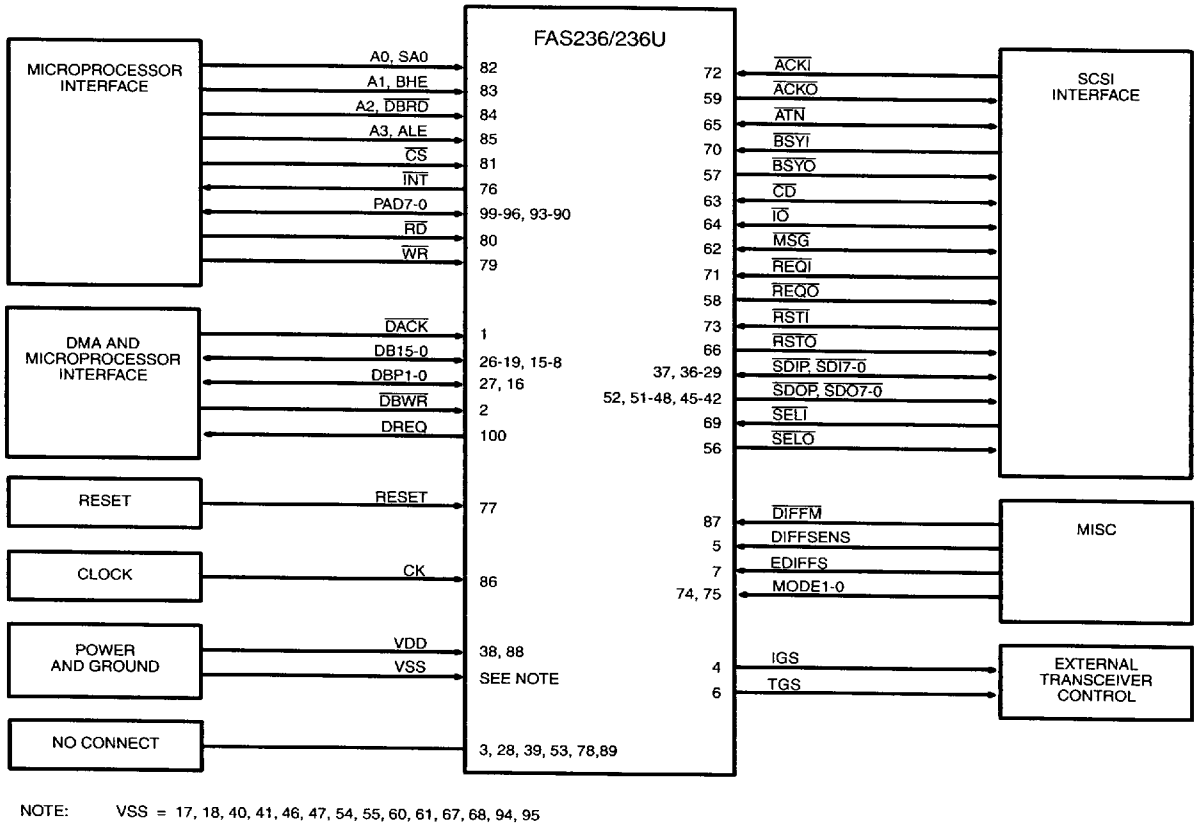


Figure 3. FAS236/236U Pin Diagram



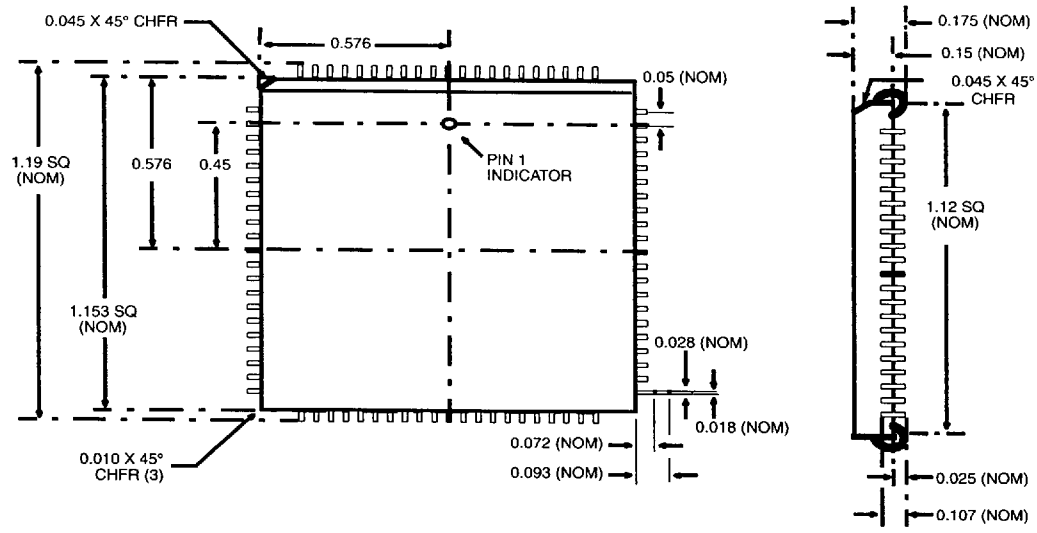
NOTE: VSS = 2, 22, 27, 33, 38, 44, 67, 75, 76

Figure 4. FAS216/216U Functional Signal Grouping



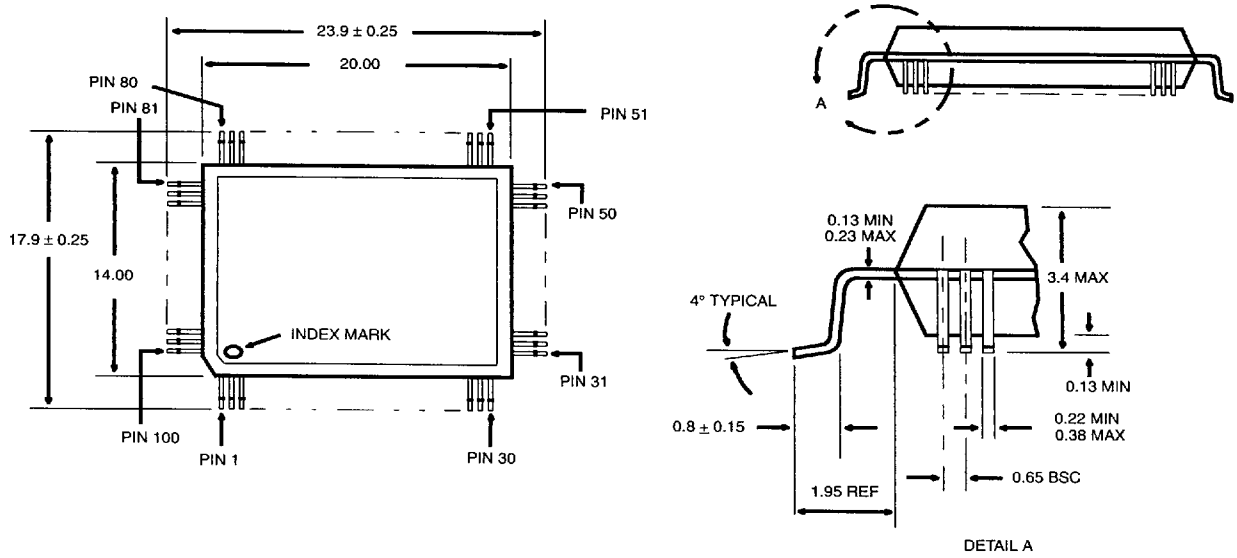
NOTE: VSS = 17, 18, 40, 41, 46, 47, 54, 55, 60, 61, 67, 68, 94, 95

Figure 5. FAS236/236U Functional Signal Grouping



NOTE: ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ARE NOMINAL UNLESS SPECIFIED OTHERWISE.

Figure 6. FAS216/216U 84-Pin PLCC Mechanical Drawings



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.
ALL DIMENSIONS ARE NOMINAL UNLESS SPECIFIED OTHERWISE.

Figure 7. FAS236/236U 100-Pin PQFP Mechanical Drawings

Electrical Characteristics

Table 1. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
VDD	Supply voltage	4.75	5.25	V
IDD[a]	Supply current (static IDD)		4	mA
IDD[b]	Supply current (dynamic IDD)		40-60	mA
TA	Ambient temperature	0	70	°C

Table Notes
Conditions not within operating conditions but within the absolute maximum stress ratings may cause the chip to malfunction
[a]Static IDD is measured with no clocks running and all inputs forced to VDD, all outputs unloaded, and all bidirectional pins configure as inputs.
[b]Dynamic IDD is dependent on the application.