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FDC37C75

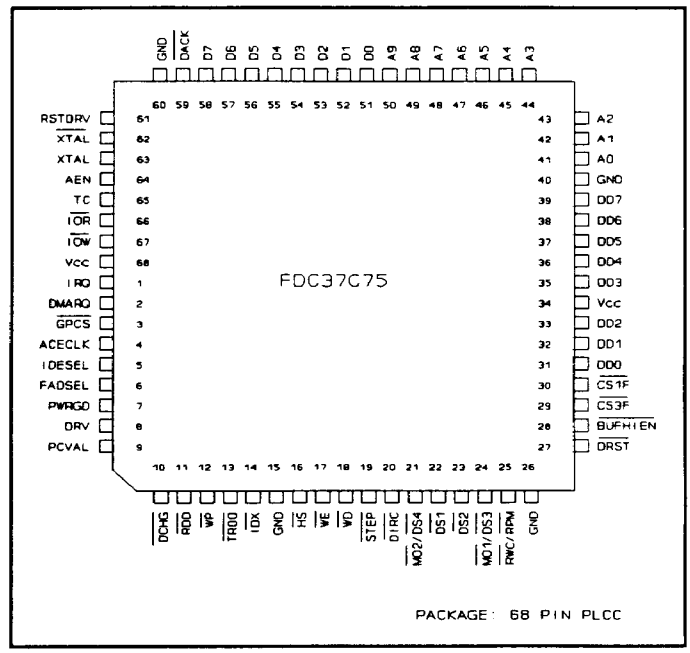
PRELIMINARY INFORMATION

Paddle Chip/Floppy Disk Subsystem Controller

FEATURES

- Provides complete "Paddle Card" function with the addition of just one 'HCT245 and optional 'HCT240
- Complete Floppy Disk Control System, Integrating:
  - Floppy Disk Formatter/Controller
  - IBM® PC/AT® Bus Interface
  - Address Decoder
  - Data Separator
  - Drive Interface
  - Write Precompensation Generator
  - Data Rate Selector
  - Clock Generator
- Includes IDE Interface/Decoder
- IBM PC/AT Compatible Format (Single and Double Density)
  - Provides Required Signal Qualification to DMA Channel (in PC/AT Mode)
  - BIOS Compatible
  - Supports Dual Speed Spindle Drive
- Enhanced Host Interface:
  - Supports 12 MHz, 286 µP With 0 Wait States
  - 24 mA bus drivers
- Direct Floppy Disk Drive Interface
  - 48 mA Drivers
  - Schmitt Trigger Inputs
- Multisector and Multitrack Transfer
- Internal Address Mark Detection Circuitry
- User Programmable Track Stepping Rate and Head Load/Unload Time
- Controls up to Four Drives
- Automatic Write Precompensation
- Internal Power-Up Reset Circuitry
- Pin Controlled Power Management

PIN CONFIGURATION



- Data Transfer in DMA or Non-DMA Mode
- Parallel Seek Operations
- On Chip Clock Generation Requires Just One 48 MHz Crystal for All Functions
- 1.8432 MHz Clock Output
- Game Port Chip Select Output
- Low Power CMOS; Single +5 V Supply

GENERAL DESCRIPTION

The FDC37C75 combines a floppy disk formatter/controller, high performance data separator, write precompensation generator, data rate selector, clock generator, and IDE interface/decoder/driver in one 68 pin PLCC package. High current drivers on all outputs, and TTL compatible Schmitt trigger circuits on all floppy disk drive inputs allow direct host and drive connection.

The host interface supports a 12 MHz PC/AT bus without the use of wait states to ensure optimal system performance.

The internal IDE interface/decoder and AT bus address decoder eliminate the external address decoder circuitry previously required for both the floppy disk controller and ATA compatible drive. External components are further reduced by the high current drivers of the FDC37C75. All drive related outputs can sink 48 mA; all host related outputs can sink 24 mA. All floppy disk drive related inputs have internal Schmitt triggers.

The FDC37C75 utilizes the SMC CMOS 765 core for guaranteed compatibility with existing software. The high performance digital data separator requires no external components to provide low error rates with high bit jitter tolerance.

Pin controlled power management provides power-down mode with all register contents preserved.

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DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
HOST PROCESSOR INTERFACE			
51 - 58	Data 0-7	D0-D7	Input/Output. The data bus connection to the host microprocessor. These pins are used by the host to transmit data to and from the FDC37C75 and are in the high-impedance state when not being used.
66	$\overline{\text{Read}}$	$\overline{\text{IOR}}$	Input. This active low signal is issued by the host microprocessor to indicate a read operation. A low pulse on this input when the FDC37C75 is selected enables data from the Buffer or Status Register onto the data bus for reading by the host.
67	$\overline{\text{Write}}$	$\overline{\text{IOW}}$	Input. This active low signal is issued by the host microprocessor to indicate a write operation. A low pulse on this input when the FDC37C75 is selected enables data from the data bus to be written into the FDC37C75.
64	Address Enable	AEN	Input. This active high signal allows DMA data transfers to occur. When AEN = "1", the DMA controller has control of the address bus, $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$. When AEN = "0", addresses to the FDC37C75 are valid.
2	Direct Memory Access Request	DMARQ	Output. This active high signal is a DMA request for byte transfers of data. This signal is cleared when the host responds with the $\overline{\text{DACK}}$ signal going low. This signal is normally driven in the Base Mode. When the FDC37C75 is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN from the Digital Output Register.
59	$\overline{\text{DMA Acknowledge}}$	$\overline{\text{DACK}}$	Input. A low level on this pin indicates a response by the host to a DMA request. It is used by the DMA controller to transfer data to or from the FDC37C75. In Special or PC/AT mode, this signal is qualified by DMAEN from the Digital Output Register.
65	Terminal Count	TC	Input. This active high signal indicates to the FDC37C75 that data transfer is complete. In Base Mode, TC will be qualified by $\overline{\text{DACK}}$ only in DMA operations. In non-DMA (Programmed I/O) operations the $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ signals are used as a gating function. In Special or PC/AT mode, TC will be qualified by $\overline{\text{DACK}}$ (whether in DMA or non-DMA operations) if DMAEN from the Digital Output Register is a logic "1". In PC/AT mode, non-DMA operations will occur successfully but will cause an abnormal termination error at the completion of a command.
1	Drive Interrupt	IRQ	Output. This signal is an interrupt indicating the completion of command execution or data transfer requests (in non-DMA operations). This signal is normally driven in the Base mode. When the FDC37C75 is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN signal for the Digital Output Register.
61	Reset	RSTDRV	Input. This active high signal resets the FDC37C75. When RSTDRV occurs, the FDC37C75 defaults to Base Mode and the data rate is defaulted to 250K MFM. When RSTDRV is active, the high current driver outputs to the disk drive are disabled. RSTDRV is inverted and buffered to provide the $\overline{\text{DRST}}$ signal to the IDE interface.
41 - 50	Address 0-9	A0-A9	Inputs. These TTL level inputs are tied to the PC/AT bus address bits SA0-SA9 and generate the internal register addresses and register load enables. In addition, these bits are used to generate the $\overline{\text{BUFHIEN}}$ and Chip Select signals $\overline{\text{CS1F}}$ and $\overline{\text{CS3F}}$ for the IDE drive, the Game Port Chip Select, and to gate the Disk Change status bit onto data bit D7 during a read of Register 3F7H.
6	Floppy Disk Address Select	FADSEL	Input. This TTL input with internal pull-up resistor is used to select the Primary or Secondary floppy disk controller AT addresses. When FADSEL = "1", the Primary Addresses are selected. When FADSEL = "0", the Secondary Addresses are selected.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
DRIVE INTERFACE			
11	Read Disk Data	RDD	Input. Raw serial bit stream from the disk drive. Each falling edge represents a flux transition of the encoded data.
17	Write Enable	WE	Output. This active low driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
18	Write Data	WD	Output. This active low driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
16	Head Select	HS	Output. This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
20	Direction Control	DIRC	Output. This high current output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
19	Step Pulse	STEP	Output. This active low high-current driver issues a low pulse for each track-to-track movement of the head.
10	Disk Change	DCHG	Input. This active low input senses from the disk drive that the drive door is open or that the diskette has possibly been changed since the last drive selection.
22	Drive Select 1	DS1	Output. This is an active low high-current output. When the FDC37C75 is in the PC/AT Mode, a logic "0" on DSEL and a logic "1" on MOEN1 from the Digital Output Register will cause the signal to enable the drive number 1 interface. When the FDC37C75 is in the Base Mode or the Special Mode, this output is number 1 of the four decoded Unit Selects, as specified in the device command syntax.
23	Drive Select 2	DS2	Output. This is an active low high-current output. When the FDC37C75 is in the PC/AT Mode, a logic "0" on DSEL and a logic "1" on MOEN2 from the Digital Output Register will cause the signal to enable the interface in drive number 2. When the FDC37C75 is in the Base Mode or the Special Mode, this output is number 2 of the four decoded Unit Selects, as specified in the device command syntax.
24	Motor On 1/ Drive Select 3	MO1/DS3	Output. This is an active low high-current output. When the FDC37C75 is in the PC/AT Mode, a logic "1" on MOEN1 from the Digital Output Register will cause this output to go low, thereby acting as the Motor On Enable for drive number 1. When the FDC37C75 is in the Base Mode or the Special Mode, this output is number 3 of the four decoded Unit Selects, as specified in the device command syntax, thereby acting as drive select 3.
21	Motor On 2/ Drive Select 4	MO2/DS4	Output. This is an active low high-current output. When the FDC37C75 is in the PC/AT Mode, a logic "1" on MOEN2 from the Digital Output Register will cause this output to go low, thereby acting as the Motor On Enable for drive number 2. When the FDC37C75 is in the Base Mode or the Special Mode, this output is number 4 of the four decoded Unit Selects, as specified in the device command syntax, thereby acting as drive select 4.
25	Reduced Write Current/ Revolutions Per Minute	RWC/RPM	Output. This active low signal occurs when tracks greater than 43 are being accessed, and the inner track locations have caused increased bit density. This signal, valid in the Base Mode and the Special Mode, indicates that write precompensation is necessary. In the PC/AT mode, this active low signal may be used to select a 300 RPM spindle rate on two speed drives when 250 Kbps MFM is selected.
12	Write Protected	WP	Input. This active low, Schmitt Trigger input senses from the disk drive that a disk is write protected.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
13	$\overline{\text{Track 00}}$	$\overline{\text{TR00}}$	Input. This active low, Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track, 00.
14	$\overline{\text{Index}}$	$\overline{\text{IDX}}$	Input. This active low, Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track.
9	Precomp-ensation Value	PCVAL	Input. The level on this pin determines the amount of write precompensation to be used on the inner tracks of the diskette. Logic "1" programs the value of 125 ns; Logic "0" programs 187 ns. This input has an internal pull up resistor.
8	Drive Type	DRV	Input. This input is used to indicate the drive type being used. A logic "0" on this input indicates a two speed spindle motor.
IDE DRIVE INTERFACE			
30	Chip Select 0	$\overline{\text{CS1F}}$	Output. Active low chip select to IDE drive $\overline{\text{CS1F}}$ input used by the IDE drive to select the host-accessible Command Block registers. It is decoded from the A0-A9 PC/AT address inputs and is internally qualified by AEN.
29	Chip Select 1	$\overline{\text{CS3F}}$	Output. Active low chip select to IDE drive $\overline{\text{CS3F}}$ input used by the IDE drive to select the host-accessible Control Block Registers. It is decoded from the A0-A9 PC/AT address inputs and is internally qualified by AEN.
31 - 33, 35 - 38	Data Bits DD0-DD6	DD0 - DD6	Data bits DD0 through DD6 to/from the IDE drive.
39	Data Bit DD7	DD7	This signal from the IDE drive is buffered by the FDC37C75. It is connected to AT bus data I/O pin D7 when data transfer is to or from the IDE drive except when the FDC37C75 register 3F7H is being read. During register 3F7 reads, AT bus bit D7 will be sourced by register 3F7 (Digital Input Register) when FADSEL = "1", or will be high impedance when FADSEL = "0".
27	$\overline{\text{Drive Reset}}$	$\overline{\text{DRST}}$	This signal is the inverted and buffered RSTDRV signal from the host AT to the IDE drive.
5	IDE Address Select	IDESEL	This input with internal pull-up resistor is used to select the Primary or Secondary floppy disk controller AT addresses for the IDE drive. When IDESEL = "1", the Primary Addresses are selected. When IDESEL = "0", the Secondary Addresses are selected.
28	$\overline{\text{High Buffer Enable}}$	$\overline{\text{BUFHIEN}}$	This output enables the external 'HCT245 Buffer for the AT upper eight data bits. $\overline{\text{BUFHIEN}}$ is driven active low at either primary address 1F0H or secondary address 170H and internally qualified by AEN.
MISCELLANEOUS			
63	Crystal	XTAL	An external 48 MHz parallel resonant crystal should be connected to these pins for all standard data rates. If an external TTL clock is used, it should be connected to XTAL, and $\overline{\text{XTAL}}$ should be left floating.
62	$\overline{\text{Crystal}}$	$\overline{\text{XTAL}}$	
3	$\overline{\text{Game Port Chip Select}}$	$\overline{\text{GPCS}}$	Active low Game Port Chip Select Output. Decoded from A0-A9 at address 201H, and qualified by AEN.
4	1.8432 MHz Clock Out	ACECLK	1.8432 MHz Clock Output. May be used to provide the clock for a 16450-type UART.
7	Power Good	PWRGD	Input. The FDC37C75 is functional when PWRGD is high. When PWRGD = logic "0", the FDC37C75 is in the low power standby mode.
34, 68	Power Supply	V_{cc}	+ 5 Volt supply pin.
15, 26, 40, 60	Ground	GND	Ground pin.

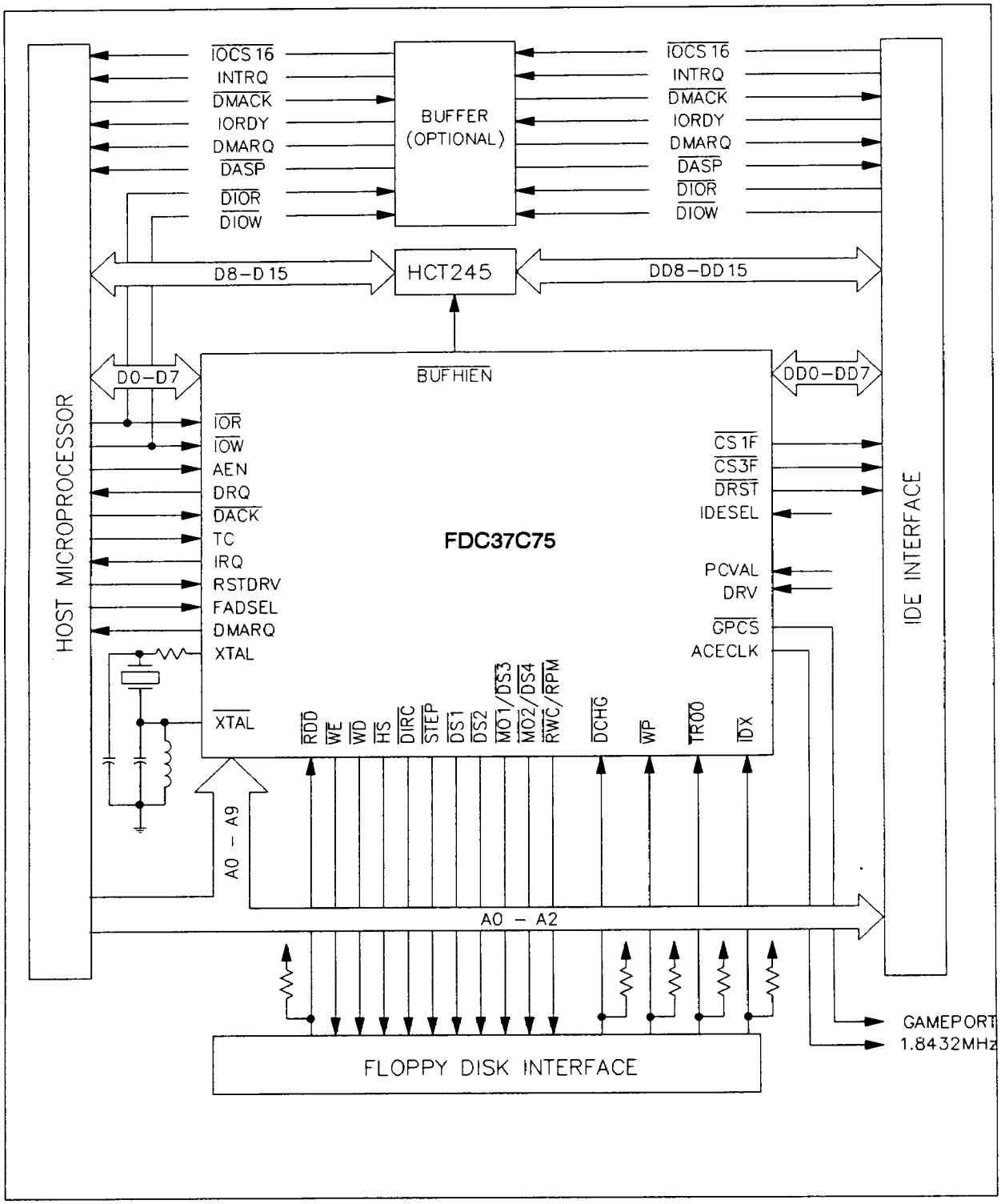


FIGURE 1 - TYPICAL SYSTEM BLOCK DIAGRAM

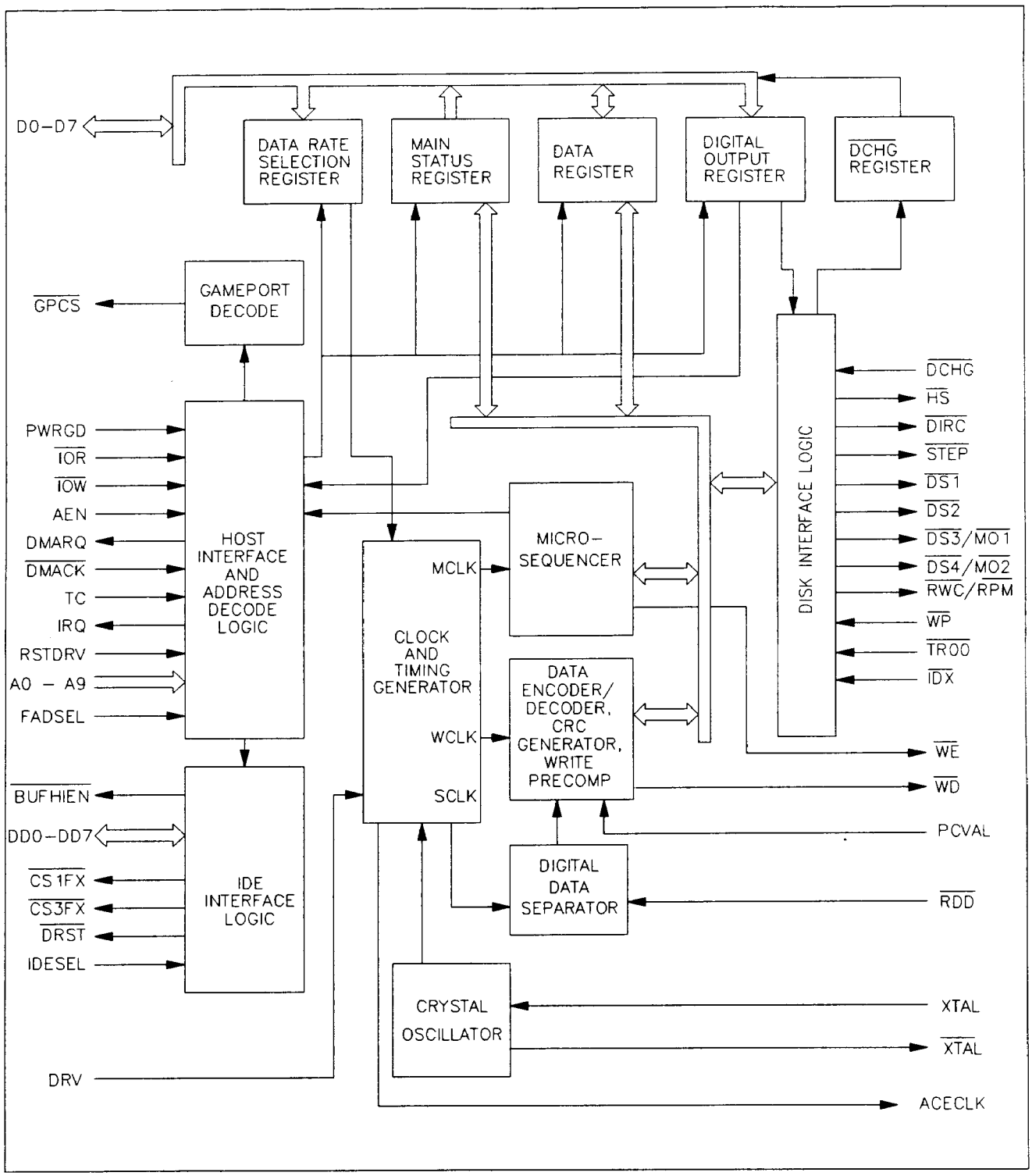


FIGURE 2 - FDC37C75 BLOCK DIAGRAM

SYSTEM DESCRIPTION

The system block diagram in Figure 1 illustrates a complete implementation of the FDC37C75 used in a floppy disk drive system with IDE interface and driver ("paddle chip" function). The FDC37C75 provides simple interfacing to the microprocessor, drive, and IDE connector. This combination of functions allows the simple implementation of an inexpensive "paddle card"/ floppy disk controller, or IDE interface on the motherboard of a PC/AT compatible computer.

MICROPROCESSOR INTERFACE

A typical FDC37C75 interface to the microprocessor consists of an 8-bit data bus, 10-bit address bus, and a control bus. All signals are directly connected to the host, eliminating the need for external circuitry. All FDC37C75 outputs to the host are able to sink 24 mA. The FDC37C75 contains the following internal registers for interfacing to the host microprocessor: Data Rate Selection Register, Main Status Register, Data Register, and Digital Output Register. The Data Rate Selection Register selects the data rate for internal clock generation and synchronization of disk data transfers. The Main Status Register contains information related to the status of the drives and provides handshaking functions for the microprocessor. The Data Register is used in data transfers with the drive during Read and Write operations, and holds the command blocks issued by the microprocessor and the results after the command is executed. The Digital Output Register provides the Motor On and Drive Select signals and the DMA Enable qualifier for the DMARQ and IRQ outputs.

All register addresses as well as the IDE control signals are decoded from the 10 bit address bus.

FLOPPY DISK DRIVE INTERFACE

Figure 1 illustrates a typical FDC37C75 interface to up to four drives. All signals are directly connected to the drives, eliminating the need for external circuitry. All floppy disk drive inputs to the FDC37C75 have Schmitt triggers; all outputs have open-drain, 48 mA drivers. The FDC37C75 provides Data Separation as well as Automatic Write Precompensation. The data separator is based on the Standard Microsystems' FDC92C39 for proven performance. The $\overline{DCHG}$ input may be read through bit D7 of the $\overline{DCHG}$ register (address 3F7H).

IDE INTERFACE

The IDE interface $\overline{CS1F}$ and $\overline{CS3F}$ chip select signals are internally decoded from the host AT address bus. The IDESEL input is used to determine whether the primary or secondary hard disk addresses will be selected.

Data bus signals DD0 - DD7 to and from the IDE interface are internally buffered by the FDC37C75. The $\overline{BUFHIEN}$ output is used to control an external 'HCT245 transceiver for buffering the upper 8 data bits. A hard disk reset signal, $\overline{DRST}$, is buffered from the RSTDRV host AT bus input.

MISCELLANEOUS OUTPUTS

A Game Port Chip Select signal is decoded at address 201H from the address lines A0 - A9. A clock output, ACECLK, of 1.8432 MHz is provided to drive a general purpose UART such as a 16450. See FUNCTIONAL DESCRIPTION for more information on these signals.

FUNCTIONAL DESCRIPTION

Refer to Figure 2 for Internal Block Diagram of the FDC37C75.

HOST INTERFACE LOGIC

The internal registers are used chiefly in writing commands to, and reading status from, the floppy disk control portion of the FDC37C75. In the interfacing of the internal registers to the host, the user must keep in mind a few considerations. During the Command Phase of a command, the Main Status Register must be read before each byte of the command word is written into the data register to ensure that bits D6 and D7 are logic "0" and "1 ", respectively. During the Result Phase of a command, the Main Status Register must be read before each result byte from the data register is read to ensure that bits D6 and D7 are both logic "1 ". The user should ensure that 12 µs elapses before each access of the Main Status Register by the CPU. To avoid waiting 12 µs before each access to the Main Status Register in a Command Phase, the user may save time by polling D6 and D7 of the Main Status Register for the appropriate bit settings. When the correct bit settings appear, the FDC37C75 is ready for commands. No access of the Main Status Register is necessary in the execution phase of a command. During the execution phase, each receipt of a data byte from the drive is indicated by an interrupt signal on the IRQ pin when the FDC37C75 is in the non-DMA mode. The generation of a Read or Write signal clears the interrupt and outputs the data onto the data bus. If the processor cannot respond to the interrupts quickly enough (every 13 µs for MFM and 27 µs for FM), then it may poll the Main Status Register and bit D7 functions as the interrupt signal. If a Write command is in process, then the Write signal performs the reset to the interrupt. The timing parameters mentioned above will double for mini floppy data rates. After an interrupt in the non-DMA Mode, the Main Status Register must be examined to determine the cause, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. In the DMA Mode, no interrupt signals occur during the Execution Phase. Instead, a DMA Request is generated

and the DMA controller responds with a DMA Acknowledge and either a Read or a Write, which clears the DMA Request. After the completion of the Execution Phase or the EOT sector has been read or written, an interrupt will occur, signifying the beginning of the Result Phase. The reading of the first byte of data from the Data Register clears the interrupt.

In PC/AT use, since non-DMA host transfers are not normally used, the FDC37C75 will successfully complete commands but will always give abnormal termination error status, since the TC signal is qualified by the $\overline{DACK}$ signal.

During the Result Phase of a command, all bytes from the Data Register must be read in order to successfully complete the command. The FDC37C75 will not accept a new command until all bytes have been read. The bytes in the Command Phase and the Result Phase must be written and read in the exact order as seen in the Commands section of this document. No shortening of the phases is allowed. The last byte sent to the FDC37C75 in a Command Phase causes the Execution Phase to automatically begin and when the last data byte is read out in the Result Phase, the command is automatically ended, making the FDC37C75 ready for a new command.

INTERNAL REGISTERS

The FDC37C75 contains eight internal registers which facilitate the interfacing between the host microprocessor and the floppy disk drive. The eight registers consist of the Data Rate Selection Register, the Main Status Register, Status Registers 0-3, the Data Register, and the Digital Output Register. Table 1 shows the bit combinations required to access the registers as well as the IDE interface. Combinations other than the ones shown below are illegal.

TABLE 1A: FIXED DISK REGISTER ADDRESSES

PRIMARY ADDRESS[1]	SECONDARY ADDRESS	$\overline{IOR}$	$\overline{IOW}$	$\overline{CS1F}$	$\overline{CS3F}$	FUNCTION[2]
1F0H	170H	X	X	1	0	Read/Write Data; $\overline{BUFHIEN}$ is active low
1F1H	171H	1	0	1	0	Read Error Register
1F1H	171H	0	1	1	0	Write Features Register
1F2H	172H	1	0	1	0	Read Sector Count
1F2H	172H	0	1	1	0	Write Sector Count
1F3H	173H	1	0	1	0	Read Sector Number
1F3H	173H	0	1	1	0	Write Sector Number
1F4H	174H	1	0	1	0	Read Cylinder Low
1F4H	174H	0	1	1	0	Write Cylinder Low
1F5H	175H	1	0	1	0	Read Cylinder High
1F5H	175H	0	1	1	0	Write Cylinder High
1F6H	176H	1	0	1	0	Read Drive/Head
1F6H	176H	0	1	1	0	Write Drive/Head
1F7H	177H	1	0	1	0	Read Status
1F7H	177H	0	1	1	0	Write Command
3F6H	376H	1	0	0	1	Read Alternate Status
3F6H	376H	0	1	0	1	Write Device Control
3F7H	377H	1	0	0	1	Read Drive Address (bits D6 - D0)[3]
3F7H	377H	0	1	0	1	Not used

Notes: (1) Primary Addresses selected when IDESEL = "1"; Secondary Address selected when IDESEL = "0".
(2) Register functions are shown for reference only.
(3) Address 3F7H/377H is shared with the floppy disk controller in the read mode. Bits D6 - D0 contain Fixed Disk Drive Address information. Bit D7 contains the contents of the 1-bit Floppy Disk $\overline{DCHG}$ register.

TABLE 1B: FLOPPY DISK REGISTER ADDRESSES

PRIMARY ADDRESS[1]	SECONDARY ADDRESS	$\overline{IOR}$	$\overline{IOW}$	$\overline{CS1F}$	$\overline{CS3F}$	FUNCTION
3F2H	372H	1	0	0	0	Not used
3F2H	372H	0	1	0	0	Write Digital Output Register
3F3H	373H	1	0	0	0	Not used
3F3H	373H	0	1	0	0	Not used
3F4H	374H	1	0	0	0	Read Main Status Register
3F4H	374H	0	1	0	0	Write Main Status Register[2]
3F5H	375H	1	0	0	0	Read Data Register
3F5H	375H	0	1	0	0	Write Data Register
3F6H	376H	1	0	0	0	Not used
3F6H	376H	0	1	0	0	Not used
3F7H	377H	1	0	0	0	Read $\overline{DCHG}$ Register[3]
3F7H	377H	0	1	0	0	Write Data Rate Selection Register

Notes: (1) Primary Addresses selected when FADSEL = "1"; Secondary Address selected when FADSEL = "0".
(2) Valid for D0 = 1 only; this enters the soft power-down mode of the floppy disk control portion of the FDC37C75. See "Low Power Modes".
(3) Address 3F7H/377H is shared with the Fixed Disk Register space in the read mode. Bits D6 - D0 contain Fixed Disk Drive Address information. Bit D7 contains the contents of the 1-bit Floppy Disk $\overline{DCHG}$ register.

Data Rate Selection Register

The Data Rate Selection Register provides support logic that latches the two LSB's of the data bus upon receiving address 3F7H/377H. These data bits are used to select the desired data rate which, in turn, controls the internal clock generation. When the data rate is switched, the clock is de-glitched to allow for continuous operation. Refer to Table 2 for proper programming of the Data Rate Selection Register.

Table 2 - Data Rate Selection Register (3F7H/377H)

DB1	DB0	DRV	Encoding Scheme	Data Rate (kbits/s)	RPM (in PC/AT/ EISA Mode)
0	0	X	MFM	500	1
0	0	X	FM	250	1
0	1	0	MFM	250	0
0	1	1	MFM	300	0
1	0	X	MFM, RST Default	250	1
1	0	X	FM, RST Default	125	1
1	1	X	FM	125	0

The Data Rate Selection Register also provides the means of disabling Write Precompensaton. Write Precompensation may be disabled in the PC/AT/EISA mode by writing a logic high to bit 2 of the Control Register. Please note that a hardware reset will reset bit 2 to a logic low, re-enabling Write Precompensation.

DB2	Function
0	Write Precompensation Enabled
1	Write Precompensation Disabled

Main Status Register

The Main Status Register is an 8-bit register that contains the status information of the FDC37C75, and may be accessed at any time. Only the Main Status Register may be accessed to facilitate the transfer of data between the microprocessor and the FDC37C75. That is, Status Registers 0-3 may be read only after the completion of a command and provide no assistance in the transfer of data between the microprocessor and the FDC37C75. Each time the Main Status Register is accessed, the microprocessor should wait 12 µs if 500 kbits/sec MFM is selected as the data rate, and 24 µs if 250 kbits/sec MFM is selected. Refer to Table 3 for the contents of the Main Status Register.

Table 3 - Main Status Register (3F4H/374H)

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	FDD 0 Busy	D0B	A high level on this bit indicates that drive 0 is in the Seek Mode and that the FDC37C75 will not accept READ or WRITE commands. *
1	FDD 1 Busy	D1B	A high level on this bit indicates that drive 1 is in the Seek Mode and that the FDC37C75 will not accept READ or WRITE commands.
2	FDD 2 Busy	D2B	A high level on this bit indicates that drive 2 is in the Seek Mode and that the FDC37C75 will not accept READ or WRITE commands.
3	FDD 3 Busy	D3B	A high level on this bit indicates that drive 3 is in the Seek Mode and that the FDC37C75 will not accept READ or WRITE commands.
4	FDC Busy	CB	A high level on this bit indicates that a READ or WRITE command is in progress and that the FDC37C75 will not accept any other command.
5	Execution Mode	EXM	A high level on this bit indicates that the FDC37C75 is in the Execution Phase in Non-DMA Mode. When this bit goes low, the Execution Phase has ended and the Results Phase has begun. This bit operates only in the Non-DMA Mode.
6	Data	DIO	A high level on this bit indicates that the direction of data transfer is from the Data Register to the microprocessor. A low level on this bit indicates that the direction of data transfer is from the microprocessor to the Data Register.
7	Request	RQM	A high level on this bit indicates that the Data Register is ready to send or receive data to or from the microprocessor. Both the DIO and the RQM bits should be used to perform the "ready" and "direction" hand-shaking functions to the host.

* Note: A write to the Main Status Register of X1H (D0 = 1), will place the floppy disk control portion of the FDC37C75 in the Soft Power-Down Mode.

Status Registers 0-3

Status Registers 0-3 are each 8 bit registers that contain status information on the FDC37C75 and are available only in the Result Phase and may be read only after completing a command. The command that has been executed determines which of the Status Registers will be read. Refer to Tables 4-7 for the contents of Status Registers 0-3.

Table 4 - Status Register 0

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Unit Select 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.
1	Unit Select 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
2	Head Select	HS	This flag is used to indicate the state of the head at interrupt.
3	Not Ready	NR	This bit will always be a logic "0", since Drive Ready is always presumed to be true.
4	Equipment Check	EC	A high level on this bit indicates that the Track 0 signal has failed to occur after 77 step pulses (Recalibrate Command).
5	Seek End	SE	A high level on this bit indicates that the FDC37C75 has completed the seek command.
6,7	Interrupt Code	IC	The four combinations of these bits indicate four different situations: 7 6 0 0 Normal Termination of command was completed and properly executed. 0 1 Abnormal Termination (AT) of command. Execution of command was started but not successfully completed. 1 0 Invalid Command (IC) issue. Command which was issued was never started. 1 1 Abnormal Termination (AT) of command. During execution of command, the ready signal from drive changed state.

Table 5 - Status Register 1

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Missing Address Mark	MA	A high level on his bit indicates that the FDC37C75 cannot detect the Data Address Mark or the Deleted Data Address Mark. In this case, the MD bit of Status Register 2 is also set to a logic "1".
1	Not Writable	NW	A high level on this bit indicates that, during execution of the WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK Command, the FDC37C75 has detected a $\overline{WP}$ signal from the drive, indicating that the diskette is write protected.
2	No Data	ND	A high level on this bit indicates one of three conditions. Either 1) during the execution of the READ DATA, or FORMAT A TRACK Command,the FDC37C75 cannot find the sector specified in the Internal Data Register, or 2) during the execution of the READ ID Command, the FDC37C75 cannot read the ID field without an error, or 3) during the execution of the READ A CYLINDER Command, the starting sector cannot be found.
3	(not used)		This bit is not used and is always at a logic "0".
4	Overrun)	OR	A high level on this bit indicates that the FDC37C75 has not been serviced by the microprocessor during data transfers within a certain time interval.
5	Data Error	DE	A high level on this bit indicates that the FDC37C75 has detected a Cyclic Redundancy Check Error in either the ID field or the data field.
6	(not used)		This bit is not used and is always at a logic "0".
7	End of Cylinder	EN	A high level on this bit indicates that the FDC37C75 has tried to access a sector beyond the final sector of a cylinder.

Table 6 - Status Register 2

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Missing Address Mark in Data Field	MD	A high level on this bit indicates that the FDC37C75, upon reading data from the drive, cannot find a Data Address Mark, or Deleted Data Address Mark.
1	Bad Cylinder	BC	A high level on this bit indicates that the contents of the cylinder on the medium is different from that stored in the Internal Data Register and the contents of the cylinder is FFH. This bit is related to the ND (No Data) bit of Status Register 1.
2	Scan Not Satisfied	SN	A high level on this bit indicates that, during the execution of a SCAN Command, the FDC37C75 cannot find a sector on the cylinder which meets the specified condition.
3	Scan Equal Hit	SH	A high level on this bit indicates that, during the execution of a SCAN command, the condition of "equal" has been satisfied.
4	Wrong Cylinder	WC	A high level on this bit indicates that the contents of the cylinder on the medium is different from that stored in the Internal Data Register. This bit is related to the ND (No Data) bit of Status Register 1.
5	Data Error	DE	A high level on this bit indicates that the FDC37C75 has detected a Cyclic Redundancy Check Error in the data field.
6	Control Mark	CM	A high level on this bit indicates that, during the execution of the READ DATA or SCAN Command, the FDC37C75 has encountered a sector which contains a Deleted Data Address Mark.
7	(not used)		This bit is not used and is always at a logic "0".

Table 7 - Status Register 3

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Unit Select 0	US0	This bit is used to indicate the status of the Unit Select 0 signal to the drive.
1	Unit Select 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the drive.
2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the drive.
3	Two Side	TS	This bit is used to indicate the status of the Two-Side signal to the drive.
4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal to the drive.
5	Ready	RY	This bit is used to indicate the status of the Ready signal from the drive. This bit is always at a logic "1".
6	$\overline{\text{Write Protected}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the drive.
7	Fault	FT	This bit is used to indicate the status of the Fault signal from the drive.

Data Register (3F5H/375H)

The Data register is an 8-bit register which stores data, commands, parameters, and drive status information. Data is read from or written to the Data Register in order to program or obtain results of a command that has been issued.

Digital Output Register (3F2H/372H)

The Digital Output Register provides for selection of the disk drive and control of the disk drive spindle motors. These selections are typically implemented with the standard latched port found in floppy disk subsystems. The Digital Output Register provides support logic that latches the data bus upon receiving address 3F2H/372H. Refer to Table 8 for the contents of the Digital Output Register.

Table 8 - Digital Output Register

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Drive Select	DSEL	A low level on this bit, when MOEN 1 is a logic "1", activates a $\overline{DS1}$ ($\overline{Drive\ Select\ 1}$ output pin). A high level on this bit, when MOEN2 is a logic "1" activates $\overline{DS2}$ ($\overline{Drive\ Select\ 2}$ output pin). This bit only activates $\overline{DS1}$ or $\overline{DS2}$ when the FDC37C75 is in PC/AT/EISA Mode.
1	$\overline{Drive\ Select\ Enable}$	$\overline{DSELEN}$	A low level on this bit enables $\overline{DS1}$ and $\overline{DS2}$ to become active.
2	$\overline{Soft\ Reset}$	$\overline{SRST}$	A low level on this bit provides for soft reset of the FDC37C75.
3	DMA Enable	DMAEN	This bit, active in Special Mode and PC/AT/EISA Mode, qualifies the DMARQ and IRQ outputs and the $\overline{DACK}$ input.
4	Motor 1 On Enable	MOEN1	The MO1 signal is the inverted output of this signal, which is active only in the PC/AT/EISA Mode.
5	Motor 2 On Enable	MOEN2	The MO2 signal is the inverted output of this signal, which is active only in the PC/AT/EISA Mode.
6	(not used)		This bit is not used.
7	Mode Select	MSEL	During a software reset, a low level on this bit selects PC/AT/EISA Mode while a high level selects Special Mode.

MODES OF OPERATION

The FDC37C75 may operate under three different modes. They are the Base, Special, and PC/AT/EISA Modes. Table 9 illustrates the features of each mode of operation. The Data Rate Selection Register is used in any of the three modes without a change in its functionality. Figure 3 illustrates the block diagram of all the possible entries within the three operation modes.

Base Mode

After a hardware reset, Base Mode may be entered by a microprocessor access to the FDC37C75. The recommended access is a read of the Main Status Register. When a hardware reset occurs, the FDC37C75 is held in a soft reset, with the DMA and IRQ outputs tri-stated. When the Base Mode is entered, the DMARQ and IRQ signals resume their normal driving conditions. The $\overline{Drive\ Select}$ ($\overline{DS1}$ - $\overline{DS4}$) outputs, which provide for a 1 out of 4 decoding of the Unit Select bits of the command structure, may be used in the Base Mode. Please note that the Digital Output Register may not be used during Base Mode. There is, consequently, no qualifying by DMAEN and no Soft Reset. The Reduced Write Current (RWC) output, which indicates the necessity of write precompensation, may be used in the Base Mode.

PC/AT/EISA Mode

When the FDC37C75 is being used in a PC/AT/EISA or compatible system environment, the PC/AT Mode is required.

In the PC/AT/EISA Mode, the $\overline{Drive\ Select}$ ($\overline{DS1}$-$\overline{DS4}$) outputs are replaced with the DSEL, MOEN1 , and MOEN2 signals from the Digital Output Register. The DMAEN signal from the Digital Output Register may be used as a qualifier for the DMARQ and IRQ outputs, and the $\overline{SRST}$ signal may be used to do a software driven reset. The $\overline{Reduced\ Write\ Current}$ ($\overline{RWC}$) output now performs the function of $\overline{Revolutions\ Per\ Minute}$ ($\overline{RPM}$). Users with two speed drives may reduce spindle speed from a nominal 360 RPM to 300 RPM when this signal is active low. Similarly, this signal may be used to reduce write current when a slower data rate is selected for a given drive. In order to enter the PC/AT/EISA Mode from the Base Mode, the user will perform a write to the Digital Output Register (3F2H/372H). The data written may be anything except an 80H, because a logic "1" in Bit 7 of the Digital Output Register is used to select Special Mode.

In order to enter the PC/AT Mode from the Special Mode, the user will write 00H to the Digital Output Register. That is,

Bit 0: X (Don't care)
Bit 1: X (Don't care)
Bit 2: 0 (A low level on $\overline{SRST}$ causes a soft reset)
Bit 3: X (Don't care)
Bit 4: 0 (Disable Motor On Enable 1)
Bit 5: 0 (Disable Motor On Enable 2)
Bit 6: X (Don't care)
Bit 7: 0 (A low level on MSEL selects PC/AT/EISA Mode)

To complete the entry into the PC/AT/EISA Mode from the Special Mode, the user will then read the Data Rate Selection Register address (3F7H/377H).

Special Mode

In the Special Mode, the Drive Select (DS1 - DS4) outputs, which provide for a 1 out of 4 decoding of the Unit Select bits of the command structure, may be used. The DMAEN signal from the Digital Output Register may be used as a qualifier for the DMA and IRQ outputs and the $\overline{DACK}$ input. The SRST bit may be used to do a software driven reset. The Reduced Write Current ($\overline{RWC}$) output, which indicates the necessity of write precompensation, may also be used in the Special Mode.

The Special Mode may only be entered from the Base Mode. In order to enter the Special Mode, the user will write 8OH into the Digital Output Register (3F2H/372H) because a logic "1" in Bit 7 of the Digital Output Register selects Special Mode. That is,

Bit 0: X (Don't care)
Bit 1: X (Don't care)
Bit 2: 0 (A low level on $\overline{SRST}$ causes a soft reset)
Bit 3: X (Don't care)
Bit 4: 0 (Disable Motor On Enable 1)
Bit 5: 0 (Disable Motor On Enable 2)
Bit 6: X (Don't care)
Bit 7: 0 (A high level on MSEL selects Special Mode)

To complete the entry into the Special Mode, the user will then read the Data Rate Selection Register address (3F7H/377H).

Table 9 - Modes of Operation

FEATURES	BASE MODE	PC/AT/EISA MODE	SPECIAL MODE
Functions of DSEL1-4	DSEL1-4	DSEL1-2, MOEN1-2	DSEL1-4
Software Reset supported	No	Yes	Yes
DMA pin supported by DMAEN bit	No	Yes	Yes
IRQ pin qualified by DMAEN bit	No	Yes	Yes
Functions of $\overline{RPM}/\overline{RWC}$	$\overline{RWC}$	$\overline{RPM}$	$\overline{RWC}$

Power Down Mode

The FDC37C75 may be placed into the Low Power Standby Mode by driving the PWRGD pin low. In this mode, the entire chip is in standby; all inputs are ignored, all outputs are in the high impedance state, the oscillator is stopped, and the low V_{cc} detect circuit is stopped. All register contents are preserved. The Low Power Standby Mode is exited by a hard reset (RSTDRV = 1) after PWRGD is brought high.

Just the floppy disk controller portion of the FDC37C75 may be placed in the "Soft Power-down" mode by writing a X1H (D0 = 1) to the Main Status Register (3F4H/374H). The Floppy Disk Soft Power-down is exited by a hard reset (RSTDRV = 1).

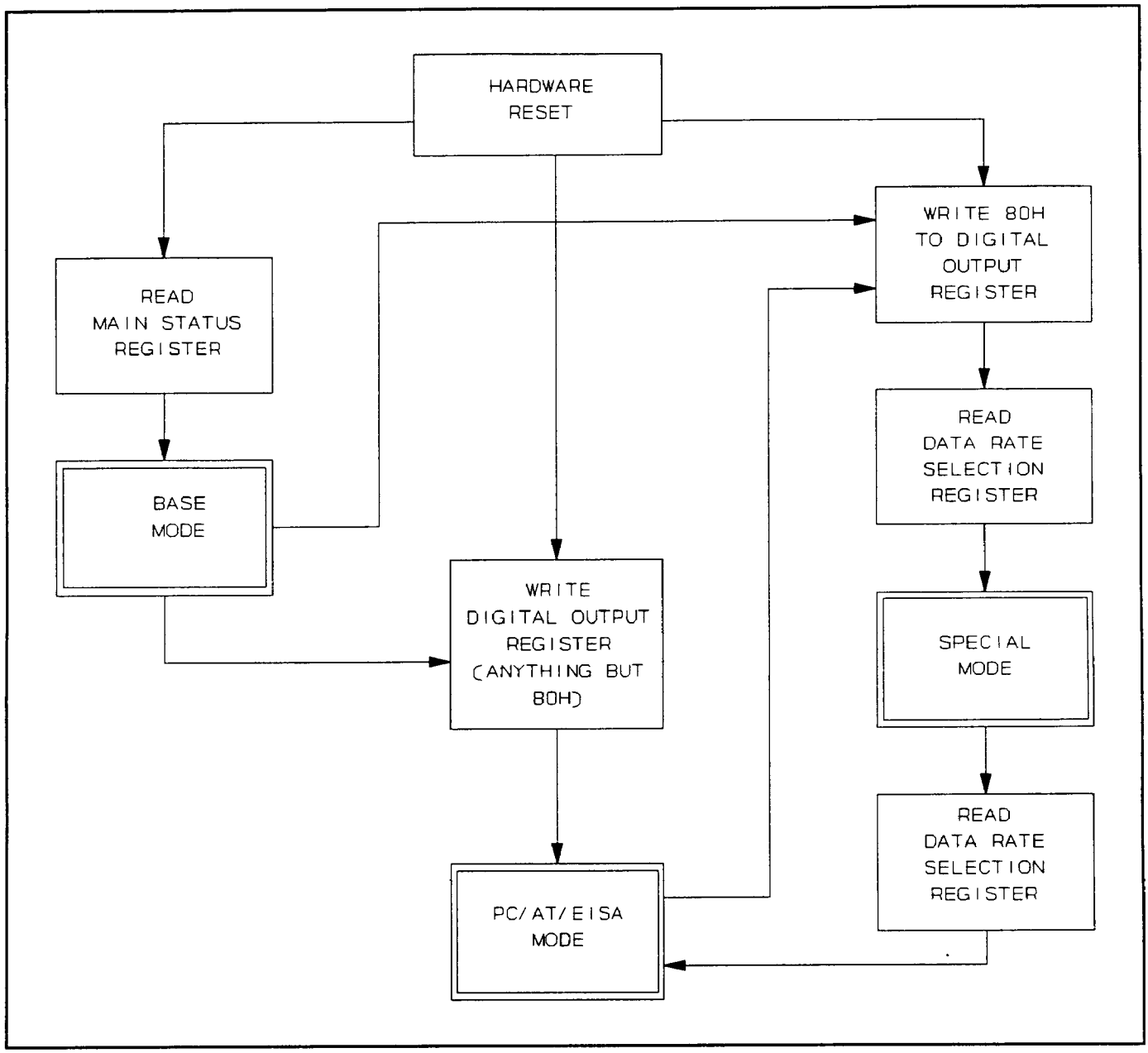


FIGURE 3 - POSSIBLE MODE ENTRIES

POLLING ROUTINE

Following either a hard or soft reset, the FDC37C75 automatically begins polling the drives for a change in the Ready lines. The polling is done continuously between commands and between step pulses in the SEEK command. The purpose of the polling routine is to detect when the drives return to a Ready status after being reset or after a command is completed. The polling sequence is Drive 1, 2, 3, 4, and each drive is polled every 1.024 ms, except during the READ/WRITE commands. For minifloppies, the polling rate is 2.048 ms. In Special or PC/AT Modes, if DMAEN is not valid by 1 ms after reset becomes inactive, then IRQ may already be set and pending when enabled onto the bus. When the FDC37C75 is in the PC/AT Mode, the user will not see the polling at the Drive Select signals. Refer to Figure 4 for the general timing of the Drive Select Polling.

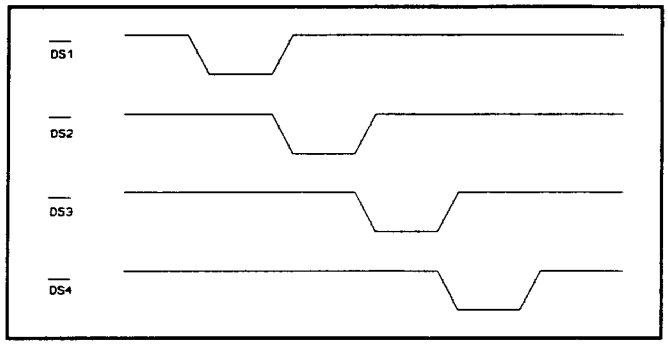


FIGURE 4 - DRIVE SELECT POLLING TIMING

RESET LOGIC

A hardware reset is performed by applying a logic "1" to the RSTDRV pin of the FDC37C75. When a hardware reset occurs, the device will remain in the reset condition for the duration of the pulse. Once the pulse is removed, the FDC37C75 will default to Base Mode with a data rate of 250 kbits/s MFM (or 125 kbits/s FM, code dependent) when a 16 MHz input clock is used. The FDC37C75 will default to 500 kbits/s MFM when a 32 MHz input clock is used. A software reset is performed by applying a logic "0" to bit 2 of the Digital Output Register. When a software reset occurs, the FDC37C75 is reset the same as it is during a hardware reset, with the exception that the mode and the data rate are not affected. During a reset, the high current driver outputs to the drives are disabled. Neither a hard reset nor a soft reset will affect the values of the internal timers, that is, Head Unload Time, Head Load Time, and Step Rate Time (described in the COMMANDS section of this document). If the on chip crystal oscillators are used instead of the TTL clock inputs, a longer duration of the pulse on the RST pin during a hardware reset is required to stabilize the internal timing.

The FDC37C75 contains internal circuitry to automatically reset the device during initial power-up. The device also contains power fail protection circuitry in the disk interface which allows it to reset itself in the event of power failure.

DATA SEPARATOR AND WRITE PRECOMPENSATION

The Data Separator portion of the FDC37C75 is based on the Standard Microsystems FDC92C39. It performs the complete data separation function of separating the data and clock pulses from the FM and MFM encoded data. In addition, it contains the Automatic Write Precompensation Logic necessary when writing to the inner and outer tracks of the drive. The encoded Write Data signal is synchronized to the input clock and is clocked through an internal shift register, but is delayed upon being output. When a logic "0" is applied to the PCVAL pin and a track inside of track 43 is accessed, data will be precompensated by ±187 ns. For MFM encoding, when a logic "1" is applied to the PCVAL Pin, data will be precompensated by ±125 ns, regardless of track number and data rate. For frequencies other than 16 MHz on the CLK1 pin, the precompensation value will be three clock cycles for PCVAL="0", or two clock cycles for PCVAL="1". When CLK2 is used for nonstandard data rates, the precompensation value is always two clock cycles, thus disabling the function of PCVAL. Note that FM encoding is not precompensated. Precompensation may be disabled by writing a logic high to bit D2 of the Data Rate Selection Register.

CLOCK GENERATION

The FDC37C75 generates the three required internal clocks from the crystal oscillator. The three internal clocks include the Master Clock (MCLK), Sampling Clock (SCLK), and Write Clock (WCLK). The MCLK is used by the microsequencer to clock the latches in a two-phase scheme. One microinstruction cycle consists of four MCLK cycles. The frequency of MCLK is 8 times the selected MFM data rate or 16 times the FM data rate. SCLK is used in the internal data separator for data recovery. The frequency of SCLK is 32 times the selected data rate. WCLK is used in MFM or FM encoding when writing data to the disk. WCLK has a frequency of twice the selected data rate. Refer to Table 10 for the frequencies of the internal clocks and their relationship to the selected data rates and codes.

Table 10 - Internal Clock Frequencies

Data Rate (bits/s)	Code	MCLK (MHz)	SCLK (MHz)	WCLK (kHz)
500k	MFM	4.0	16.0	1000
250k	FM	4.0	8.0	500
250k	MFM	2.0	8.0	500
125k	FM	2.0	4.0	250
300k	MFM	2.4	9.6	600

IDE INTERFACE

The IDE interface $\overline{CS1F}$ and $\overline{CS3F}$ chip select signals are internally decoded from the host AT address bus bits A0 - A9. The IDESEL input is used to determine whether the primary or secondary hard disk addresses will be selected.

Data bus signals DD0 - DD7 to and from the IDE interface are internally buffered by the FDC37C75. The $\overline{\text{BUFHIEN}}$ output is used to control an external 'HCT245 transceiver for buffering the upper 8 data bits. The $\overline{\text{BUFHIEN}}$ is active low at address 1F0H/170H, and is internally gated with AEN. A fixed disk reset signal, $\overline{\text{DRST}}$, is inverted and buffered from the RSTDRV host AT bus input.

To avoid conflict with the Floppy Disk Read $\overline{\text{DCHG}}$ register, only bits DD0 - DD6 contain IDE interface information when reading the Drive Address Register (3F7H/377H). When register address 3F7H is selected for reading, bit D7 will either reflect the state of the $\overline{\text{DCHG}}$ pin (FADSEL = "1") or be high impedance (FADSEL = "0").

All IDE interface signals not buffered or decoded by the FDC37C75 may be directly connected to the host AT bus, or, if desired, buffered with an optional 'LS240.

GAME PORT CHIP SELECT

An active-low chip select output is internally decoded at address 201H. It is internally qualified by AEN.

UART CLOCK OUTPUT

A 1.8432 MHz clock output, ACECLK, is provided for use with an external UART such as the 16450 or similar UART.

COMMAND SEQUENCE

The FDC37C75 is capable of performing 18 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC37C75 and the processor, it is convenient to consider each command as consisting of three phases :

Command Phase: The FDC37C75 receives all information required to perform a particular operation from the processor.

Execution Phase : The FDC37C75 performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor.

Table 11 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of the Main Status Register (A_0 = 0) or the Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7 - D_0	Data Bus	8-bit Data bus; D_7 is the most significant bit, and D_0 is the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT is the final Sector number on a Cylinder. During Read or Write operation the FDC37C75 will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands, this value determines the number of bytes that VCO's will stay low after two CRC bytes. During Format command GPL determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in the ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDC37C75 (2 to 254 ms in 2 ms increments).

Table 11 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0, the FDC37C75 will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R is the Sector number which will be read or written.
R/W	Read/Write	R/W is the Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT is the Stepping Rate for the FDC37C75. The stepping rate applies to all drives. The stepping rate is programmable from 1 to 16 ms in 1 ms increments. F_H = 1 ms, E_H = 2 ms, etc.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-ST3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive (0 or 1).

INSTRUCTION SET

Table 12 lists the required parameters and the results associated with each command that the FDC37C75 is capable of performing. Refer to Table 11 for explanations of the various symbols used.

TABLE 12 - INSTRUCTION SET [1 2 3]

READ DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

[1] Symbols used in this table are described in the beginning of this section

[2] A_0 should equal binary 1 for all operations.

[3] X = Don't care, usually made to equal binary 0.

READ DELETED DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ ID									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Seector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								

FORMAT A TRACK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								

SCAN EQUAL										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

RECALIBRATE									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0.

SENSE INTERRUPT STATUS									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
	W									
RESULT	W	STO								FDC status information at the end of seek-operation.
	W	PCN								

SPECIFY

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

SENSE DRIVE STATUS

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
RESULT	W	ST3								Status information about FDD

SEEK

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution	W	ST0								Head positioned over proper cylinder on diskette

INVALID CODES

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	Invalid Codes								Invalid Command Codes (NoOp - FDC goes into Stand-by State)
Result	R	ST0								ST0 = 80_H

SOFTWARE RESET

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND Execution	W	0	0	1	1	0	1	1	0	Command Codes Same as hardware reset

RETURN VERSION

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
COMMAND	W	X	X	X	1	0	0	0	0	Command Codes
Result	R	1	0	0	*1	0	0	0	0	*Indicates B-type product

Read Data

A set of nine (9) byte words are required to place the floppy disk control section of the FDC37C75 into the Read Data Mode. After the Read Data command has been issued, the FDC37C75 loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC37C75 outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of this signal, the FDC37C75 stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then, at the end of the sector, terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC37C75 depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 13 shows the Transfer Capacity.

TABLE 13 - TRANSFER CAPACITY

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) X (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) x (26) = 3,328	26 at Side 0
0	1	01	(256) x (26) = 6,656	or 26 at Side 1
1	0	00	(128) x (52) = 6,656	26 at Side 1
1	1	01	(256) x (52) = 13,312	
0	0	01	(256) x (15) = 3,840	15 at Side 0
0	1	02	(512) x (15) = 7,680	or 15 at Side 1
1	0	01	(256) x (30) = 7,680	15 at Side 1
1	1	02	(512) x (30) = 15,360	
0	0	02	(512) x (8) = 4,096	8 at Side 0
0	1	03	(1024) x (8) = 8,192	or 8 at Side 1
1	0	02	(512) x (16) = 8,192	8 at Side 1
1	1	03	(1024) x (16) = 16,384	

The "multi-track" function (MT) allows the FDC37C75 to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector L, Side 0 and completing at Sector L, Side 1 (Sector L is the last sector on the side). Please note that this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC37C75 must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC37C75 reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexadecimal.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC37C75 detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC37C75 sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

After reading the ID and Data Fields in each sector, the FDC37C75 checks the CRC bytes. If a read error is

detected (incorrect CRC in ID field), the FDC37C75 sets the DC (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC37C75 also sets the DD (Data Error in Data field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

If the FDC37C75 reads a Deleted Data Address Mark from the diskette, and the SK bit (bit D5 in the first Command Word is not set (SK = 0) then the FDC37C75 sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC37C75 skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC37C75 and the processor, via the data bus, the FDC37C75 must be serviced by the processor every 27 µs in the FM Mode, and every 13 µs in the MFM Mode, or the FDC37C75 sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 14 shows the value for C, H, R, and N, when the processor terminates the Command.

Table 14 - ID Information in Processor - Terminated Command

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC37C75 into the Write Data mode. After the Write Data command has been issued, the FDC37C75 loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the specify command), and begins reading ID Fields. When all four bytes loaded during the Command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC37C75 takes data from the processor byte-by-byte via the data bus, and outputs it to the drive.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written. The FDC37C75 continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC37C75, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with 00 (zeros).

The FDC37C75 reads the ID field of each sector and checks the CRC bytes. If the FDC37C75 detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

The Write Command operates in much the same manner as the Read Command. The following items are the

same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 µs in the FM mode, and every 13 µs in the MFM mode. If the time interval between data transfers is longer than this, the FDC37C75 sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. Status register 0 also has bit 7 and 6 set to 0 and 1 respectively.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC37C75 detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, the FDC37C75 skips the sector with the Data Address Mark and reads the next sector.

Read a Track

This command is similar to the READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC37C75 starts reading all data fields on the track, as continuous blocks of data. If the FDC37C75 finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC37C75 compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC37C75 does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC37C75 stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette before the INDEX HOLE is encountered for the second time, the MA (Missing Address Mark) flag in Status Register 1 is set to a "1" (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a "1" (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to "0" and "1" respectively. During this command there is no data transfer between FDC37C75 and the CPU except during the result phase.

Format a Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette. Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/ cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; four data requests per sector are made by the FDC37C75 for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC37C75 for each sector on the track. If the FDC37C75 is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register are incremented by one after each sector is formatted. The R register therefore contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC37C75 encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the drive at the end of a write operation, then the FDC37C75 sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also, the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 15 shows the relationship between N, SC, GPL for various sector sizes. (See Table 16 for recommended IBM PC and PC/AT compatible programming parameters.)

Table 15

Format	Sector Size	N	SC	GPL[1]	GPL[2][3]
8" Standard Floppy					
FM Mode	128 Bytes/Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode [4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 Bytes/Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode [4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	09	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½ Sony Micro Floppydisk®					
FM Mode	128 Bytes/Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes: (1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
(2) Suggested values of GPL in format command.
(3) All values except sector size and hexadecimal.
(4) In MFM mode FDC37C75 cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00)

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC37C75 compares the data on a byte-by-byte basis, and looks

for a sector of data which meets the conditions of:

$$D_{FDD} = D_{PROCESSOR}, D_{FDD} \leq D_{PROCESSOR}, \text{ or}$$

$$D_{FDD} \geq D_{PROCESSOR}$$

The hexadecimal byte of FF either from memory or from the drive can be used as a mask byte because it always meets the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur:

1. The conditions for scan are met (equal, low, or high), or,
2. The last sector on the track is reached (EOT), or
3. The terminal count signal is received.

If the conditions for scan are met, then the FDC37C75 sets the SH (Scan Hit) flag of Status Register 2 to a "1" (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC37C75 sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC37C75 to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 16 shows the status of bits SH and SN under various conditions of SCAN.

Table 16

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 (SN)	BIT 3 (SH)	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

If the FDC37C75 encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC37C75 skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC37C75 sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read, or the MT (Multi-Track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21, the following will happen: Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped, and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 µs (FM Mode) or 13 µs (MFM Mode). If an Overrun occurs the FDC37C75 ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the drive is moved from cylinder to cylinder under control of the Seek Command. FDC37C75 has four independent Present Cylinder Registers for each drive. They are clear only after the Recalibrate command. The FDC37C75 compares the PCN (Present Cylinder Number), which is the current head position, with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN:	Direction signal to drive set to a 1 (high),and Step Pulses are issued (Step In).
PCN > NCN:	Direction signal to drive set to a 0 (low), and Step Pulses are issued (Step Out).

The rate at which Step Pulses are issued is controlled by the SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued, NCN is compared against PCN; when NCN = PCN, the SE (Seek End) flag in Status Register 0 is set to a 1 (high), and the command is terminated. At this point the FDC37C75 interrupt goes high. Bits DB0 - DB3 in the Main Status Register are set during the seek operation and are cleared by the Sense Interrupt Status Command.

During the Command Phase of the Seek operation, the FDC37C75 is in the FDC37C75 BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC37C75 is in the NON BUSY state, another seek Command may be issued, and in this manner parallel Seek Operations may be performed on up to 4 Drives at once. No other command can be issued for as long as the FDC37C75 is in process of sending Step Pulses to any drive.

If a drive is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 µs, the timing between the first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the drive to the Track 0 position. The FDC37C75 clears the contents of the PCN counter, and checks the status of the Track 0 signal from the drive. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC37C75 sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1's (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

For IBM compatibility, two RECALIBRATE Commands must be issued for disks with more than 77 tracks.

The ability to overlap RECALIBRATE Commands to multiple drives and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal will be generated by the FDC37C75 for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of drive changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in the NON-DMA Mode, DB5 in the Main Status Register is high. Upon entering the Result Phase this bit is cleared. Reasons 1 and 4 do not require a Sense Interrupt Status command. The interrupt is cleared by reading or writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register, 0 identifies the cause of the interrupt. See Table 17.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Issuing the Sense Interrupt Status Command without an interrupt pending is treated as an invalid command.

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time)

Table 17

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms, ... 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between the Head Load signal going high and the Read/Write operation starting. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,... 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (XTAL). Times indicated above are for a 48 MHz clock; if the clock is reduced to 32 MHz then the time intervals are increased by a factor of two.

The choice of DMA or non-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1), the non-DMA mode is selected, and when ND = 0, the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the drives. Status Register 3 contains the Drive Status information stored internally in the FDC37C75 registers.

Invalid

If an invalid command is sent to the FDC37C75 (a command not defined above), then the FDC37C75 will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC37C75 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC37C75 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0, it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC37C75 will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC37C75 in a standby or no operation state.

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP 4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP
80x	12x			50x	12x			Y	D	E	O	R	22x	12x				R		4b
4E	00	3x C2	FC	4E	00	3x A1	FE	L		C		C	00	00	3x A1	FB F8		C		

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	C	H	S	N	C	GAP2	SYNC	DATA AM	DATA	C	GAP3	GAP
40x	6x		26x	6x		Y	D	E	O	R	11x	6x			R		4b
FF	00	FC	FF	00	FE	L		C		C	FF	00	FB or F8		C		

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C
Positive Voltage on any pin, with respect to Ground . . . . . V_{cc} +0.3V
Negative Voltage on any pin, with respect to Ground . . . . . -0.3V
Maximum V_{cc} . . . . . +7V

* Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +5.0 V ± 10%)

PRELIMINARY
Not a final specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Low Input Voltage 1	V_{IL1}			0.8	V	TTL Level Inputs: All inputs except Floppy Disk Interface as noted below
High Input Voltage 1	V_{IH1}	2.0			V	
Low Input Voltage 2 (Low to High Threshold)	V_{IL2}	0.8			V	Schmitt Trigger Inputs: all Floppy Disk Interface except FADSEL
High Input Voltage 2 (High to Low Threshold)	V_{IH2}			2.0	V	
Schmitt Trigger Hysteresis	V_{HYS}	0.45			V	Schmitt Trigger Inputs
Low Output Voltage 1	V_{OL1}			0.4	V	I_{OL} = 24.0 mA;
High Output Voltage 1	V_{OH1}	2.8			V	All outputs except Floppy Disk Interface I_{OH} = -5.0 mA
Low Output Voltage 2	V_{OL2}			0.4	V	I_{OL} = 48 mA; All Floppy Disk Interface
High Output Voltage 2	V_{OL2}	2.8			V	I_{OH} = -10 mA
Latch Up Current	I_{LU}	±200			mA	
Input Leakage Current 1	I_{L1}			±10.0	µA	All inputs except PCVAL, FADSEL, DRV, IDESEL
Low Input Pull-Up Current	I_{PU}	10.0		60	µA	V_{IN} = 0V; PCVAL, FADSEL, DRV, IDESEL
High Input Leakage Current 2	I_{L2}	0.0		-10.0	µA	V_{IN} = 5V; PCVAL, FADSEL, DRV, IDESEL
V_{CC} Supply Current 1 V_{CC} Supply Current 2 Power Down Mode V_{CC} Supply Current	I_{CC1} I_{CC2} I_{CCPD}		45 95 100		mA mA µA	100µA Source Loads 5 mA Source Loads V_{IN} = GND or V_{CC}; I_O = 0
Power Dissipation 1 Power Dissipation 2	PD_1 PD_2		425 575		mW mW	I_{CC1} Max I_{CC2} Max **
Power Qualified Reset Threshold	V_{PQR}	2.8		4.35	V	
Gain			TBD			V_{OUT}/V_{IN}
Pin Capacitance XTAL1			TBD		pf	
XTAL2			TBD		pf	

AC CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = 5.0 V ± 10%)

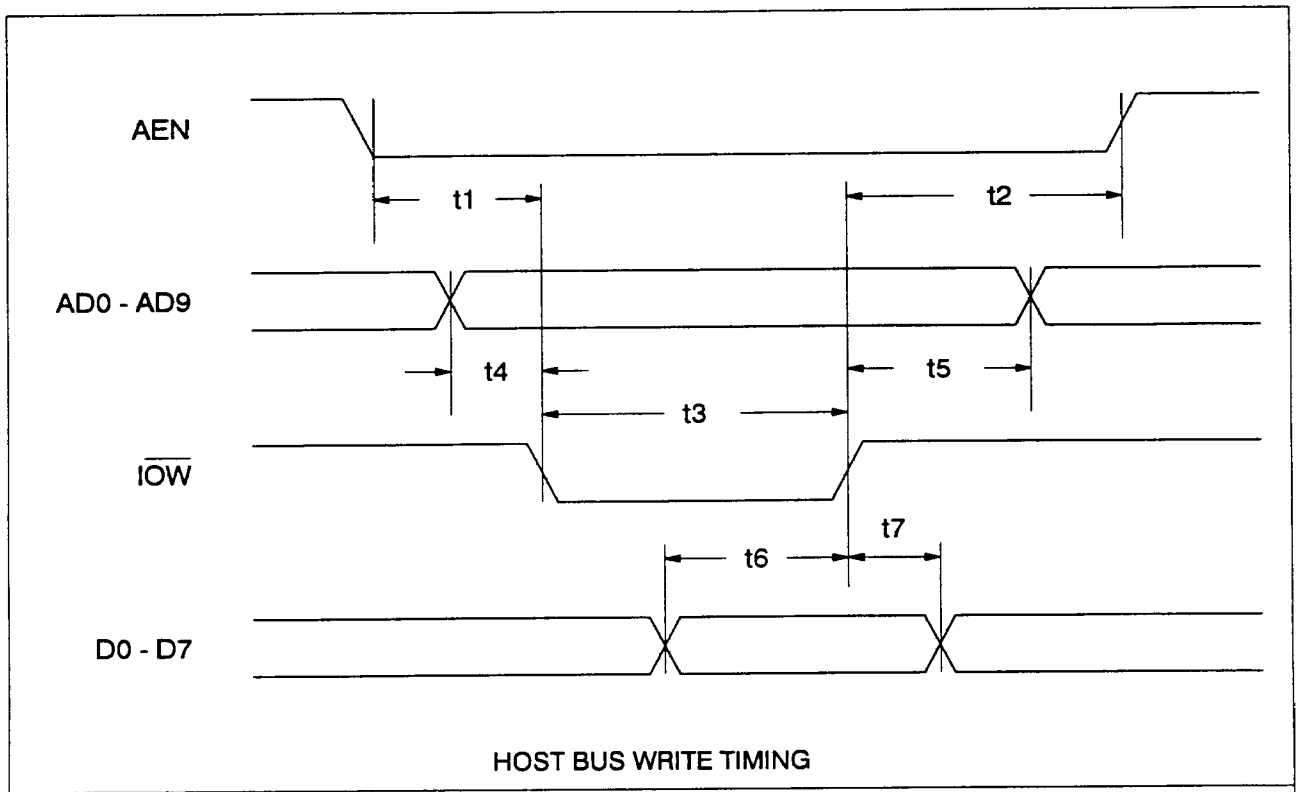
PRELIMINARY
NOTICE: This is not a final specification. Some parameters are subject to change.

HOST BUS AC TIMING

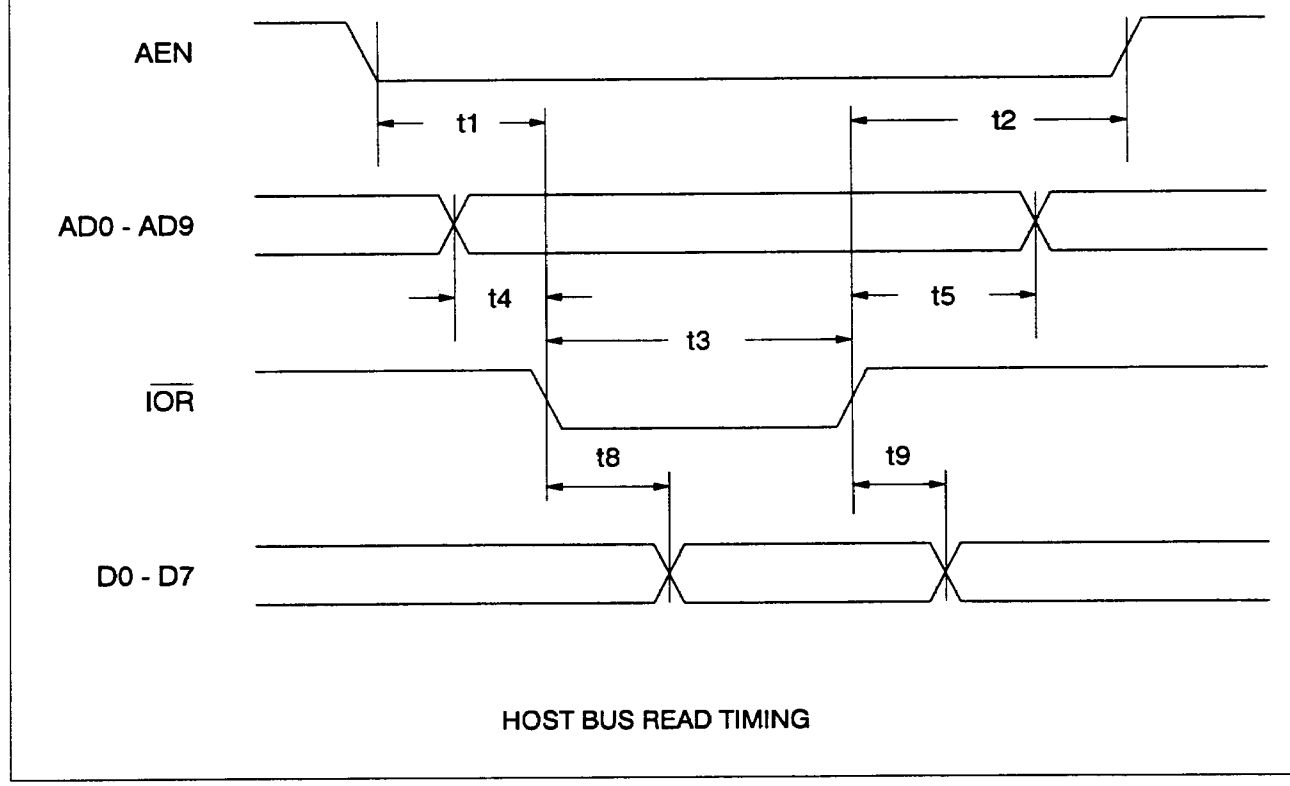
REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t1	AEN setup time to $\overline{IOW}$ and $\overline{IOR}$	40		ns	
t2	AEN hold time from $\overline{IOW}$ and $\overline{IOR}$	10		ns	
t3	$\overline{IOR}$ and $\overline{IOW}$ pulse width	150		ns	
t4	Address setup time	40		ns	
t5	Address hold time	10		ns	
t6	Data setup time to $\overline{IOW}$	40		ns	
t7	Data hold time from $\overline{IOW}$	10		ns	
t8	Data propagation delay from $\overline{IOR}$		100	ns	
t9	Data hold time	10	60	ns	

IDE INTERFACE TIMING

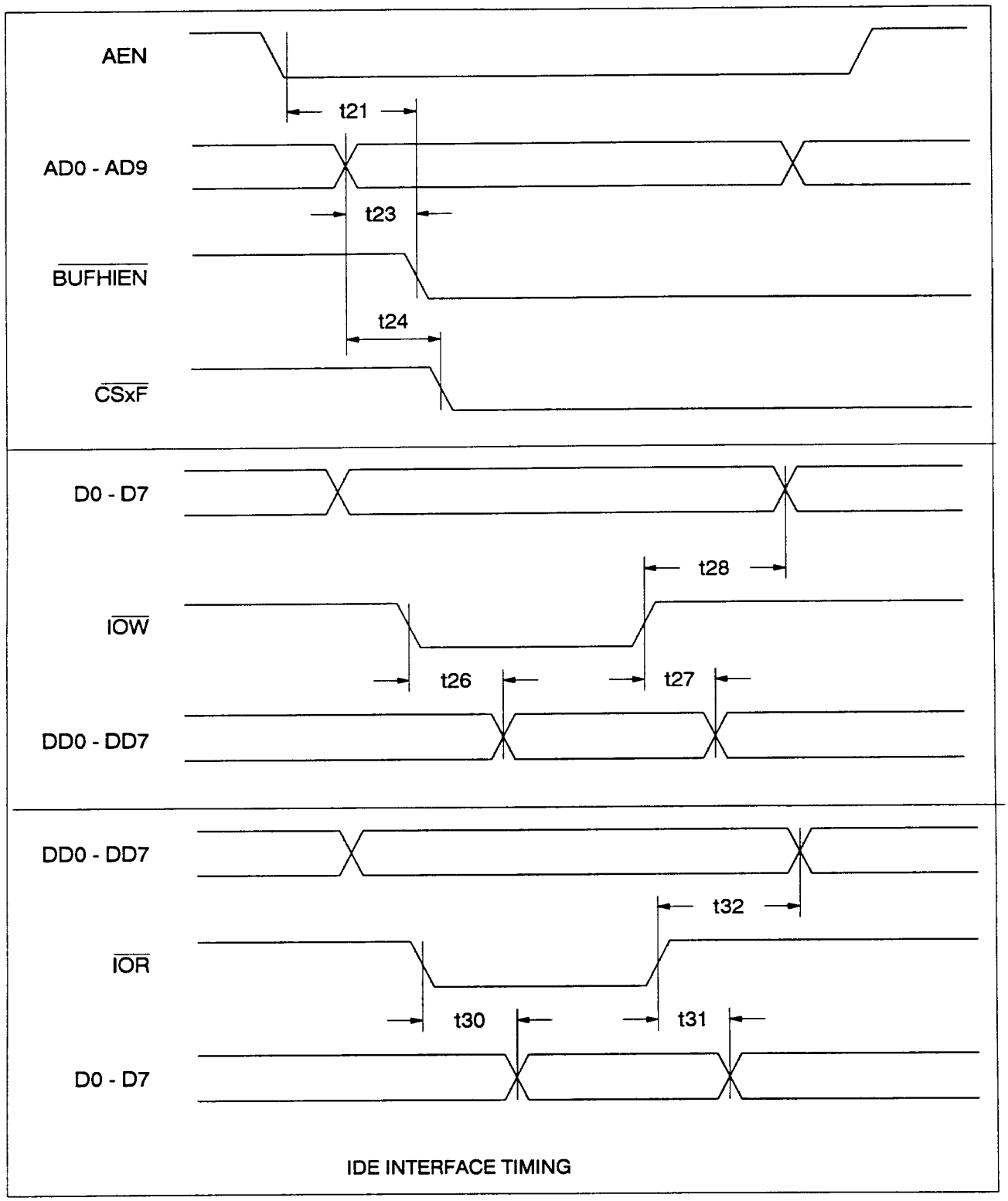
REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t21	$\overline{BUFHIEN}$ delay from AEN		40	ns	
t23	$\overline{BUFHIEN}$ delay from AD0 - AD9		40	ns	
t24	CS1F, CS3F delay from AD0 - AD9		TBD	ns	
t26	DD0 - DD7 delay from $\overline{IOW}$		60	ns	
t27	DD0 - DD7 hold time	TBD	100	ns	
t28	DD0 - DD7 setup time	40		ns	
t30	D0 - D7 delay from $\overline{IOR}$		50	ns	
t31	D0 - D7 hold	10	60	ns	
t32	D0 - D7 hold time	40		ns	



HOST BUS WRITE TIMING



HOST BUS READ TIMING



IDE INTERFACE TIMING

PRELIMINARY
NOTICE: This is not a final specification. Some parameters are subject to change.

DMA TIMING

REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t1	DMARQ cycle time	52		X*	
t2	$\overline{DACK}$ Delay time from DMARQ High	0		ns	
t3	DMARQ Reset Delay from $\overline{DACK}$ Low		140	ns	
t4	$\overline{DACK}$ Width	90		ns	
t5	$\overline{IOR}$ or $\overline{IOW}$ Response from DMARQ High		48	X*	
t6	$\overline{IOR}$ Delay from DMARQ High	0		ns	
t7	$\overline{IOW}$ Delay from DMARQ High	0		ns	
t8	Data Access Time from $\overline{IOR}$ Low		90	ns	
t9	Data Set Up Time from $\overline{IOR}$ High	80		ns	
t10	Data to Float Delay from $\overline{IOR}$ High	10	65	ns	
t11	Data Hold Time from $\overline{IOW}$ High	0		ns	
t12	AEN High to $\overline{DACK}$ Low		TBD	ns	

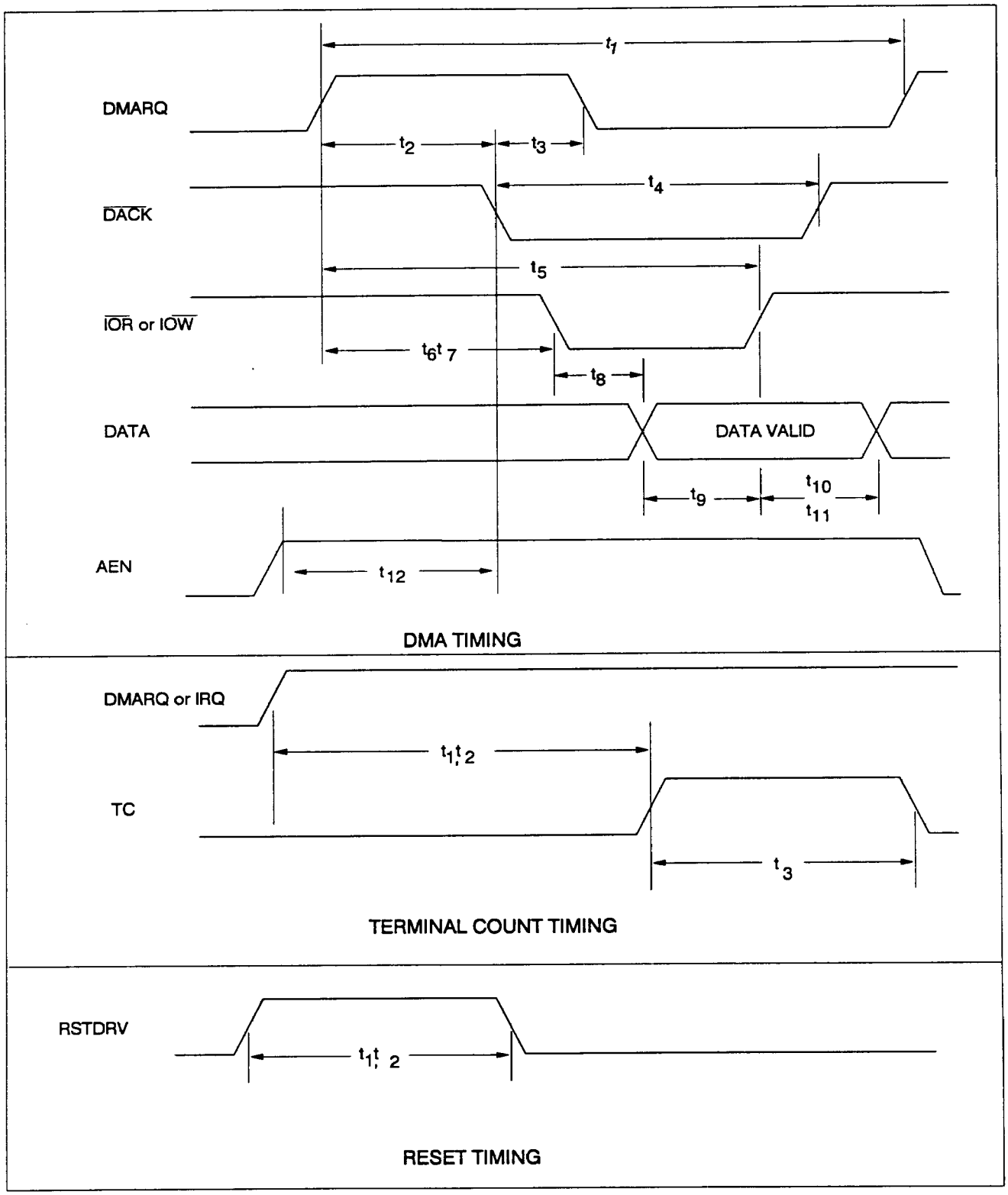
TERMINAL COUNT TIMING

REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t1	TC Delay from Last DMARQ or IRQ, Read	0	192	X*	
t2	TC Delay from Last DMARQ or IRQ, Write		384	X*	
t3	TC Width	60		ns	

RESET TIMING

REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t1	RSTDRV Pulse Width	250		ns	
t2	Software Reset Pulse Width	5		X*	

* X specifies one MCLK period. It is dependent upon the selected data rate (see Table 10).



PRELIMINARY
NOTICE: This is not a final specification. Some parameters are subject to change.

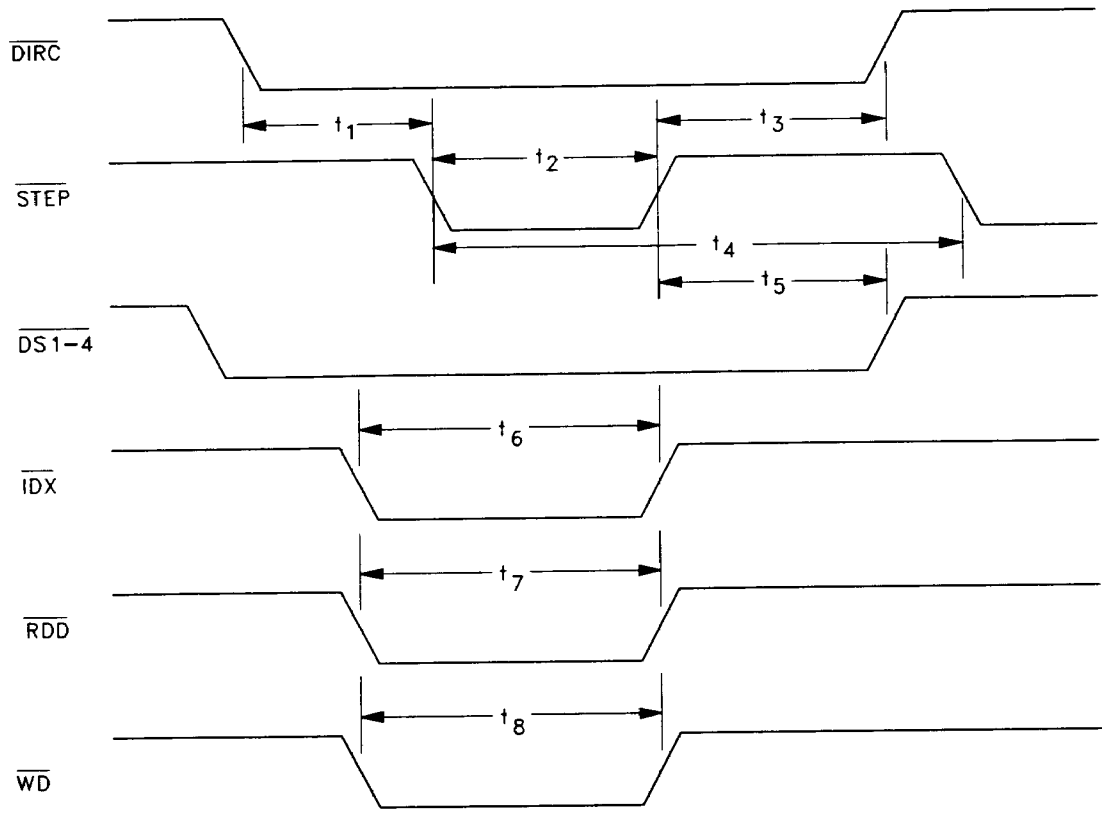
DISK DRIVE TIMING

REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t1	$\overline{\text{DIRC}}$ Set Up to $\overline{\text{STEP}}$ Low	4		X*	
t2	$\overline{\text{STEP}}$ Active Time Low	24		X*	
t3	DIRC Hold Time After $\overline{\text{STEP}}$	96		X*	
t4	$\overline{\text{STEP}}$ Cycle Time	132		X*	
t5	$\overline{\text{DS1-4}}$ Hold Time from $\overline{\text{STEP}}$ Low	20		X*	
t6	$\overline{\text{IDX}}$ Pulse Width	2		X*	
t7	$\overline{\text{RDD}}$ Active Time Low	40		ns	
t8	$\overline{\text{WD}}$ Write Data Width Low	.5 Typ		Y**	

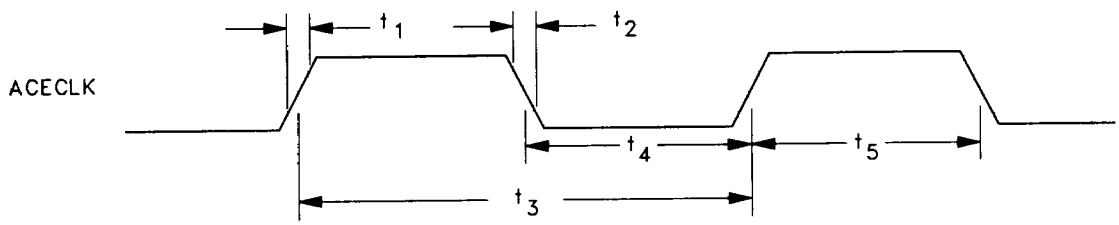
* X specifies one MCLK period. It is dependent upon selected data rate (see Table 10).
** Y specifies one WCLK period. It is dependent upon selected data rate (see Table 10).

ACECLK TIMING

REF	DESCRIPTION	MIN	MAX	UNITS	NOTES
t1	Clock Rise Time		20	ns	
t2	Clock Fall time		20	ns	
t3	Clock Cycle Time	542.5 typ		ns	
t4	Clock Low Time	252 typ		ns	
t5	Clock High Time	252 typ		ns	



DISK DRIVE TIMING



CLOCK TIMING

Table 16 - PROGRAMMING VALUES FOR FLOPPY DISK CONTROLLERS (IBM PC AND PC/AT COMPATIBLE SYSTEMS)

Parameter	HEX VALUES TO BE PROGRAMMED			
	1.44 MB 3.5"	720 KB 3.5"	1.2 MB 5.25"	360 KB 5.25"
Bytes/Sector (N)	02	02	02	02
Sectors/Track (SC)	12	09	0F	09
Gap Length (1) (GPL1)	1B	2A	1B	2A
Gap Length (2),(3)(GPL2,3)	6C	50	54	50
Head Settle Time (ms)	15	15	15	15
Motor Start Up (1/8 sec)	08	08	08	08
Cylinders	80	80	80	40
Tracks	160	160	160	80
Tracks/Inch	135	135	96	48
Heads	02	02	02	02
RPM	300	300	360	300
Transfer (KB/s)	500	250	500	250

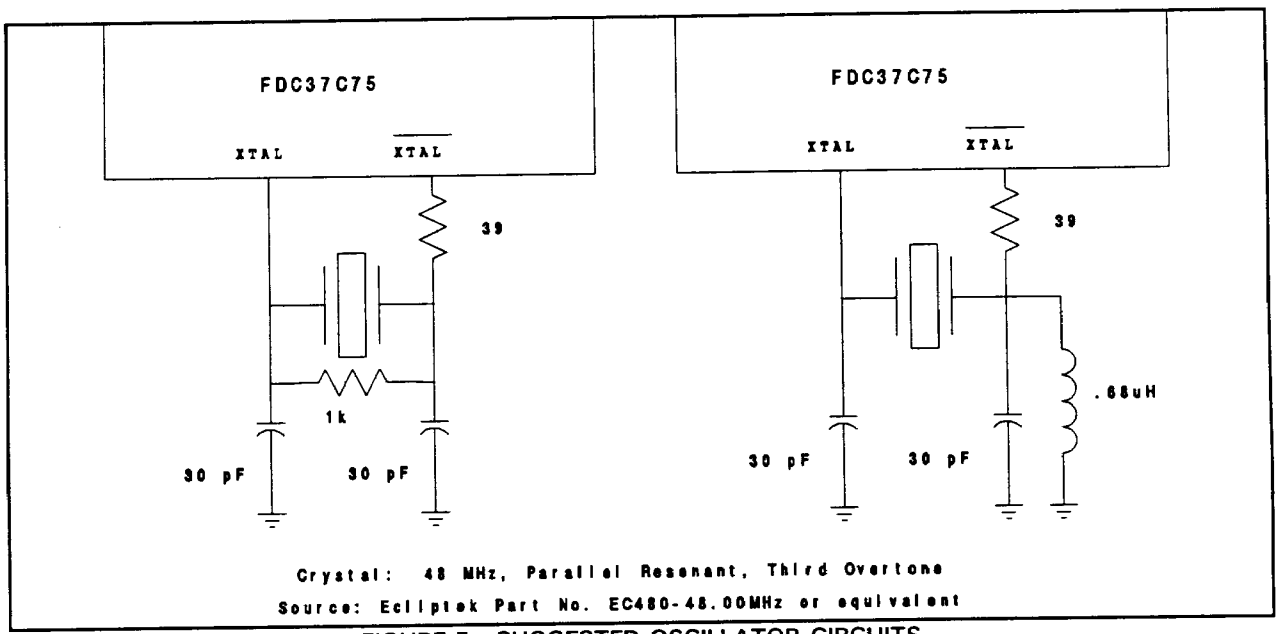


FIGURE 5 - SUGGESTED OSCILLATOR CIRCUITS

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