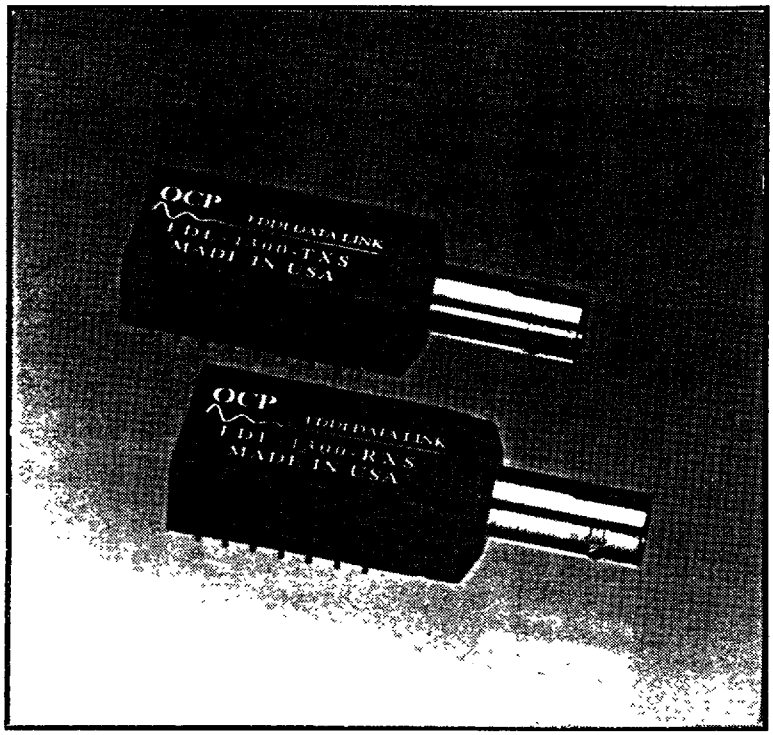
T-41-91

OCP

FDL-1300-SA SPECIAL

Data Link Modules for FDDI



Features

- ☐ *Full FDDI Compliance*
- ☐ *Integral ST™ Optical Connector*
- ☐ *Single Supply Voltage (+5 V or -5.2 V)*
- ☐ *Standard 16 Pin Footprint*
- ☐ *Model FDL-1300-SA is Pinout Compatible with AT&T ODL-125*
- ☐ *Dual-in-Line Conductive Plastic Package*
- ☐ *0°C to +70°C Operating Temperature Range*

Description

The FDL-1300 Fiber Optic Transmitter and Receiver Data Link Set is designed to meet or exceed all the requirements of the Physical Layer Medium Dependent (PMD) specification for the Fiber Distributed Data Interface (FDDI). Highly reliable 1300 nm surface-emitting LEDs selected for proper rise/fall time, center wavelength and spectral width are utilized in the transmitters. The receivers incorporate an InGaAs/InP PIN photodiode and a high speed transimpedance amplifier to meet the sensitivity and dynamic range requirements of FDDI. The receiver post- amplifier features the specified Signal Detect function and differential emitter coupled logic (ECL) outputs. The FDL-1300-SA transmitters and receivers are housed in a cost-effective 16-pin dual-in-line conductive plastic package with integral ST™ connector and operate on standard +5 volt or -5.2 volt power supply.

The FDL-1300-SA transmitter and receiver are pin compatible with the ODL-125 Data Link Modules from AT&T. The receiver, SA-01, is optimized for both 125 Mbaud (FDDI) and 50 Mbaud operation.

Optical Communication Products, Inc.

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Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	- 55	+ 100	°C
Operating Temperature	- 40	+ 85	°C
Supply Voltage	0	+ 6.0	V
Input Voltage	0	+ 6.0	V
Lead Soldering	-	240 °C, 10 sec	-

Transmitter Electrical Interface

Parameter		Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	+ 5 V	V_{CC}	4.75	5.0	5.25	V
	- 5.2 V	V_{EE}	- 5.25	- 5.2	- 4.75	V
Supply Current		I	-	110	135	mA
Power Dissipation		P	-	550	700	mW
Input HIGH Voltage (Data/$\overline{\text{Data}}$)		V_{IHS}	V_{CC} - 1.15	-	V_{CC} - 0.73	V
Input LOW Voltage (Data/$\overline{\text{Data}}$)		V_{ILS}	V_{CC} - 1.87	-	V_{CC} - 1.45	V
Differential Input Voltage		V_{DIF}	0.3	-	1.1	V
Input Common Mode Voltage [1]		V_{ICM}	-	-	1.0	V
Reference Voltage		V_{BB}	V_{CC} - 1.39	V_{CC} - 1.29	V_{CC} - 1.17	V

[1] Permissible ± V_{ICM} with respect to V_{BB}.

Receiver Electrical Interface

Parameter		Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	+ 5 V	V_{CC}	4.75	5.0	5.25	V
	- 5.2 V	V_{EE}	- 5.25	- 5.2	- 4.75	V
Supply Current		I	-	55	65	mA
Power Dissipation		P	-	275	350	mW
Output HIGH Voltage		V_{OH}	V_{CC} - 1.035	-	V_{CC} - 0.88	V
Output LOW Voltage		V_{OL}	V_{CC} - 1.83	-	V_{CC} - 1.62	V

Transmitter and Receiver Operation

The transmitter behaves logically as a differential input gate which controls a 1300 nm LED. When the DATA input voltage is greater than the $\overline{\text{DATA}}$ input voltage, the LED is ON, and vice versa. In single-ended applications, the unused input pin should be connected to reference voltage V_{BB} or biased to V_{CC} - 1.29 volts.

The receiver converts the incident optical power to a photocurrent via a high performance PIN photodiode. The photocurrent is converted to a voltage signal by a transimpedance amplifier. This signal is then amplified by additional gain stages and processed through a shaping filter and a comparator to generate the differential ECL outputs. Both outputs (DATA and $\overline{\text{DATA}}$) are open emitters requiring termination to V_{CC} - 2 volts with 50 ohms or to V_{EE} with 510 ohms. For optimum performance both outputs should be terminated identically, even if only one output is used.

The Signal Detect circuit monitors the level of incoming optical signal and generates a logic LOW signal when insufficient photocurrent is produced to ensure proper operation. The Signal Detect can be used to control an external squelch circuit to gate off spurious outputs generated by the receiver when no optical input is available. The outputs are open emitter ECL requiring termination (510 ohms to V_{EE} is recommended).

Transmitter Performance (Over Operating Temperature Range 0°C to +70°C)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Rate	B	DC	125	130	Mb/s
Optical Output Power	$\overline{P}_o$	- 19.0	- 16.0	- 14.0	dBm
Center Wavelength[1]	λ_c	1270	1320	1380	nm
Rise Time (10% to 90%)[1]	t_r	0.6	-	3.0	ns
Fall Time (90% to 10%)[1]	t_f	0.6	-	3.0	ns
Random Jitter (p-p)	RJ	0	-	0.70	ns
Duty Cycle Distortion (p-p)	DCD	0	-	0.6	ns
Data Dependent Jitter (p-p)	DDJ	0	-	0.6	ns
Extinction Ratio (P_{off}/P_{on}) x 100%	-	-	-	10	%
Transmit OFF Power	P_{off}	-	-	- 45.0	dBm
Spectral Width[1]	$\Delta\lambda$	-	150	-	nm

[1] Center wavelength, spectral width, and rise/fall time are compliant with Figure 5.1 of the FDDI PMD.

Receiver Performance (Over Operating Temperature Range 0°C to +70°C)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Data Rate		B	1	125	130	Mb/s
Optical Input Power (BER = 2.5×10^{-10})	FDDI Test[1]	$\overline{P}_{in}$	- 32.0	- 33	- 14.0	dBm
	Sensitivity[2]		- 35.5	- 37.0		
Signal Detect Thresholds	Assertion	P_{sd}	-	-	- 35.0	dBm
	Deassertion		- 45.0	-	-	
Signal Detect Hysteresis			1.5	-	-	dB
Signal Detect Timing	Assertion	T_{sd}	-	-	100	μs
	Deassertion		-	-	350	
Wavelength of Operation		λ	1100	1320	1600	nm
Output Duty Cycle Distortion (p-p)		DCD	-	-	0.4	ns

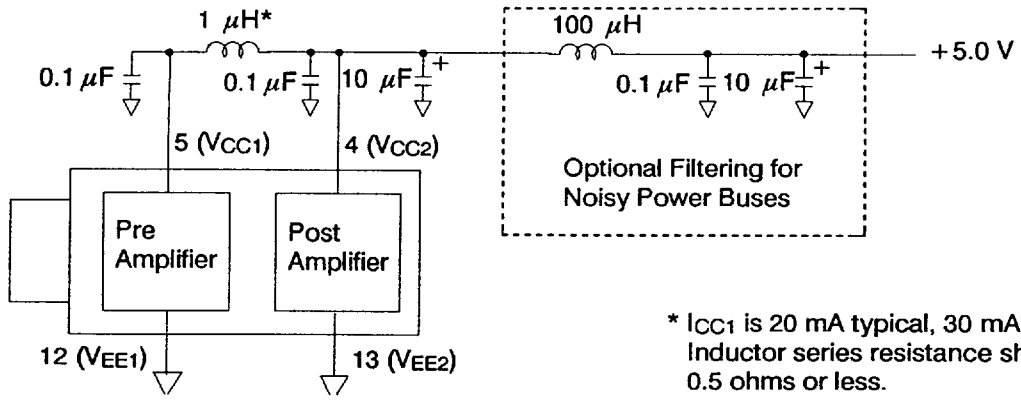
[1] FDDI Test Conditions.
[2] When tested with 2^7-1 PRBS with 50% duty cycle, optical rise/fall time of 2.5 nsec, and optimum sampling point at 50 Mbaud.

Application Notes

The transmitter and receiver power supply leads should be bypassed with RF quality capacitors (0.1microfarad) close to the package. A solid ground plane and low impedance power supply traces are highly recommended. The transmitter differential inputs and the receiver differential outputs are high speed ECL signals. Printed circuit board interconnections should be configured in accordance with ECL design rules. The *MECL System Design Handbook* from Motorola, Inc. is an excellent reference. Board layouts created by CAD autorouting techniques should be reviewed carefully.

Special care should be taken with the receiver, since it is a very sensitive analog device. If the receiver outputs drive long traces or multiple loads, the use of an ECL buffer gate to isolate the receiver from transmission line reflections is recommended. Normal handling precautions for electrostatic-sensitive devices should be observed.

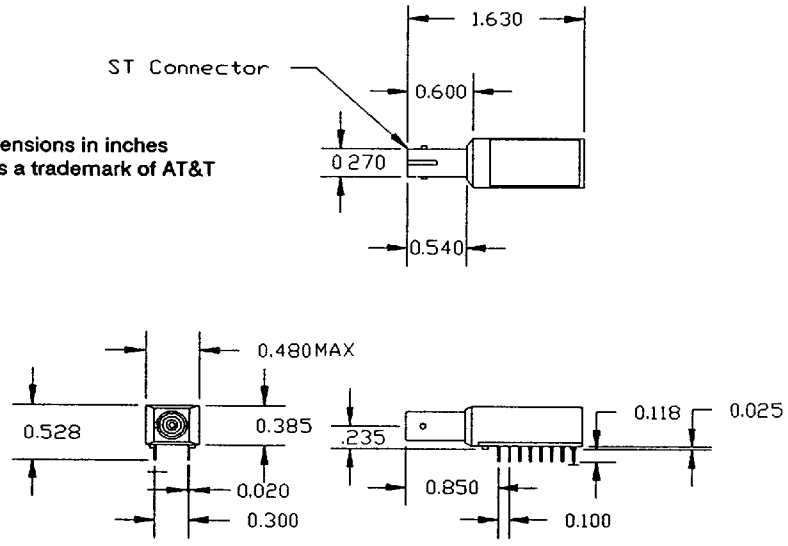
Recommended De-Coupling Circuit for +5 V Operation



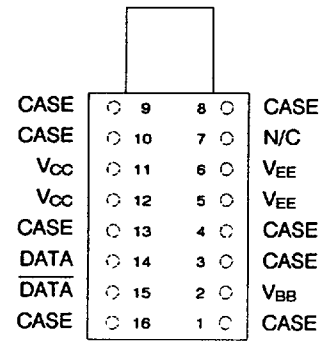
All case pins should be grounded.

* I_{CC1} is 20 mA typical, 30 mA maximum. Inductor series resistance should be 0.5 ohms or less.

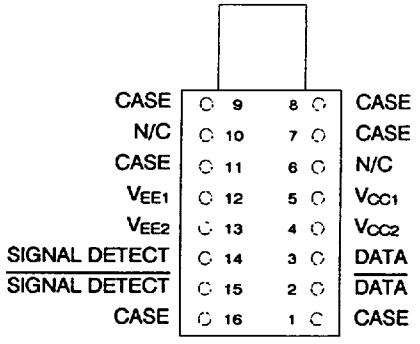
Package Outline



Pin Assignments (Top View)



Transmitter



Receiver

N/C — No internal connection

Ordering Information

FDL - 1300 -XX - SA-XX

Function

TX: Transmitter
RX: Receiver

Type

blank: for TX
01: for RX

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