FAIRCHILD SEMICONDUCTOR™

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ADVANCE INFORMATION

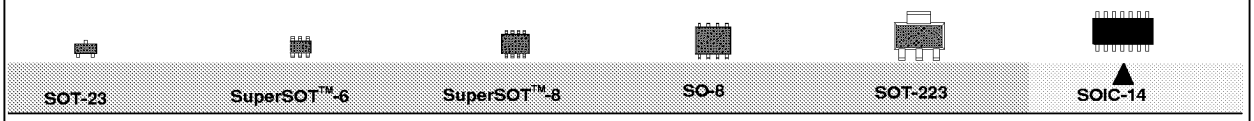
FDQ4006N
Dual Common Drain
N-Channel Enhancement Mode Field Effect Transistor

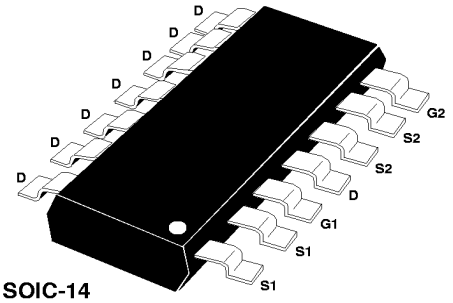
General Description

SOIC-14 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices can be paralleled externally for use in high current DC-DC converters in notebook computer and other battery powered circuits where fast switching, very low in-line power loss, and resistance to transients are needed.

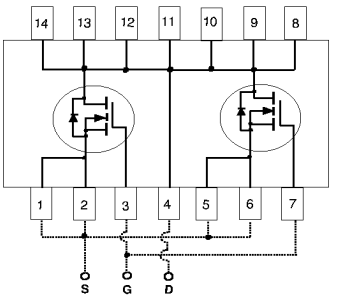
Features

- 13 A, 30 V. $R_{DS(ON)}$ = 0.0075 Ω @ V_{GS} =10 V
  $R_{DS(ON)}$ = 0.011 Ω @ V_{GS} = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- Common drain connection for easy parallel operation.
- High power and current handling capability in industry standard SOIC-14 package.





SOIC-14



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		FDQ4006N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	13	A
	- Pulsed		35	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	15	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

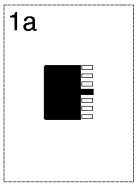
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 13A			0.0075	Ω
		T_J = 125°C			0.0135	
		V_{GS} = 4.5 V, I_D = 11 A			0.011	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	35			A
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.6 A (Note 2)			1.2	V

Notes:

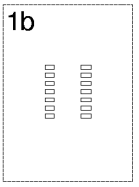
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:



a. 50°C/W when mounted on a package size 2oz copper pad.



b. 83°C/W when mounted on a 2oz minimum copper pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.