



T-52-09

Advance Information

FE5020

Address and Data Buffer Device

- Runs in Systems with Clock Speeds to 20 MHz
- Provides Address and Data Buffers that Interface to the Micro Channel*
- Contains Local Bus Address and Data Buffers for Onboard Peripherals
- Meets Micro Channel AC/DC Specifications
- 24 Milliamp Output Drive Capability
- Low Power 1.25 Micron CMOS Technology
- Surface Mountable 132 Lead JEDEC Plastic Quad Flat Pack

As part of the Faraday® FE5400 Chip Set, the FE5020 Integrated Address and Data Buffer Device significantly facilitates the design and implementation of IBM PS/2* Model 50 and 60 compatible system boards. By combining functionality normally implemented in 10 discrete components, the FE5020 decreases design complexity, saves space, reduces system cost, and increases system reliability. Figure 1 shows a typical system diagram using the FE5400 Chip Set.

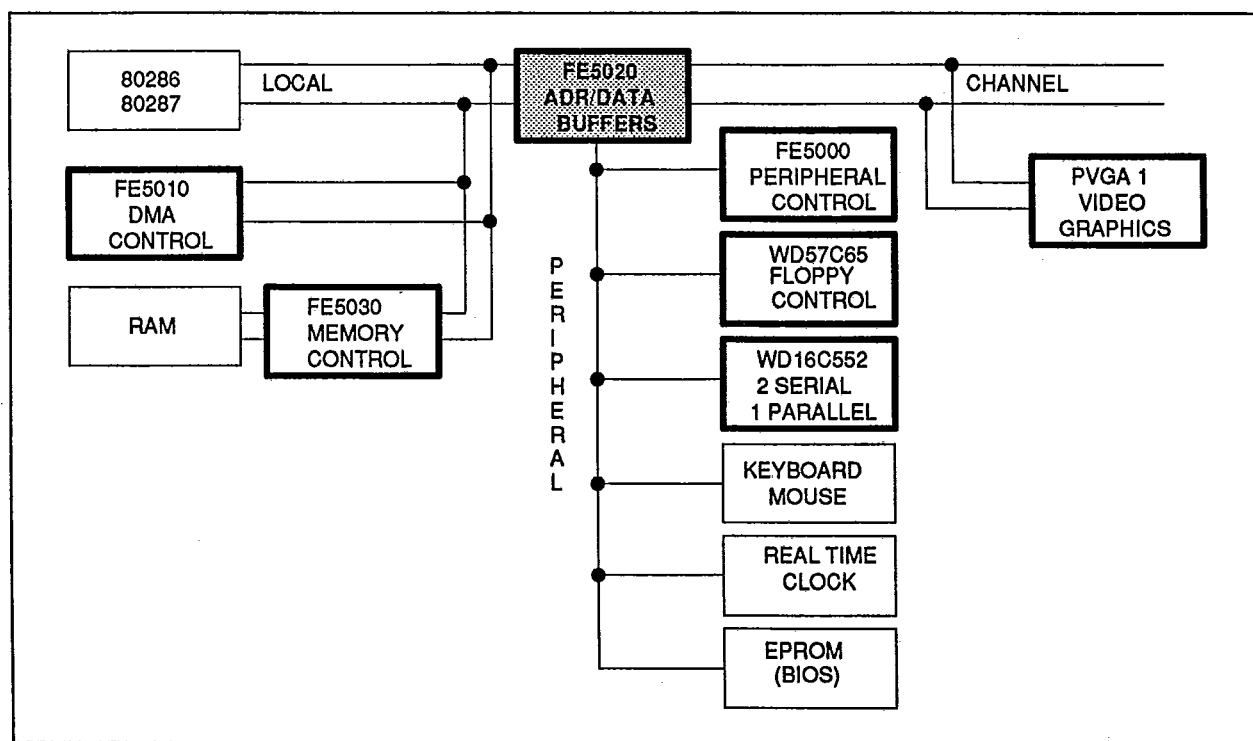


Figure 1. System Diagram (Devices with Bold Outlines are Available from Western Digital Corporation)

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Release 1.0**January 31, 1988****Additional References***IBM PS/2 Model 50160 Technical Reference Manual**Intel* Microprocessor and Peripheral Handbook***Disclaimer**

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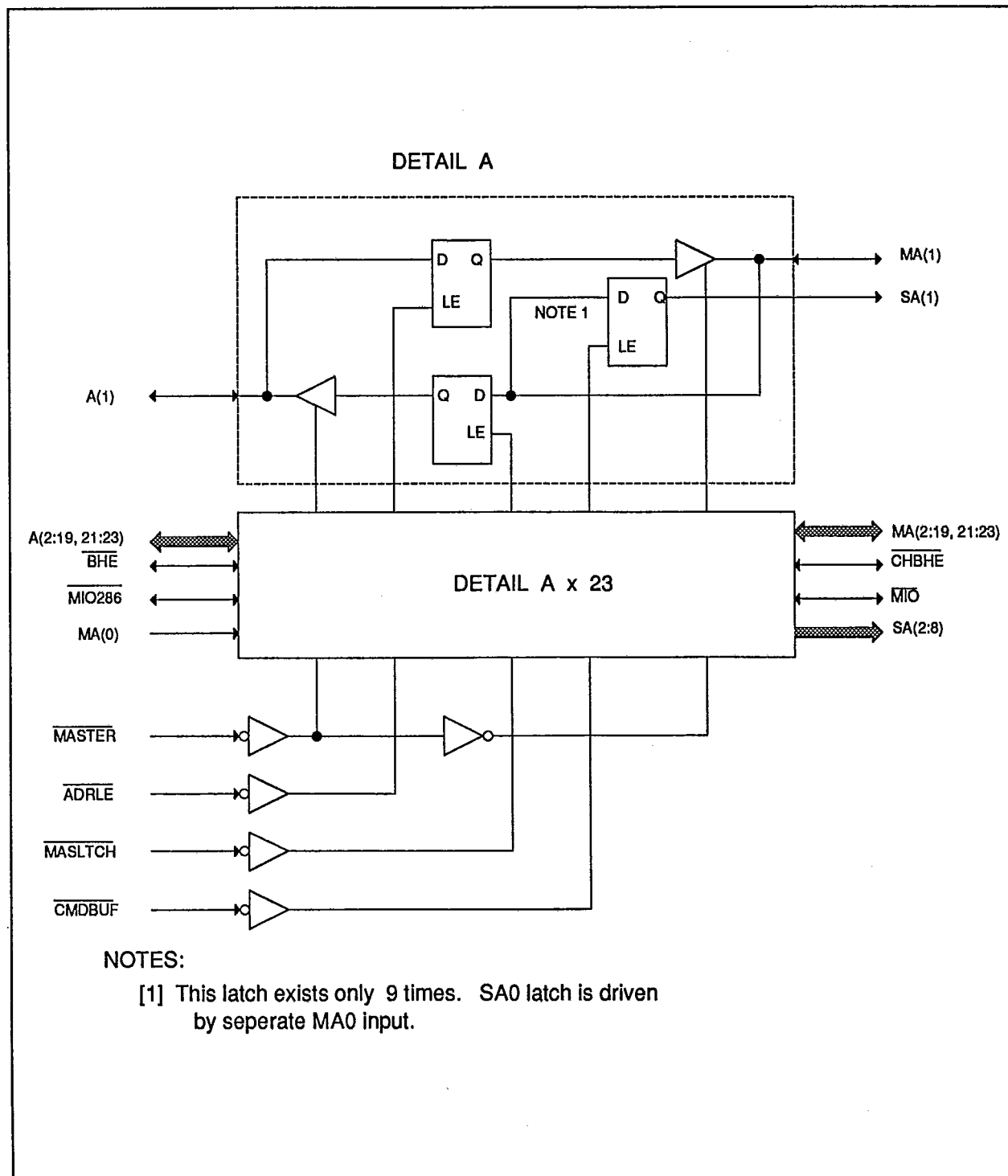


Figure 2. FE5020 Address Path Block Diagram

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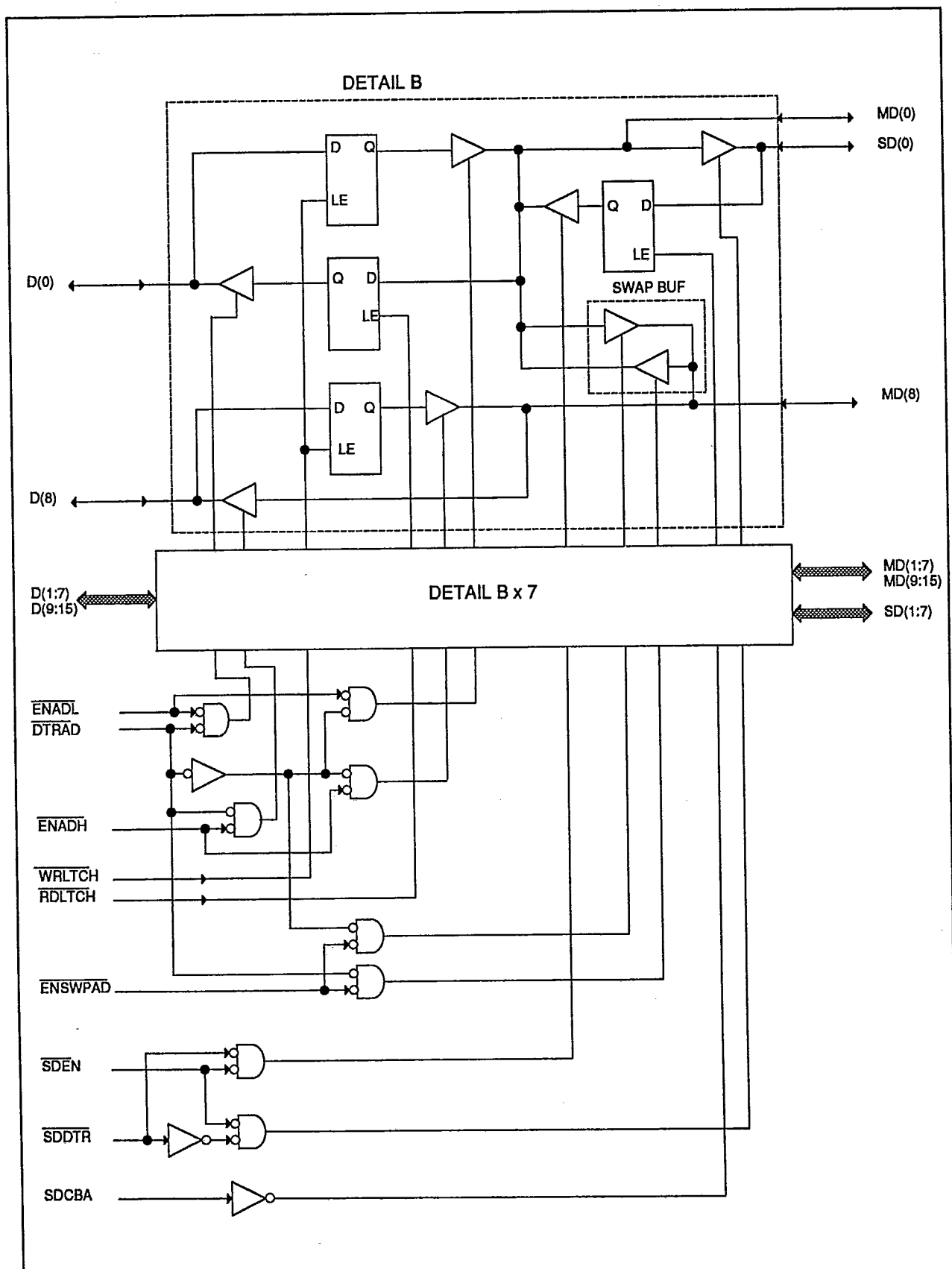


Figure 3. FE5020 Data Path Block Diagram

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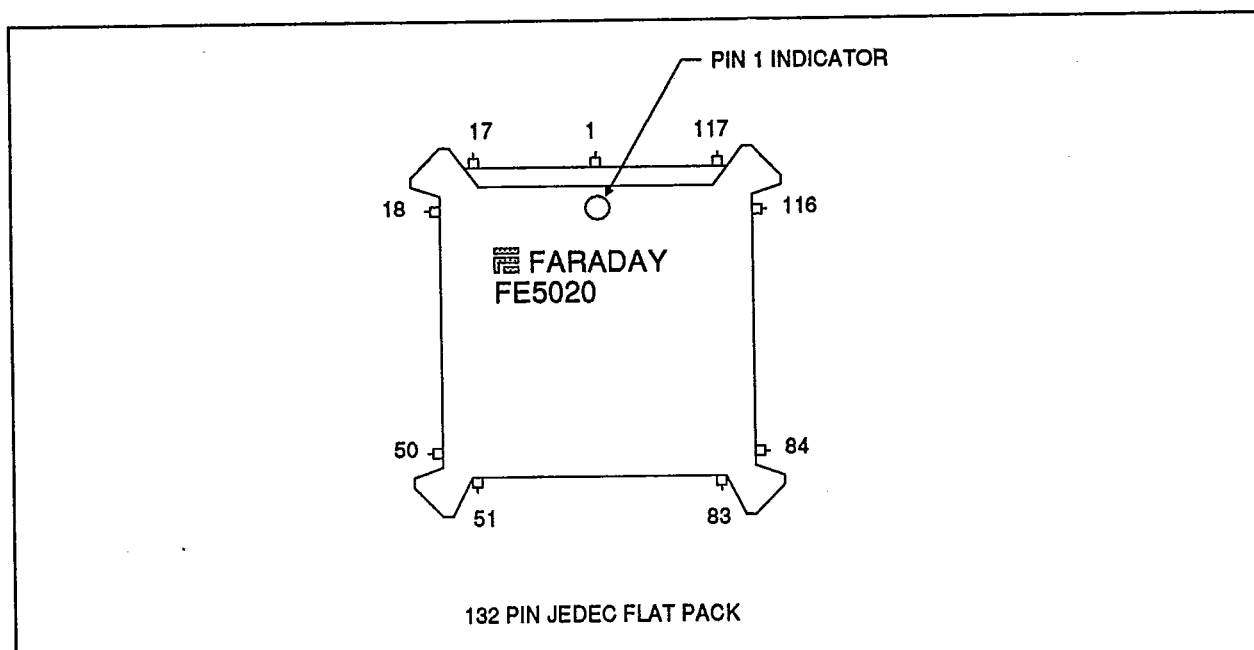


Figure 4. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	MA12	34	A16	67	MD6	100	SD7
2	MA11	35	A17	68	Vss	101	SD6
3	MA10	36	A18	69	MD7	102	SD5
4	Vss	37	A19	70	MD8	103	SD4
5	MA9	38	A21	71	MD9	104	SD3
6	MA8	39	A22	72	Vss	105	SD2
7	MA7	40	A23	73	MD10	106	SD1
8	Vss	41	Vss	74	MD11	107	SD0
9	MA6	42	ENADL	75	MD12	108	Vss
10	MA5	43	SDDTR	76	Vss	109	MIO ²⁸⁶
11	MA4	44	WRTLCH	77	MD13	110	BHE
12	Vss	45	ADRL	78	MD14	111	SA8
13	MA3	46	MASLTCH	79	MD15	112	SA7
14	MA2	47	RDLTCH	80	BIAS	113	SA6
15	MA1	48	SDCBA	81	VDD	114	SA5
16	VDD	49	CMDBUF	82	D0	115	SA4
17	A1	50	MASTER	83	D1	116	SA3
18	A2	51	MA0	84	D2	117	SA2
19	A3	52	SDEN	85	D3	118	SA1
20	A4	53	ENADH	86	D4	119	SA0
21	A5	54	DTRAD	87	D5	120	MA23
22	A6	55	ENSWPAD	88	D6	121	MA22
23	A7	56	VDD	89	D7	122	MA21
24	VDD	57	MIO	90	D8	123	Vss
25	A8	58	CHBHE	91	D9	124	MA19
26	A9	59	MD0	92	D10	125	MA18
27	A10	60	Vss	93	Vss	126	MA17
28	A11	61	MD1	94	D11	127	MA16
29	Vss	62	MD2	95	D12	128	Vss
30	A12	63	MD3	96	D13	129	MA15
31	A13	64	Vss	97	D14	130	MA14
32	A14	65	MD4	98	D15	131	MA13
33	A15	66	MD5	99	VDD	132	Vss

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1.0 PIN DESCRIPTION

PIN NO.	NAME	TYPE	FUNCTION
17	A1	IO	CPU ADDRESS—Bi-directional address bus connected to the CPU and the FE5010. A0 and A20 come directly from the FE5010.
18	A2		
19	A3		
20	A4		
21	A5		
22	A6		
23	A7		
25	A8		
26	A9		
27	A10		
28	A11		
30	A12		
31	A13		
32	A14		
33	A15		
34	A16		
35	A17		
36	A18		
37	A19		
38	A21		
39	A22		
40	A23		
15	MA1	IO	CHANNEL ADDRESS—Bi-directional Channel address bus.
14	MA2		
13	MA3		
11	MA4		
10	MA5		
9	MA6		
7	MA7		
6	MA8		
5	MA9		
3	MA10		
2	MA11		
1	MA12		
131	MA13		
130	MA14		
129	MA15		
127	MA16		
126	MA17		
125	MA18		
124	MA19		
122	MA21		
121	MA22		
120	MA23		
110	BHE	IO	BYTE HIGH ENABLE—This signal is connected to the FE5010 and CPU and indicates whether a high byte is being transferred during the current cycle.

O = Output, I = Input, IO = Bidirectional

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58	CHBHE	IO	CHANNEL BYTE HIGH ENABLE—This signal is connected to the Channel and indicates whether a high byte is being transferred during the current cycle.
109	MIO286	IO	MEMORY/IO 286—This signal is connected to the FE5010 and CPU and is used to encode the bus cycle type information.
57	MIO	IO	CHANNEL MEMORY/IO—This signal and NCHS(0:1) from the FE5010 encode the Channel bus cycle type information.
45	ADRLE	I	ADDRESS LATCH ENABLE—This signal latches the address to the Channel.
46	MASLTCH	I	MASTER LATCH—This signal latches the address from the Channel.
50	MASTER	I	MASTER—This signal determines the direction of the address.
82 83 84 85 86 87 88 89 90 91 92 94 95 96 97 98	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	IO	CPU DATA—Bi-directional data bus connected to the CPU and the FE5010.
59 61 62 63 65 66 67 69 70 71 73 74 75 77 78 79	MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15	IO	CHANNEL DATA—Bi-directional Channel data bus.
42	ENADL	I	ENABLE DATA LOW—This signal enables the low byte from the Channel.
53	ENADH	I	ENABLE DATA HIGH—This signal enables the high byte from the Channel.
55	ENSWPAD	I	ENABLE SWAP ADDRESS—This signal enables a byte swap on the Channel.
54	DTRAD	I	DATA TRANSFER DIRECTION—This signal indicates the direction of the data transfer on the Channel. When asserted low, Channel to CPU is enabled.
51	MA(0)	I	ADDRESS 0—This signal is A0 of the Channel.

O = Output, I = Input, IO = Bidirectional

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49	<u>CMDBUF</u>	I	<u>COMMAND BUFFERED</u> —This signal latches the address for the local bus.
119	SA0	O	<u>SYSTEM ADDRESS</u> —These signals are the address bus to the on-board peripherals.
118	SA1		
117	SA2		
116	SA3		
115	SA4		
114	SA5		
113	SA6		
112	SA7		
111	SA8		
107	SD0	IO	<u>SYSTEM DATA</u> —These signals are the peripheral data bus.
106	SD1		
105	SD2		
104	SD3		
103	SD4		
102	SD5		
101	SD6		
100	SD7		
48	SDCBA	I	<u>SYSTEM DATA CLOCK</u> —This signal latches the data from the peripheral bus.
43	<u>SDDTR</u>	I	<u>SYSTEM DATA TRANSMIT/RECEIVE</u> —This signal indicates the direction of the local data bus.
52	<u>SDEN</u>	I	<u>SYSTEM DATA ENABLE</u> —This signal enables the local data bus.
44	<u>WRTLCH</u>	I	<u>WRITE LATCH</u> —This signal latches write data to the Channel.
47	<u>RDLCH</u>	I	<u>READ LATCH</u> —This signal latches Channel low read data.
80	<u>BIAS</u>	I	<u>BIAS</u> —This pin provides a bias for internal current drivers. It should be connected through a 1% 1.25K ohm resistor to ground externally.
16,24,56, 81,99	VDD	I	+5V Power Supply
4,8,12, 29,41,60, 64,68,72, 76,93,108, 123,128, 132	VSS	I	0V Ground

O = Output, I = Input, IO = Bidirectional

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2.0 TECHNICAL SPECIFICATIONS

2.1 ABSOLUTE MAXIMUM RATINGS

These are absolute maximum stress ratings for the device. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V _{DD} -V _{SS})	0	7	V
Input Voltage	V _{IABS}	V _{SS} -0.3	V _{DD} +0.3	V
Bias on output pin	V _{OABS}	V _{SS} -0.3	V _{DD} +0.3	V
Storage Temperature	T _s	-40	125	°C

2.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

V_{SS} = 0 V

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V _{DD}	4.5	5.5	V
Ambient Temperature	T _A	0	70	°C
Input Voltage	V _{IN}	-0.3	V _{DD} +0.3	V
Power Dissipation	P _W	—	TBD	mW
Supply Current	I _{DD}	—	TBD	mA

2.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input capacitance @ f _c = 1 MHz	C _I	—	10	pF
I/O Capacitance	C _{IO}	—	15	pF
*Logic high input voltage	V _{IH}	2.0	—	V
*Logic low input voltage	V _{IL}	—	0.8	V
*Input leakage	I _{IL}	—	±10	uA
Tri-state output leakage	I _{OL}	—	±30	uA
I/O Pin Leakage	I _{IOL}	—	±40	uA
OUTPUTS MA [23:21], MA [19:1], MD [15:0], MIO, CHBHE				
Source current @ V _{OH} = 2.4 V	I _{OH}	4	—	mA
Sink current @ V _{OL} = 0.4 V	I _{OL}	24	—	mA
ALL OTHER OUTPUTS				
Source current @ V _{OH} = 2.4 V	I _{OH}	1	—	mA
Sink current @ V _{OL} = 0.4 V	I _{OL}	4	—	mA

Note:

The input pin "BIAS" is connected externally to ground through a 1% 1.25K ohm resistance and is part of an internal biasing circuit. Capacitance, leakage, and threshold measurements on this pin do not apply.

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3.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	A(23:21,19:1) delay to MA(23:21,19:1) 	0	25	1
T2	A(23:21,19:1) delay to MA(23:21,19:1) 	0	25	1
T3	A(8:1) delay to SA(8:1) 	0	50	1
T4	A(8:1) delay to SA(8:1) 	0	50	1
T5	MA(0) delay to SA(0) 	0	25	2
T6	MA(0) delay to SA(0) 	0	25	2
T7	BHE, MIO286 delay to CHBHE, MIO 	0	25	1
T8	BHE, MIO286 delay to CHBHE, MIO 	0	25	1
T9	MASTER on to MA(23:21,19:1) tristate	0	15	1
T10	MASTER off to A(23:21,19:1) tristate	0	15	1
T11	MASTER on to CHBHE, MIO tristate	0	15	1
T12	MASTER off to BHE, MIO286 tristate	0	15	1
T13	A(23:21,19:1), BHE, MIO286 setup to ADRL on	10	—	1
T14	A(23:21,19:1), BHE, MIO286 hold after ADRL on	5	—	1
T15	A(23:21,19:1), BHE, MIO286 setup to CMDBUF on	10	—	—
T16	A(23:21,19:1), BHE, MIO286 hold after CMDBUF on	5	—	—
T17	MA(23:21,19:1), CHBHE, MIO setup to CMDBUF on	10	—	2
T18	MA(23:21,19:1), CHBHE, MIO hold after CMDBUF on	5	—	2
T19	MA(23:21,19:1), CHBHE, MIO setup to MASLTCH on	10	—	1
T20	MA(23:21,19:1), CHBHE, MIO hold after MASLTCH on	5	—	1
T21	MA(23:21,19:1) delay to A(23:21,19:1) 	0	25	1
T22	MA(23:21,19:1) delay to A(23:21,19:1) 	0	25	1
T23	CHBHE, MIO delay to BHE, MIO286 	0	25	1
T24	CHBHE, MIO delay to BHE, MIO286 	0	25	1

Table 1. Address Path Timing (in nsec)

Notes:

1. Refer to CPU/Channel Address Control Function Table for control states.
2. Refer to Channel/Peripheral Bus Address Control Function Table for control states.

 = Positive Edge

 = Negative Edge

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		INPUT	OUTPUT
ADRL $\overline{E}$	MASTER	A(23:1), $\overline{MIO}$ 286, $\overline{BHE}$	MA(25:1), $\overline{MIO}$, $\overline{CHBHE}$
0	0	Storing	Tristate
0	1	Transparent	Current Inputs
1	0	Storing	Tristate
1	1	Storing	Previous Inputs
		INPUT	OUTPUT
MASLTCH	MASTER	MA(23:1), $\overline{MIO}$, $\overline{CHBHE}$	A(23:1), $\overline{MIO}$ 286, $\overline{BHE}$
0	0	Transparent	Current Inputs
0	1	Storing	Tristate
1	0	Storing	Previous Inputs
1	1	Storing	Tristate

Table 2. CPU/Channel Address Control Functions

		INPUT	OUTPUT
CMDBUF		MA(23:0)	SA(23:0)
0		X	Previous MA(23:0)
1		—	MA(23:0)

Table 3. Channel/Peripheral Bus Address Control Functions

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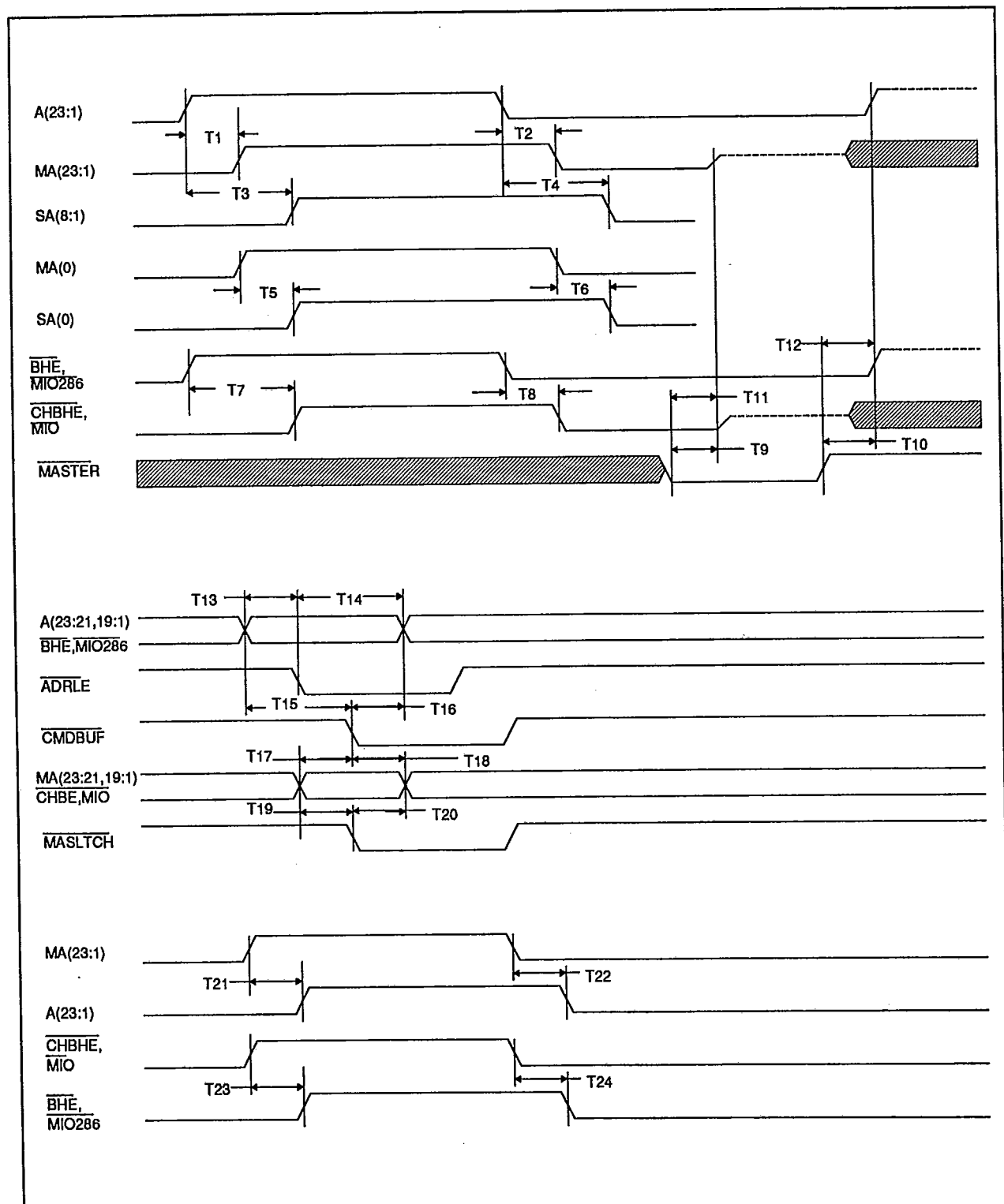


Figure 5. Address Path Timing

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PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	D(15:0) delay to MD(15:0) 	0	25	1
T2	D(15:0) delay to MD(15:0) 	0	25	1
T3	D(7:0) delay to SD(7:0) 	0	50	—
T4	D(7:0) delay to SD(7:0) 	0	50	—
T5	D(15:8) delay to MD(7:0) 	0	25	1
T6	D(15:8) delay to MD(7:0) 	0	25	1
T7	D(15:8) delay to SD(7:0) 	0	50	—
T8	D(15:8) delay to SD(7:0) 	0	50	—
T9	MD(15:0) delay to D(15:0) 	0	25	1
T10	MD(15:0) delay to D(15:0) 	0	25	1
T11	SD(7:0) delay to D(7:0) 	0	50	—
T12	SD(7:0) delay to D(7:0) 	0	50	—
T13	MD(7:0) delay to D(15:8) 	0	25	1
T14	MD(7:0) delay to D(15:8) 	0	25	1
T15	SD(7:0) delay to D(15:8) 	0	25	—
T16	SD(7:0) delay to D(15:8) 	0	25	—
T17	D(15:0) setup to $\overline{\text{WRLTCH}}$ high	10	—	1
T18	D(15:0) hold after $\overline{\text{WRLTCH}}$ high	5	—	1
T19	MD(7:0) setup to $\overline{\text{RDLTCH}}$ high	10	—	1
T20	MD(7:0) hold after $\overline{\text{RDLTCH}}$ high	5	—	1
T21	SD(7:0) setup to $\overline{\text{RDLTCH}}$ high	10	—	—
T22	SD(7:0) hold after $\overline{\text{RDLTCH}}$ high	5	—	—
T23	SD(7:0) setup to SDCBA low	10	—	2
T24	SD(7:0) hold after SDCBA low	5	—	2
T25	D(7:0) tristate from $\overline{\text{ENADL}}$ or $\overline{\text{DTRAD}}$ 	0	15	1
T26	D(15:8) tristate from $\overline{\text{ENADH}}$ or $\overline{\text{DTRAD}}$ high 	0	15	1
T27	MD(7:0) tristate from $\overline{\text{ENADL}}$ high	0	15	1
T28	D(15:8) tristate from $\overline{\text{ENADH}}$ high	0	15	1
T29	MD(15:0) tristate from $\overline{\text{DTRAD}}$ high	0	15	1
T30	SD(7:0) tristate from $\overline{\text{SDEN}}$ high	0	15	2
T31	SD(7:0) tristate from $\overline{\text{SDDTR}}$ low	0	15	2
T32	MD(7:0) tristate from $\overline{\text{ENSWPAD}}$ or $\overline{\text{DTRAD}}$ high	0	15	1
T33	MD(15:8) tristate from $\overline{\text{DTRAD}}$ low	0	15	1
T34	MD(15:8) tristate from $\overline{\text{ENSWPAD}}$ high	0	15	1
T35	MD(7:0) tristate from $\overline{\text{SDEN}}$ or $\overline{\text{SDDTR}}$ high	0	15	2,3
T36	MD(7:0) delay to SD(7:0) 	0	25	2
T37	MD(7:0) delay to SD(7:0) 	0	25	2
T38	SD(7:0) delay to MD(7:0) 	0	25	2
T39	SD(7:0) delay to MD(7:0) 	0	25	2

Table 4. Data Path Timing (in nsec)

Notes:

1. Refer to CPU/Channel Data Control Function Table for control states.
2. Refer to Channel/Peripheral Bus Data Control Function Table for control states.
3. Data sourced from SD bus latch.

 = Positive Edge
 = Negative Edge

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RDLTCH	WRTLCH	DTRAD	ENADL	ENADH	ENSWPAD	D(15:8)	D(7:0)	MD(15:8)	MD(7:0)
0	X	0	0	0	1	MD(15:8)	MD(7:0)	—	—
0	X	0	0	0	0	MD(7:0)	MD(7:0)	—	—
1	X	0	0	0	1	MD(15:1)	Previous MD(7:0)	—	—
1	X	0	1	1	1	Tristate	Tristate	—	—
X	0	1	0	0	1	—	—	D(15:8)	D(7:0)
X	0	1	0	0	0	—	—	D(15:8)	D(15:0)
X	1	1	0	0	1	—	—	Previous D(15:8)	Previous D(7:0)
X	1	1	1	1	1	—	—	Tristate	Tristate

Table 5. CPU/Channel Data Control Functions

SDDTR	SDEN	SDCBA	MD(7:0)	SD(7:0)
0	0	0	SD(7:0)	—
0	0	1	Previous SD(7:0)	—
X	1	X	Tristate	—
1	0	X	—	MD(7:0)
1	1	X	—	Tristate

Table 6. Channel/Peripheral Bus Data Control Functions

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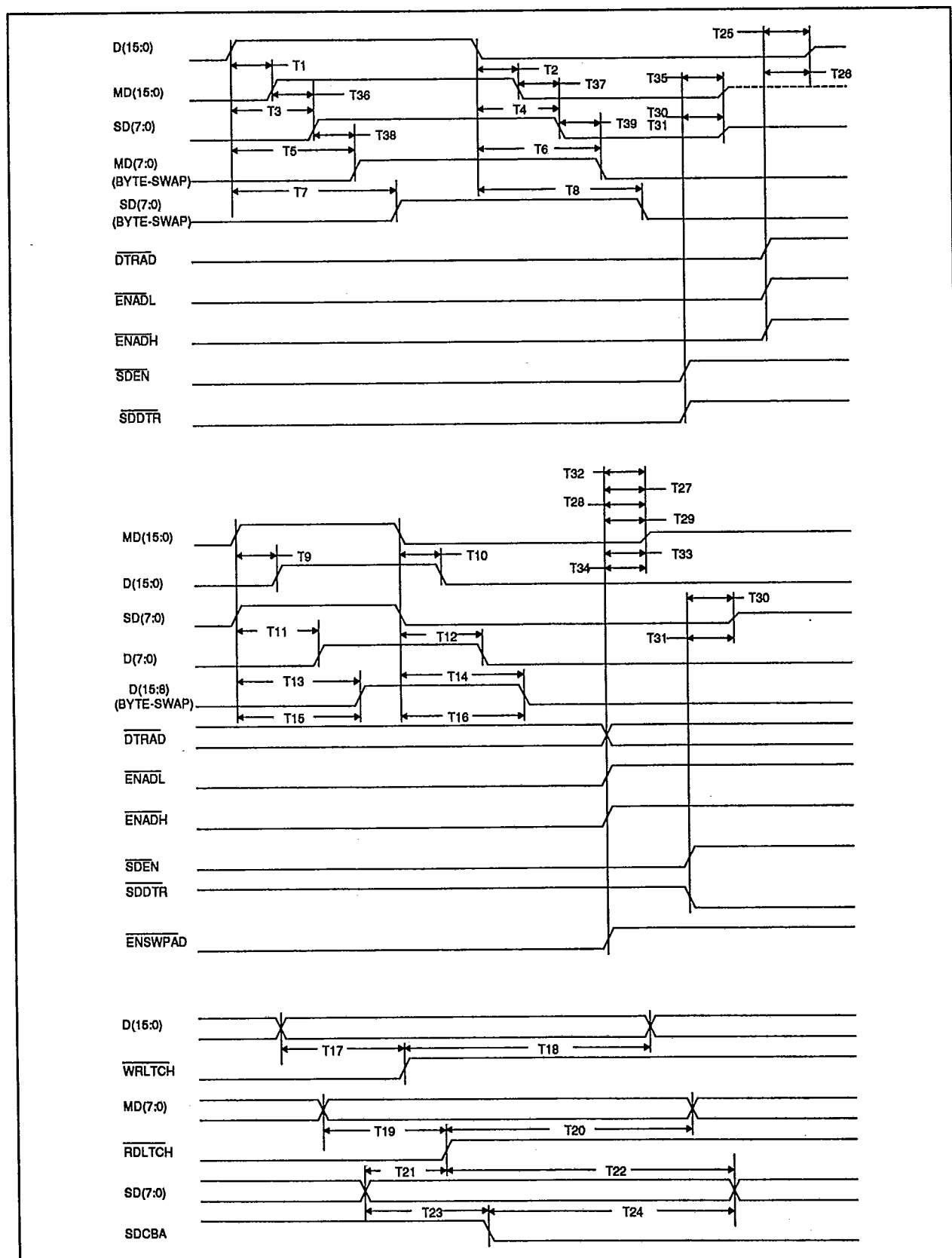


Figure 6. Data Path Timing

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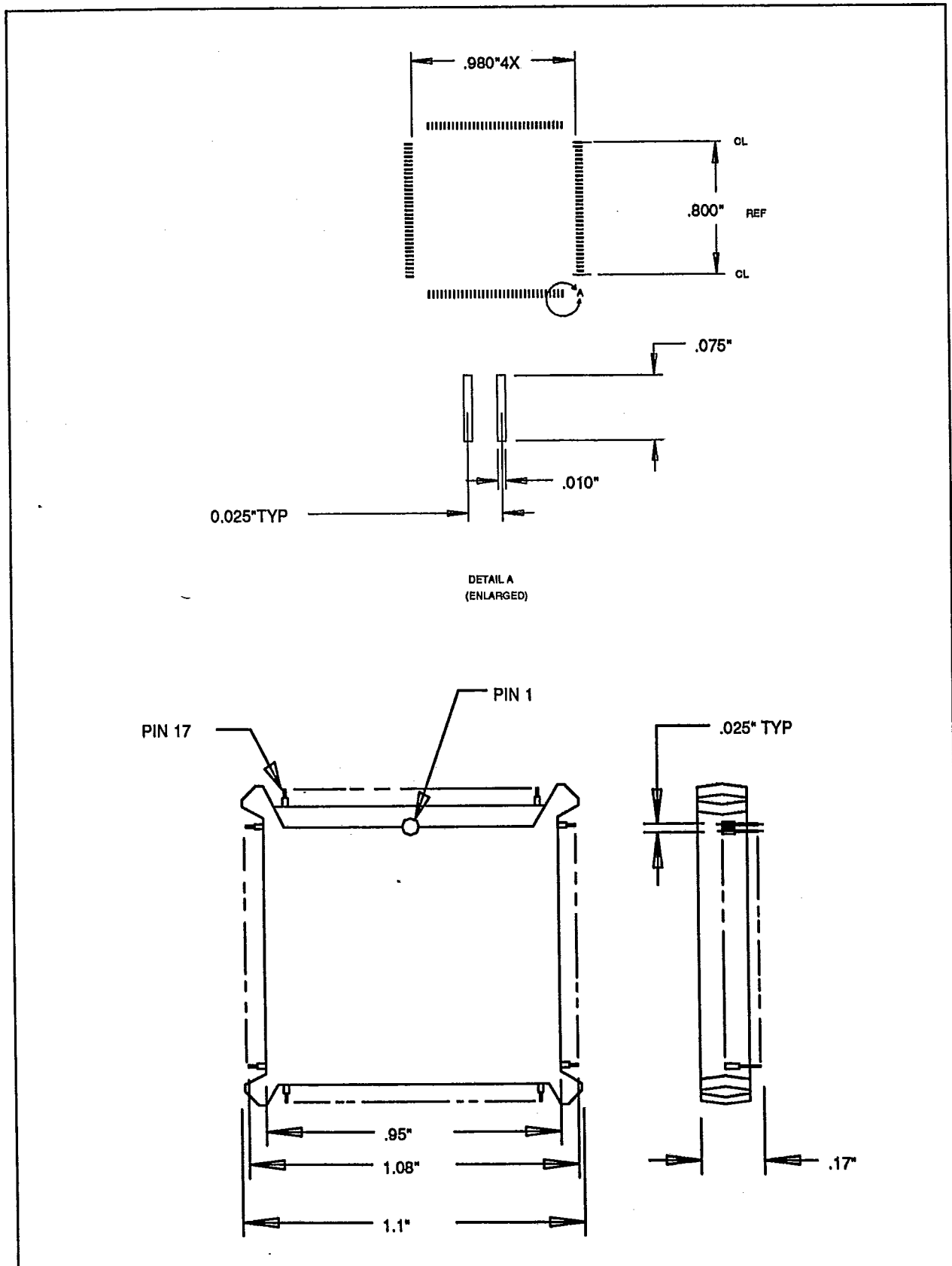
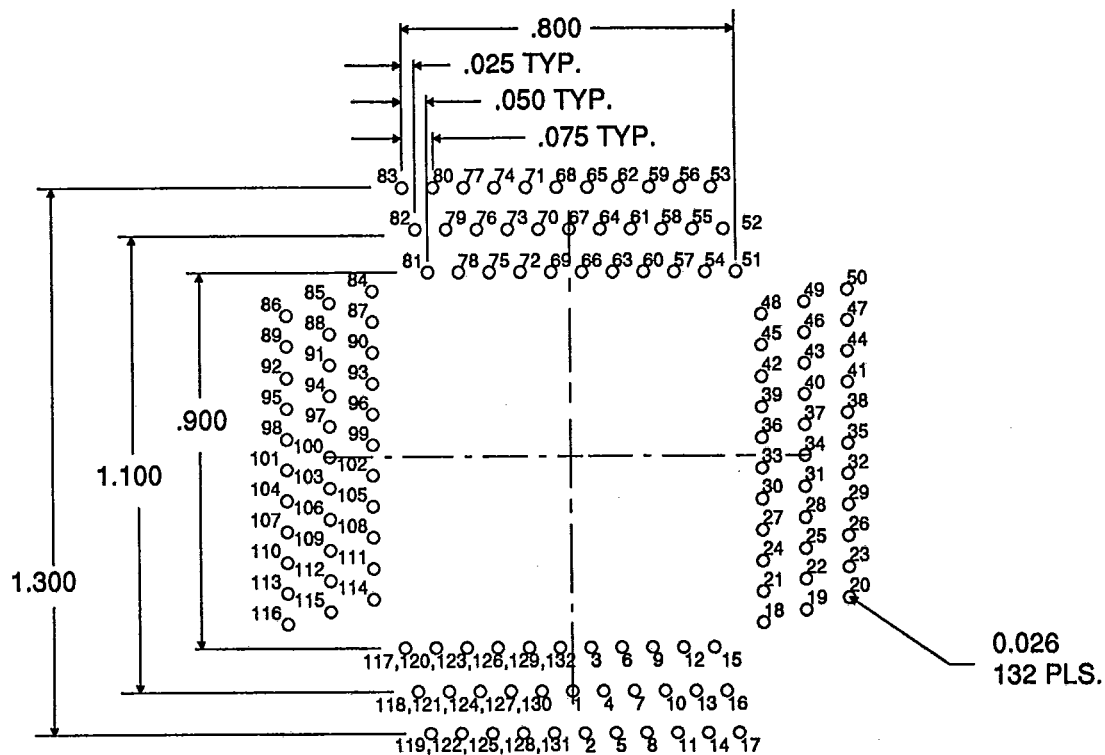


Figure 7. 132 JEDEC Flat Pack Packaging Diagram

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RECOMMENDED P.C. BOARD HOLE PATTERN
 SOCKET SIDE
 132 POSN

Amp Incorporated
 Harrisburg PA
 Part No. 821932-1

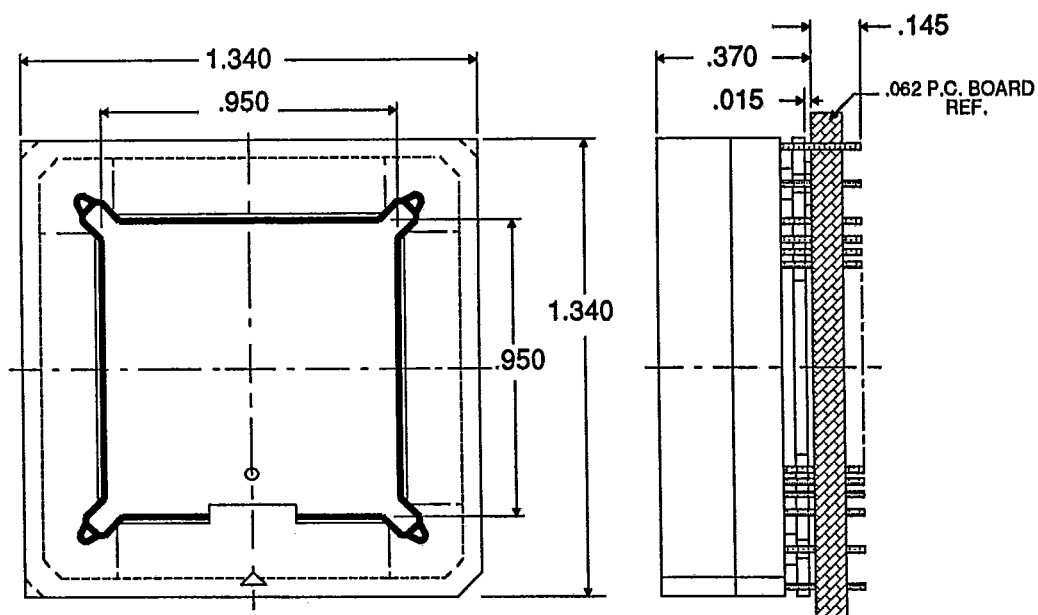


Figure 8. Socket Diagram